Lecture 16
Differential Amplifiers – I
Basics

In this lecture you will learn:

• Differential Amplifiers
• Differential FET Amplifiers
• Large Signal and Small Signal Analysis
• Half Circuit Techniques

Ideal Differential Amplifiers

An ideal differential amplifier amplifies the difference signal between two inputs:

\[ \begin{align*}
V_{i1} & \quad + \quad A_{vd} (V_{i1} - V_{i2}) \\
V_{i2} & \quad - 
\end{align*} \]

The need for differential amplifiers:

Differential amplifiers are used to remove unwanted signals that are common to both input signals.

For example, in many cases useful information is carried by the difference between two signal sources, 1 and 2, and unwanted noise signals that add to both the 1 and 2 signals will be rejected by a differential amplifier which will only amplify the difference of these signals.

These unwanted signals that add to both signals 1 and 2 could be a result of:

a) Variation in the power supply voltage as a function of time
b) Variation in the substrate potential of the entire chip
c) Variation in the temperature of the chip
d) Electromagnetic interference signals from the environment
Difference Mode and Common Mode Signals

The difference-mode and the common-mode components of two signals are:

- Difference-mode component: \( v_{id} = v_{i1} - v_{i2} \)
- Common-mode component: \( v_{ic} = \frac{v_{i1} + v_{i2}}{2} \)

Any two signals can be written in terms of their difference-mode and common-mode components:

- \( v_{i1} = v_{ic} + \frac{v_{id}}{2} \)
- \( v_{i2} = v_{ic} - \frac{v_{id}}{2} \)

Differential Amplifier: Single-Ended Output

- \( v_{out} = A_{vd} (v_{i1} - v_{i2}) + A_{vc} \left( \frac{v_{i1} + v_{i2}}{2} \right) \)
- Difference-Mode Gain: \( A_{vd} \)
- Common-Mode Gain: \( A_{vc} \)

One always wants the difference-mode gain to be much much larger than the common-mode gain (ideally one would want the common mode gain to be zero!)

Common-Mode Rejection Ratio (CMRR):

\[
CMRR = \frac{A_{vd}}{A_{vc}}
\]
Differential Amplifier: Double-Ended Output

\[ v_{o1} = \frac{A_{vd}}{2} (v_{i1} - v_{i2}) + A_{vc} \left( \frac{v_{i1} + v_{i2}}{2} \right) \]

\[ = A_{vd} \frac{v_{id}}{2} + A_{vc} v_{ic} \]

\[ v_{o2} = -\frac{A_{vd}}{2} (v_{i1} - v_{i2}) + A_{vc} \left( \frac{v_{i1} + v_{i2}}{2} \right) \]

\[ = -A_{vd} \frac{v_{id}}{2} + A_{vc} v_{ic} \]

Difference-Mode Output:

\[ v_{od} = v_{o1} - v_{o2} = A_{vd} v_{id} \]

Common-Mode Output:

\[ v_{oc} = \frac{v_{o1} + v_{o2}}{2} = A_{vc} v_{ic} \]

One always wants the difference-mode gain to be much much larger than the common-mode gain

Common-Mode Rejection Ratio (CMRR):

\[ CMRR = \frac{A_{vd}}{A_{vc}} \]

FET Differential Amplifiers

Comments:

\[ I_{D1} + I_{D2} = I_{BIAS} \]

Comments:

\[ I_{D1} + I_{D2} = -I_{BIAS} \]
**FET Differential Amplifier: Common Mode Input (Rough Analysis)**

\[ I_{D1} = I_{D2} = \frac{I_{BIAS}}{2} \]
\[ V_{O1} = V_{O2} = V_{DD} - \frac{I_{BIAS}}{2} R \]

Still: \( I_{D1} = I_{D2} = \frac{I_{BIAS}}{2} \)
\[ \Rightarrow \Delta V_{O1} = A_{vc} \Delta V = 0 \]
\[ \Delta V_{O2} = A_{vc} \Delta V = 0 \]
\[ \Rightarrow A_{vc} = 0 \]

**FET Differential Amplifier: Difference Mode Input (Rough Analysis)**

\[ I_{D1} = I_{D2} = \frac{I_{BIAS}}{2} \]
\[ V_{O1} = V_{O2} = V_{DD} - \frac{I_{BIAS}}{2} R \]

Does not change from DC bias value

Now: \( (I_{D1} + \Delta I) + (I_{D2} - \Delta I) = I_{BIAS} \)
\[ \Rightarrow \Delta V_{O1} = \frac{A_{vd}}{2} \Delta V = -\Delta I R \]
\[ \Delta V_{O2} = -\frac{A_{vd}}{2} \Delta V = \Delta I R \]
\[ \Rightarrow A_{vd} = -2 \frac{\Delta I R}{\Delta V} \quad \text{Large} \]
**FET Differential Amplifier: Difference Mode Input (Rough Analysis)**

\[ \Delta V_{GS1} = \frac{\Delta V}{2} \]
\[ \Delta V_{GS2} = -\frac{\Delta V}{2} \]

\[ \Rightarrow \Delta I = g_m \Delta V_{GS1} = g_m \frac{\Delta V}{2} \]
\[ \Rightarrow A_{vd} = -2 \frac{\Delta I}{\Delta V} = -g_m R \]

**Currents:**

\[ I_{D1} = \frac{k_n}{2} \left[ (V_{GS1} - V_{TN})^2 + (V_{GS2} - V_{TN})^2 \right] \]
\[ I_{D2} = \frac{k_n}{2} \left[ (V_{GS1} - V_{TN})^2 \right] \]

Drain currents depend only on the difference-mode input signal.
A FET Differential Amplifier: Large Signal Analysis

Currents: 
\[ I_{D1} = \frac{I_{\text{BIAS}}}{2} + k_n \frac{V_{id}}{4} \sqrt{\frac{4I_{\text{BIAS}}}{k_n} - V_{id}^2} \]
\[ I_{D2} = \frac{I_{\text{BIAS}}}{2} - k_n \frac{V_{id}}{4} \sqrt{\frac{4I_{\text{BIAS}}}{k_n} - V_{id}^2} \]

Voltages: 
\[ V_{O1} = V_{DD} - I_{D1}R \]
\[ V_{O2} = V_{DD} - I_{D2}R \]

Difference-Mode Output Voltage:
\[ V_{Od} = V_{O1} - V_{O2} = -R_k n \frac{V_{id}}{2} \sqrt{\frac{4I_{\text{BIAS}}}{k_n} - V_{id}^2} \]

The difference-mode output is sensitive to only the difference-mode input and not to the common-mode input.
Half-Circuit Techniques

Consider the following linear circuit

Suppose the circuit consists of identical parts that can be separated into two symmetric half-circuits as shown:

Since the circuit is linear, and superposition will hold, one can decompose the input signals into difference-mode and common-mode signals and then separately consider the circuit response to each signal:

\[ v_{id} = v_1 - v_2 \]
\[ v_{ic} = \frac{v_1 + v_2}{2} \]
\[ v_{i1} = v_{ic} + \frac{v_{id}}{2} \]
\[ v_{i2} = v_{ic} - \frac{v_{id}}{2} \]
Half-Circuit Techniques: Difference-Mode Input

First consider the difference-mode input:

Because of symmetry, the nodes in the center will be at zero potential

Therefore, one can use the following half-circuit to perform the analysis:

Half-Circuit Techniques: Difference-Mode Input

Now consider the common-mode input:

Because of symmetry, the wires in the center will carry no current

Therefore, one can use the following half-circuit to perform the analysis:
A FET Differential Amplifier: Small Signal Analysis

**DC Bias:**

\[ V_{I1} = V_{I2} \]

\[ I_{D1} = I_{D2} = I_{BIAS} / 2 \]

The small signal model can be built using the standard techniques.

The small signal circuit models are always **linear**.

Does this circuit consist of two identical and symmetric halves??

A FET Differential Amplifier: Small Signal Analysis

**DC Bias:**

\[ V_{I1} = V_{I2} \]

\[ I_{D1} = I_{D2} = I_{BIAS} / 2 \]

The small signal model can be built using the standard techniques.

The small signal circuit models are always **linear**.

Now it does have two identical and symmetric halves!
A FET Differential Amplifier: Small Signal Analysis for Difference-Mode Input

Assume a difference-mode input

\[ v_{id} \]

\[ g_{mb1}v_{bs1} g_{m1}v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

Use the symmetric half-circuit for analysis

\[ g_{mb1}v_{bs1} g_{m1}v_{gs1} \]

\[ v_{id} \]

\[ v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

\[ g_{m1}v_{gs1} \]

\[ v_{A} \]

\[ v_{id} \]

\[ v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

\[ v_{id} \]

\[ v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

\[ g_{m1}v_{gs1} \]

\[ v_{A} \]

\[ v_{id} \]

\[ v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

\[ g_{m1}v_{gs1} \]

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\[ g_{m1}v_{gs1} \]

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\[ g_{m1}v_{gs1} \]

\[ v_{A} \]

\[ v_{id} \]

\[ v_{gs1} \]

\[ v_{o1} \]

\[ v_{o2} \]

\[ g_{m1}v_{gs1} \]

\[ v_{A} \]

\[ v_{id} \]

\[ v_{gs1} \]
A FET Differential Amplifier: Small Signal Analysis for Common-Mode Input

Use the symmetric half-circuit for analysis

\[ v_{oc} = \frac{v_{o1} + v_{o2}}{2} \]

\[ v_{o2} = v_{o1} \quad \Rightarrow v_{oc} = v_{o1} \]

\[ A_v = \frac{v_{oc}}{v_{ic}} = \frac{v_{o1}}{v_{ic}} \]

\[ v_{ic} = v_{gs1} + v_{s1} = v_{gs1} + i_d(2r_{oc}) \]

\[ i_d = g_{m1}v_{gs1} - g_{mb1}v_{s1} + \frac{v_{o1} - v_{s1}}{r_{o1}} \]

\[ = g_{m1}(v_{ic} - i_d(2r_{oc})) - g_{mb1}i_d(2r_{oc}) - \frac{i_dR + i_d(2r_{oc})}{r_{o1}} \]

\[ \Rightarrow i_d = \frac{g_{m1}v_{o1}}{r_{o1} + R + 2r_{oc} + (g_{m1} + g_{mb1})r_{o1}(2r_{oc})} \]

\[ A_v = \frac{v_{o1}}{v_{ic}} = \frac{-i_dR}{r_{o1} + R + 2r_{oc} + (g_{m1} + g_{mb1})r_{o1}(2r_{oc})} \]

A FET Differential Amplifier: CMRR

Difference-Mode Gain:

\[ A_{vd} = \frac{v_{od}}{v_{id}} = -g_{m1}(r_{o1} \| R) \]

Common-Mode Gain:

\[ A_v = \frac{v_{oc}}{v_{ic}} = -\frac{g_{m1}r_{o1}R}{r_{o1} + R + 2r_{oc} + (g_{m1} + g_{mb1})r_{o1}(2r_{oc})} = -\frac{g_{m1}(r_{o1} \| R)}{1 + \frac{2r_{oc}}{r_{o1} + R}[1 + (g_{m1} + g_{mb1})r_{o1}]} \]

Common-Mode Rejection Ratio (CMRR):

\[ CMRR = \frac{A_{vd}}{A_v} = 1 + \frac{2r_{oc}}{r_{o1} + R}[1 + (g_{m1} + g_{mb1})r_{o1}] \]

\[ \approx g_{m1}(2r_{oc}) \quad \text{Large if } r_{oc} \text{ is large} \]