ECE4740: Digital VLSI Design

Lecture 14: Pass transistors and transmission gates

500

Ratio'ed logic

Other CMOS logic styles

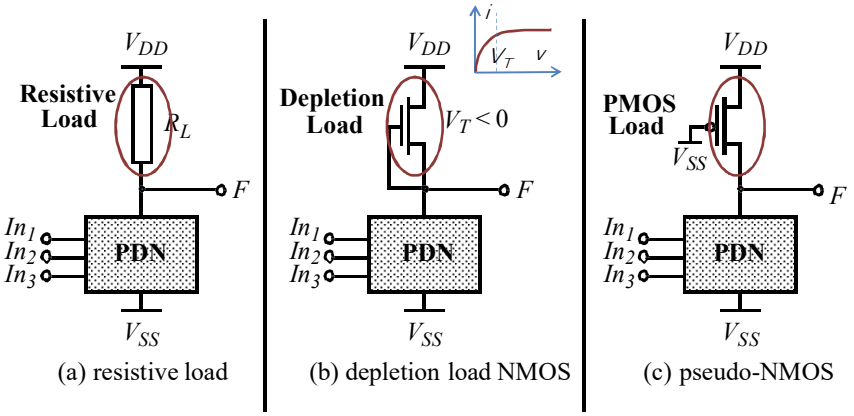
501

Why do we even care?

- Advantages of static CMOS
  - Low static power
  - Robust
  - Supported by most synthesis & back-end tools
- "Disadvantages" of static CMOS
  - For N inputs, requires (at least) 2N transistors
  - PUN can be area consuming
  - Same function is computed twice

502

Ratio'ed logic

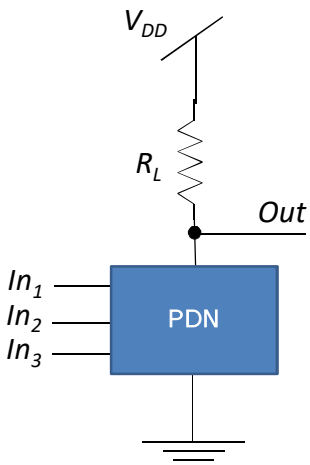


- Goal: Reduce # of transistors over CMOS
- Ratio'ed = functionality depends on ratios!

503

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Ratio'ed logic with resistive load



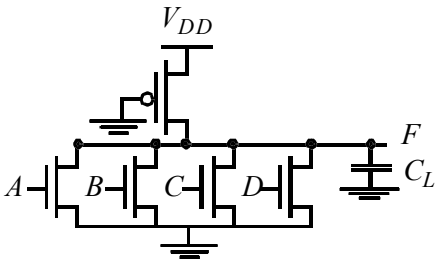
- N transistors + load R_L
- $V_{OH}=V_{DD}$
- $V_{OL}=R_{PDN}/(R_{PDN}+R_L)$
- Asymmetric VTC
- Reduced noise margin
- Static power consumption
- $t_{pLH}=0.69R_LC_L$
- What is t_{pHL}?

remember 2015 practice prelim 1?

remember 2015 practice prelim 1?

504

Pseudo-NMOS w/ active load



- $V_{OH}=V_{DD}$
- For V_{OL} assume NMOS lin. & PMOS sat.

$$V_{OL} \approx \frac{\mu_p W_p}{\mu_n W_n} V_{DSATp}$$

to make V_{OL} small make PMOS small

505

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

VTC of pseudo-NMOS

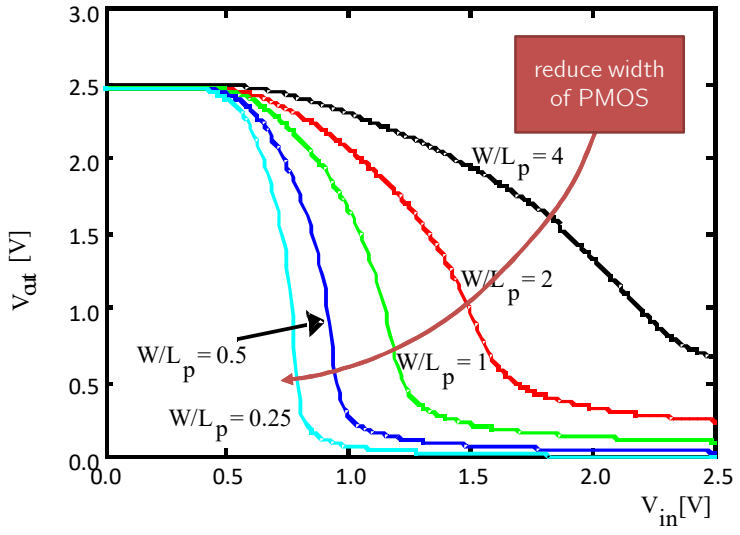


Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

506

Disadvantage: Static power

- Static power consumption when output is low (direct current through PMOS)
- Assume PMOS is in saturation:

$$P_{low} = V_{DD} I_{low} \approx V_{DD} \left| k_p \left(-(V_{DD} - V_{Tp}) V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) \right|$$

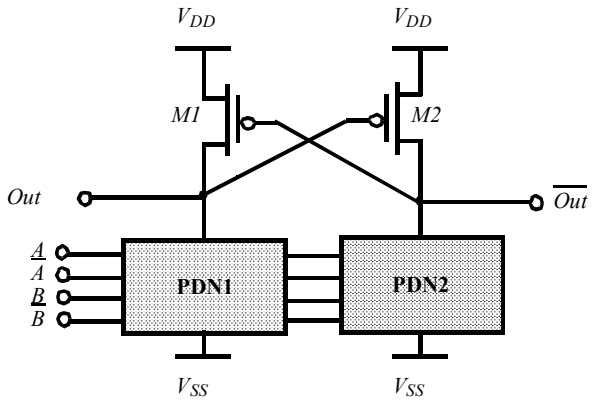
- One would need better loads!

507

Ratio'ed logic

Other CMOS logic styles

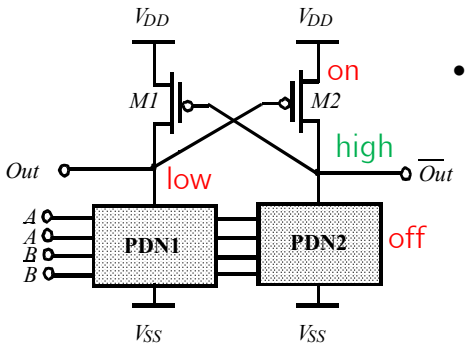
Improving loads is critical



- Differential cascode voltage switch logic (DCVSL)

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

DCVSL details

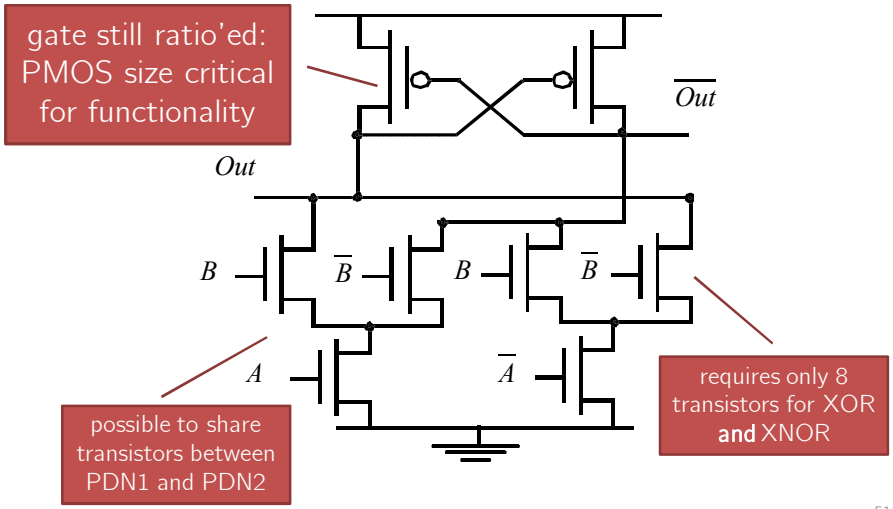


- PDN1 and PDN2 are mutually exclusive
  - If PDN1 conducts PDN2 is off
  - And vice versa

- DCVSL has full rail-to-rail swing
- No static power consumption
- Provides complementary signal
- Gate is still ratio'ed!

510

DCVSL example: XOR/XNOR



511

Image taken from: CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Harris

Why aren't we always using DCVSL?

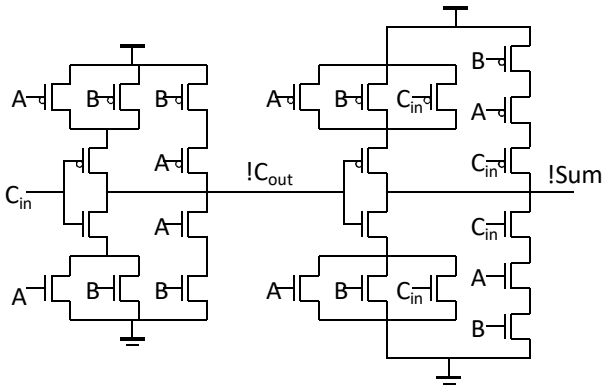
- Advantages of differential cascode voltage switch logic (DCVSL) over static CMOS
  - Complementary outputs immediately available
  - May reduce # of transistors up to 2x
  - Keeps values (similar to latches)
- Disadvantages
  - Doubles number of wires (affects density)
  - Often higher dynamic power dissipation
  - Design tools mostly handle only static CMOS

Useful for certain logic gates

Pass-transistor logic

Full adder in static CMOS

C_{in}	A	B	Σ	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



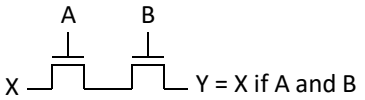
- Requires 24+4 (for C and Sum inv.) transistors

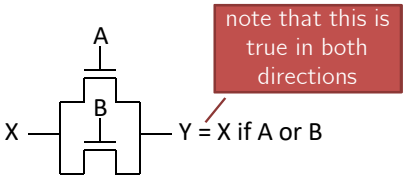
514

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Is there a better way?

- XOR/XNOR gates usually require a large number of transistors in static CMOS logic
- Remember: pass transistors
  - NMOS switch closes if gate input is high



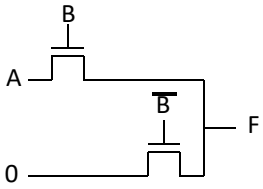


- But, NMOS pass strong 0 but weak 1

515

Pass transistor (PT) logic

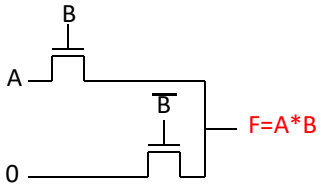
- What is this circuit doing?



- Find truth table
- Is it static (is there always a low impedance path to both rails)?
- How many transistors would you need with static CMOS?

516

AND gate with pass transistors



A	B	F=A*B
0	0	0
0	1	0
1	0	0
1	1	1

- Requires 4 logic gates (needs an inverter)
- CMOS logic would require 6 logic gates
- The gate can be static
- No rail-to-rail swing

517

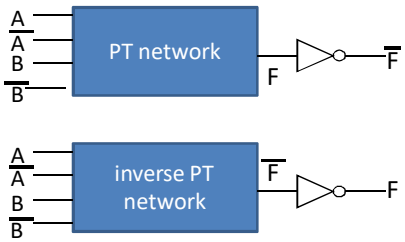
Properties of PT logic

- Gate can be static (if designed properly)
- N transistors instead of 2N
- Usually no static power consumption
- Ratioless
- Gate has no signal directivity, i.e., is bidirectional (versus unidirectional)
- Non-inverting logic

518

Complementary PT logic (CPL)

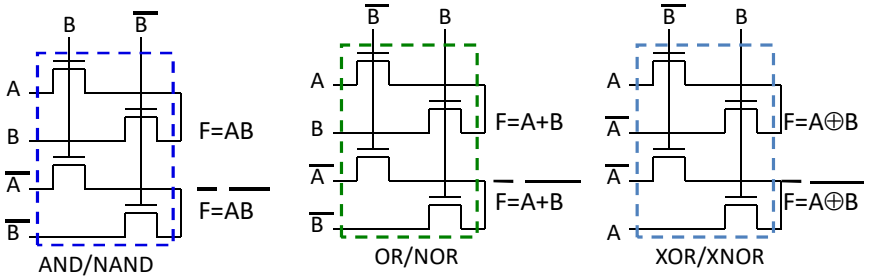
- Also called differential PT logic (DPL)



- Similar to DCVSL
  - Input complementary inputs
  - Output complementary outputs

519

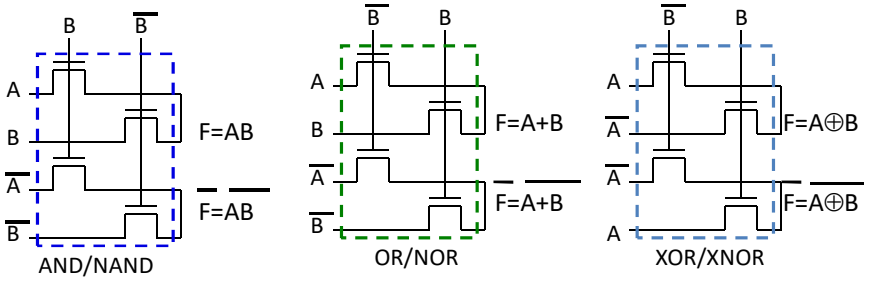
CPL/DPL efficient for XOR etc.



- Pros
  - No need for extra inverters (theoretically)
  - Static and modular (same topology)
  - Simple XOR (good for adders)

520

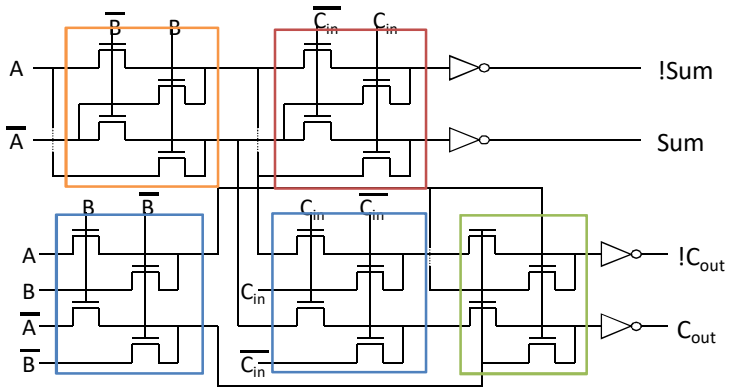
Disadvantages of CPL/DPL



- Cons
  - Additional routing overhead (2x)
  - Static power dissipation problems
  - Bidirectional

521

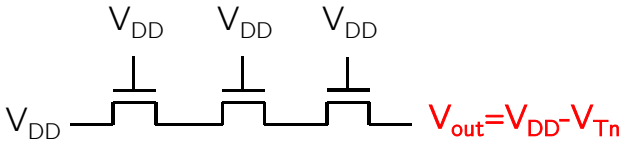
CPL/DPL-based full adder

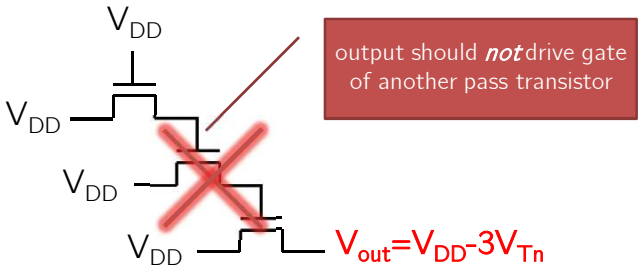


- 20+4*2 = 28 transistors (=static CMOS)
- Why are we using inverters at the output?

522

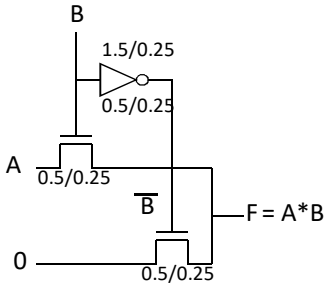
Cascading pass transistors

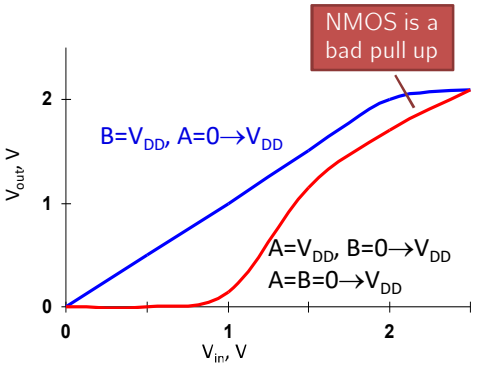




523

VTC of PT AND gate



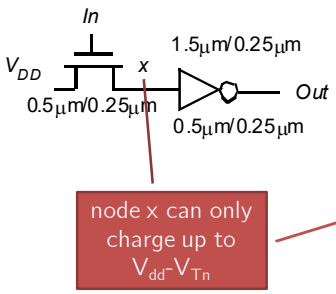


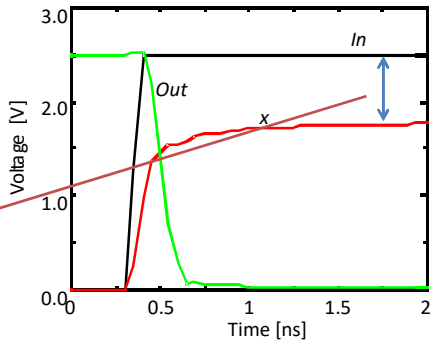
- Pure PT logic is not regenerative
  - Signal gradually degenerates after passing through a number of PTs (use inverters to fix)

524

Buffered pass transistor logic

- Buffer needed to recover weak 1



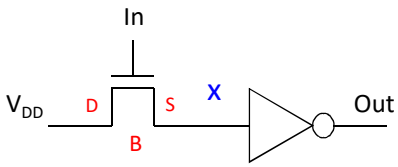


- Body effect makes it even worse

525

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Body effect revisited

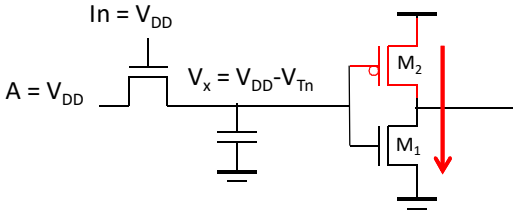


- Large V_{SB} when pulling high (B is tied to GND and S charged close to V_{DD})
- Voltage drop at node x is even worse

$$V_x = V_{DD} - \left(V_{Tn0} + \gamma \left(\sqrt{|2\phi_f| + V_x} - \sqrt{2\phi_f} \right) \right)$$

526

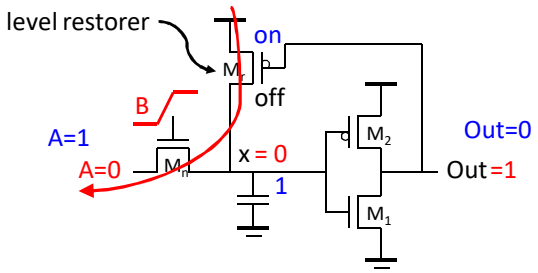
V_T drop causes static power



- Pass transistor suffers from body effect
- M_2 may be weakly conducting forming a path from V_{DD} to GND

527

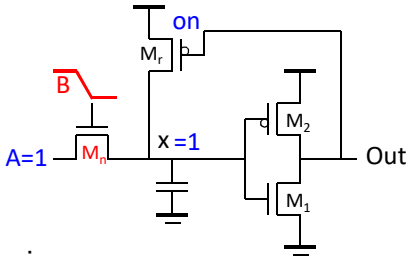
Solution 1: level restorer



- Full swing on node x → no static power
- No static backwards current (restorer only high when A is high)
- For correct operation M_r must be sized properly → results in ratio'ed logic!

528

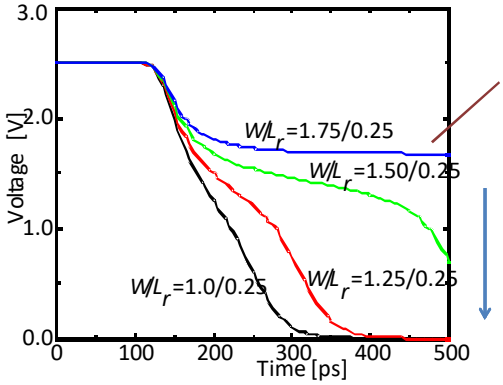
Solution 1: level restorer (cont'd)



- Ratio'ed logic:
  - When node x going from 1 to 0, M_n must be stronger than pull up M_r
  - Otherwise x never goes below V_M of inverter
- Need to size M_n and M_r

529

Sizing the level restorer



node x never goes below V_M

make restorer weaker:
→ increase R_{eqr}

- Restorer also affects speed and power
  - Increases capacitance at node x

530

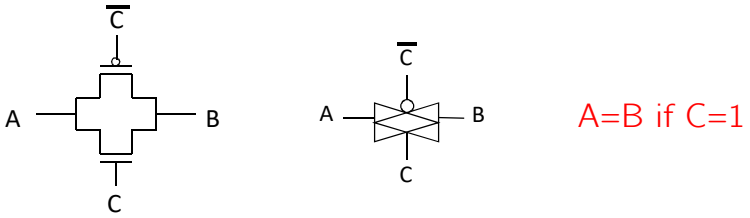
Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Proper way of using pass transistors

Transmission gates

531

Transmission gate

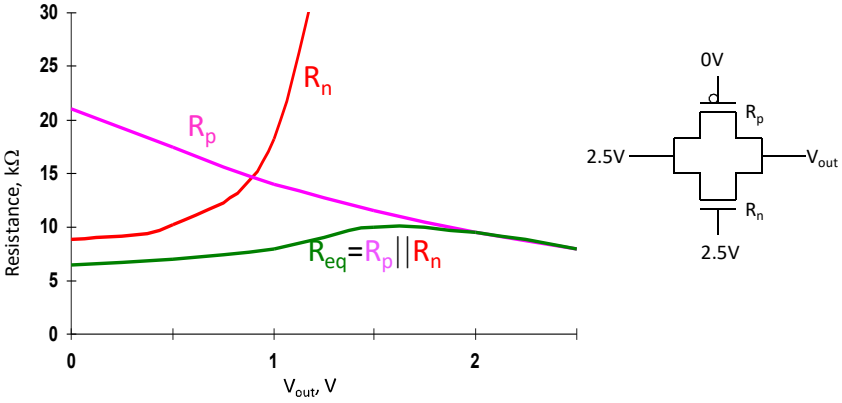


A=B if C=1

- Full swing bidirectional switch controlled by the gate signal C
- NMOS good pull-down; PMOS good pull-up
- Enables rail-to-rail swing

532

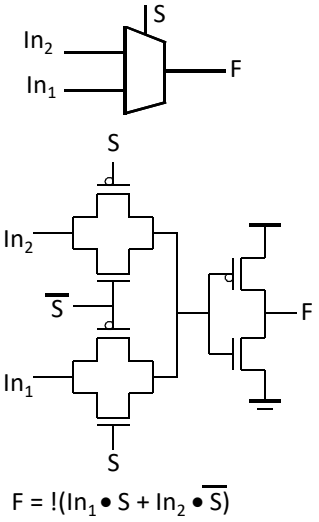
Resistance of transmission gate



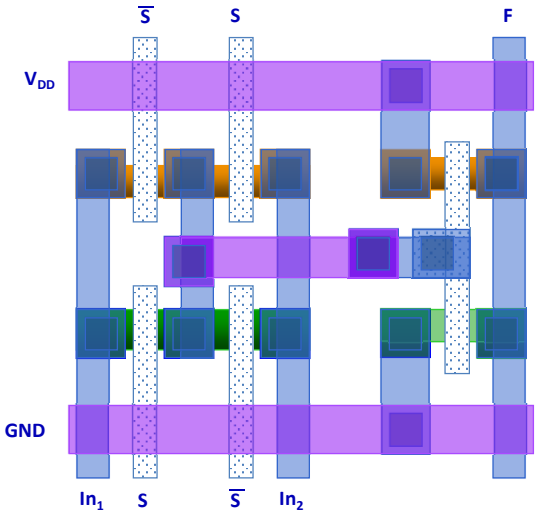
- TG has only mild non-linearity

533

TG 2-to-1 multiplexer (MUX)

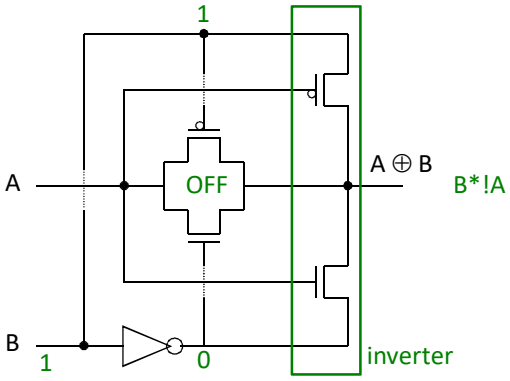


$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$



534

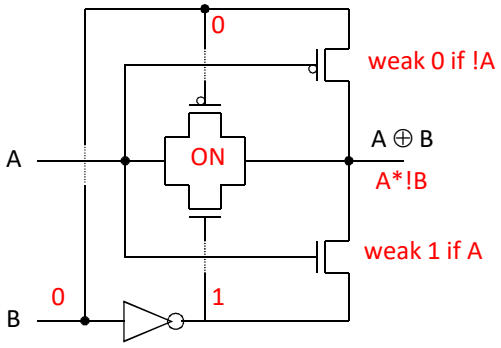
XOR gate using transmission gates



- Requires only 6 transistors
- CMOS requires 12 transistors

535

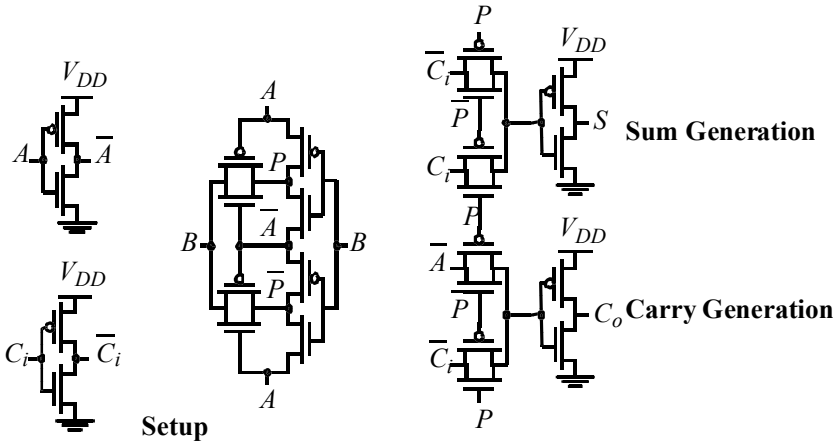
XOR gate using transmission gates



- Requires only 6 transistors
- Transmission gate ensures no voltage drop!

536

TG-based full adder

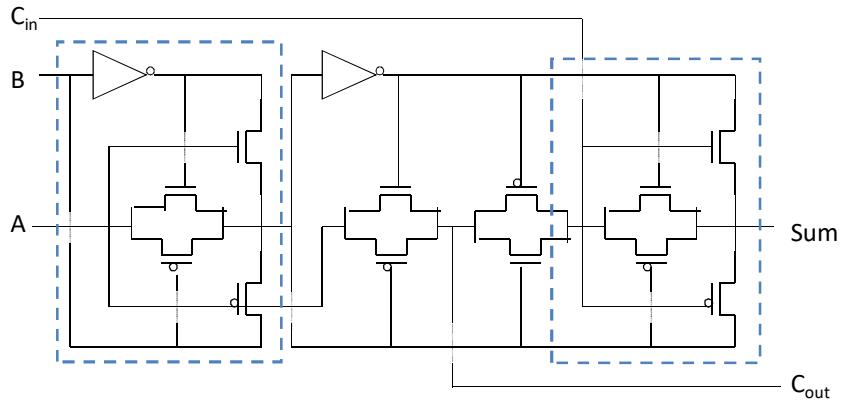


- Similar delays for sum and carry

537

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

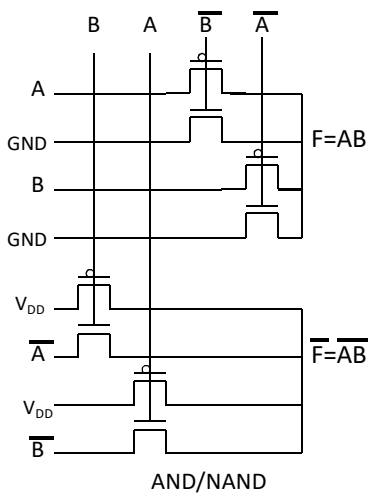
TG-based full adder (cont'd)

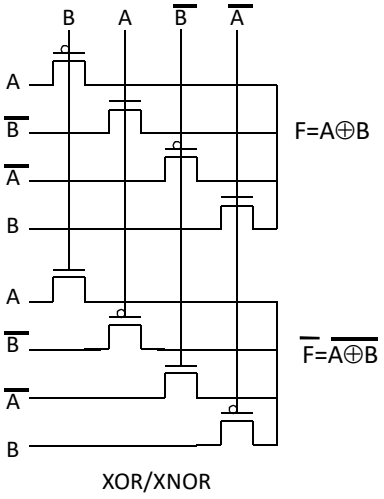


- 16 transistors (opposed to 28 for CMOS)
- Full rail-to-rail swing

538

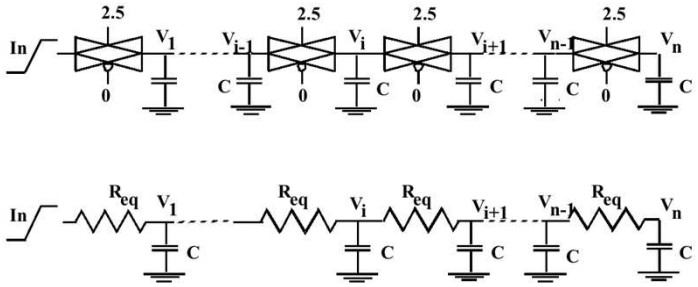
(Differential TG logic)





539

Caveat: delay in TG networks



- Elmore delay of RC chain:

quadratic delay increase in number of TGs

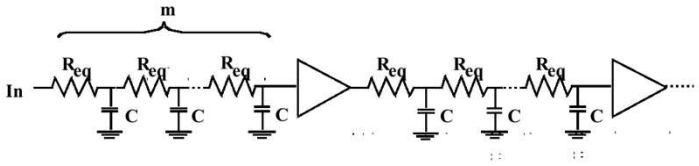
$$t_p = 0.69 \sum_{k=0}^{n} CR_{eq}k = 0.69CR_{eq}\frac{n(n+1)}{2}$$

540

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic

Delay optimization

- Insert buffers into TG network



$$t_p = 0.69CR_{eq}\frac{n(m+1)}{2} + \left(\frac{n}{m} - 1\right) t_{inv}$$

- Optimum number of buffers:

rule of thumb: no more than 2-3 TGs in series

$$m_{opt} = 1.7\sqrt{\frac{t_{inv}}{CR_{eq}}} \approx 3.4$$

541

Image taken from: Digital Integrated Circuits (2nd Edition) by Rabaey, Chandrakasan, Nikolic