Physics-Based Reliability Guidelines for Flip-Chip Devices (FCOB and FCOF)

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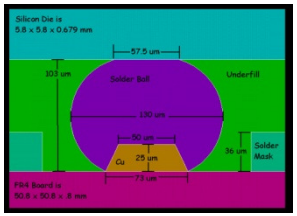
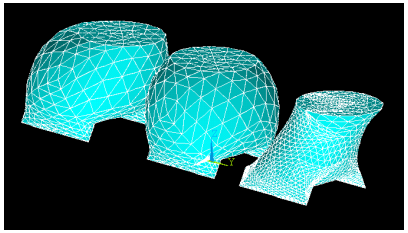
OBJECTIVES:

•Develop integrated process-reliability models, to determine reliability of face-down devices under thermal cycling and long-term temperature dwelling
•Study the effect of process-induced defects on interconnect failure: Shadow Voids, Incomplete Underfill Dispensing, Silica Particle Settling, Delamination
•Use the physics-based models to study the failure modes such as die cracking, solder cracking with and without underfill delamination
•Develop geometry, material and process guidelines for flip-chip devices
•Integrate predictions from the models into testbeds and enhance models from data from the testbeds



FE Cross-Section of FCOB Solder Ball



Solder Interconnect Shape as Predicted by Surface Evolver

APPROACH:

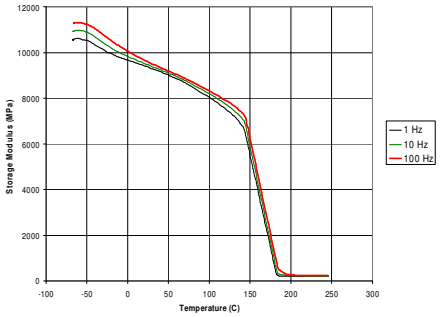
•To simulate underfill cure process taking into consideration the time and temperature-dependent material properties

•To determine stresses induced in the structure during assembly and subsequent thermal cycling.

•Characterize underfills to study their effect on reliability

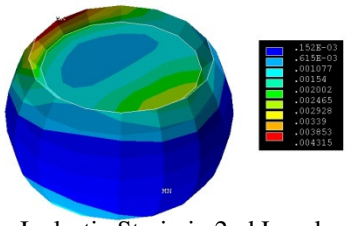
•Incorporate temperature, time-dependent material behavior into numerical models of FCOB, FCOF assemblies and Flip Chip CSP assemblies:

•Develop qualification guidelines for Flip-chip packages under various field-use

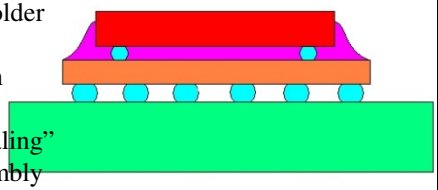


ACCOMPLISHMENTS:

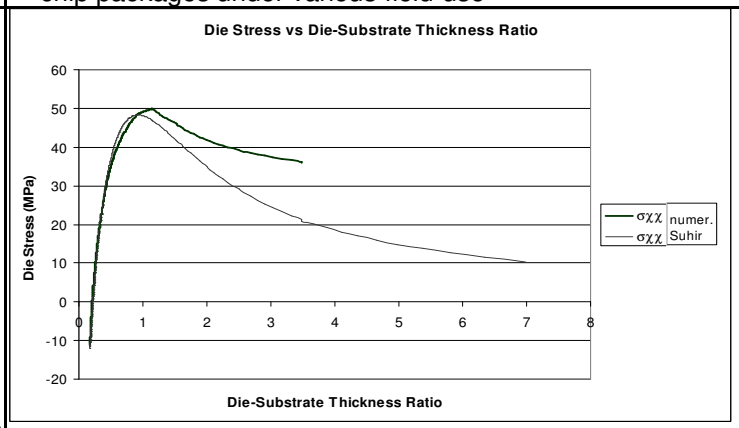
•This research has successfully integrated proces and reliability mechanics in numerical models
•This research has provided comprehensive desig guidelines against die cracking
•This research is the first to account for process-induced defects (incomplete underfill dispensing, shadow voids, etc), and sophisticated models to account for underfill delamination-induced solder cracking have been developed.
•Several advanced material models have been integrated with complex numerical models
• viscoplastic effects, damage, damage "healing"
•Design guidelines for reliable flip-chip assembly have been developed.

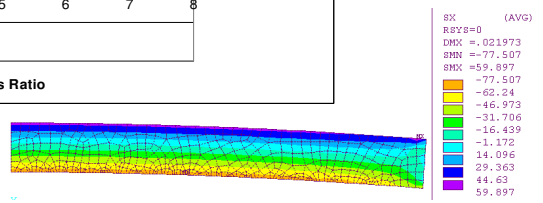


Inelastic Strain in 2nd Level Solder Bump of FC-CSP



Flip Chip CSP





Die Bending Stress at End of Underfilling Process