ECE Special Topic Course Request

1. Course Title: Advanced Digital Design with Verilog

2. Term and Year:
Spring 2018

3. Course Description (25 words or less):
Digital system design focusing on real world signal processing in FPGA devices using Verilog hardware descriptive language. The class focuses on real word design examples utilizing System Engineering design principles.

4. Level:
☐ 18xx ☐ 28xx
☐ 38xx ☐ 48xx
☒ 88xx (Graduate)

5. Instructor(s) for this offering: Tim Brothers

6. Campus(es) for this offering:
☒ Atlanta
☐ GT-Lorraine
☐ GT-Savannah
☐ GT-SJTU
☐ Video
☐ Other:

7. Credit Hours: ☒ 3-0-3 ☐ 2-3-3 ☐ 3-3-4 ☐ Other:

Laboratory (if applicable): ☐ unscheduled ☐ scheduled

For courses with substantial laboratory or project work, a 2-3-3 or 3-3-4 credit distribution may be appropriate. Institute policy requires all lecture courses (3-0-3, most 2-3-3 or 3-3-4) to have a final exam, given during the scheduled final exam period. For courses with major projects, an alternate final exam format (e.g., oral project presentations) may be approved.

8. Course taught previously? ☐ No ☒ Yes, list terms and enrollments: Spring 2017: 44 students

9. (GRADUATE only) **MS/PhD course domain(s):**

☐ Bio ☐ CSS ☐ DSP ☐ EDA ☐ Emag ☐ Energy ☐ Micro ☐ Optics ☐ Sys&Ctrl ☐ Telecom ☒ VSDD

Approval must be obtained from ALL TIGs responsible for the specified course domain(s) before submission to ECEGC.

10. Prerequisites: ☐ check here if there are NO prerequisites for this course

ece4270

Use an asterisk to indicate that concurrency is allowed and "[C]" to indicate that a minimum grade of C is required. For example, the prerequisites for ECE 4007 would be listed as follows: **ECE 3042[C] and ECE 4001***

ECE 4xxx courses are considered advanced topics in EE/CmpE and, therefore, generally must have another ECE course as prerequisite. Prerequisites for undergraduate courses are enforced and may not be waived by the instructor, although ECE graduate students will be granted prerequisite overrides. Prerequisites are not enforced for graduate courses.

11. Textbooks: ☐ check here if NO textbooks are to be ordered for this course

For each text to be ordered, specify either "required" or "optional" and provide the other requested information.
To specify more than three texts, include the information for the additional texts on the syllabus and check here: ☐

	Reqd/Opt	ISBN Number	Author, Title, Publisher, Year
a)	Required	9789401782	Seetharaman Ramachandran, "Digital VLSI System Design: A Design Manual for Implementation of Projects on FPGAs and ASICs using Verilog", Sprin
b)	Required		
c)	Required		

12. Special Considerations (*e.g., major/level restrictions, cross-listing with another department, non-traditional scheduling)*:

Cross Listed with Undergraduate ECE section.

This form must be submitted each time a course is proposed for offering as a special topic in ECE. To also request **permanent catalog listing**, the ***ECE New Course Request*** form must be completed and submitted along with this form.

In addition to this completed form, the following information is required (unless also included in a permanent listing request):

- Course syllabus, including a **1-page** topical outline and a description of how students will be evaluated or graded.
- Summary of grades assigned and CIOS student evaluations for all previous offerings of the course.

ECE Special Topic Course Request

After TIG approval, (1) all materials must be submitted to the chair of the ECE Undergraduate or Graduate Committee, as appropriate, and (2) this completed form and the course syllabus must be submitted **electronically** to Doug Williams.

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Course Information

ECE TBD, Advanced Digital Design with Verilog

T/R 12:05 - 1:25pm, Van Leer TBD

Spring 2018

Course Description

Digital system design focusing on real world signal processing in FPGA devices using Verilog hardware descriptive language. The class focuses on real word design examples utilizing System Engineering design principles. The class utilizes exploratory learning in a collaborative hands on environment.

Prerequisites

ECE 4270

Texts

- Seetharaman Ramachandran, "Digital VLSI System Design: A Design Manual for Implementation of Projects on FPGAs and ASICs using Verilog", Springer Publishing, 2007. ISBN: 978-94-017-8277-7

Contact Information

	Office Hours	Office	e-mail
Professor: Tim Brothers	TBD	TBD	404-407-7079 timothy.brothers@gtri.gatech.edu
TBD	TBD	TBD	TBD

Workload and Grading

There will be approximately 10-12 homework sets, 10-12 quizzes, a midterm, and a final exam. The lowest homework grade and the **two** lowest quizzes will be dropped. Grading is as follows (we reserve the right to deduct points for egregiously non-professional behavior):

Homework 25% Quizzes 25% Midterm 25% Final Exam 25%

Due Dates

- Homework is due at the beginning of class on Thursday.
- Quizzes will normally be at the start of class on Tuesday.
- Tests are specified in the course schedule at the end of this document. The dates are subject to change.

Homework

Homework is due at the ***beginning*** of class, and is divided between problems and programming assignments. Each of you is expected to turn in homework that is completely your own work, but you are encouraged to discuss problems and solution approaches with others. Be sure to attempt each problem on your own before seeking help. Working homework is the best way to learn the material and do well in the class. Homework must be neat and well-organized or it may not be graded or may have points deducted. **Be sure to put your name, date, section, and the assignment number on the front page or on a cover sheet.** Note that HW #12 is due at the end of dead week. Since you can drop one homework grade, you can choose to drop this last one so that you do not have anything due during dead week (or you can turn it in the week prior).

Quizzes

There will be quiz most weeks. The quiz will be 10 minutes at the start of the class. The objective of the quiz is to check your knowledge from the previous homework or class. Before the quiz you should review your notes and the previous homework solution to ensure you fully understand the concepts covered.

Tests
There will be two tests, a midterm and a final. These will NOT be cumulative tests, however the concepts in this class build on the previous information so it is important to understand all material presented in the midterm. **One** page of notes (single sided 8.5x11 inch) can be used on the midterm. **Two** pages of notes (single sided 8.5x11 inch) can be used on the final.

T-Square
T-Square (http://t-square.gatech.edu) is the primary means of distributing information. **Please note that homework assignments will be posted on T-Square and will not be handed out in class.** The following information will also be found on T-Square as it becomes available: (1) homework solutions, (2) class grades, (3) this syllabus, and (4) miscellaneous handouts.

Piazza
This term we will be using Piazza for class discussion. The system is highly catered to getting you help fast and efficiently from classmates, the TA, and myself. Rather than emailing questions to the teaching staff, I encourage you to post your questions on Piazza. If you have any problems or feedback for the developers, email team@piazza.com.

Find our class page at: https://piazza.com/class/iy1jp27hshr1f8

Getting Help
The material in this course builds on earlier material, so it is very important to not get behind. Be sure to take advantage of office hours and other resources that are available. If you can't make office hours, email questions or arrange for an appointment. Check out the resources in the links below:
http://ecetutoring.gatech.edu/schedule.html, http://www.successprograms.gatech.edu/,
http://www.deanofstudents.gatech.edu/

Major Emergencies
If you have some sort of major life emergency – serious illness or injury, death in the family, house burns down or is flooded, etc. – that seriously impedes your progress in the class, please let us know as soon as possible so we can work something out. You will find professors can be quite reasonable if you keep us in the loop. Please do not disappear without warning halfway through, making us think that you dropped the class, and then reappear out of nowhere the week before finals asking what you can do to make things up.

On Things That Distract
Please consider this class practice for meetings once you obtain an engineering job. Act in a professional manner during class. Please silence all cell phones, tablets, pagers, etc. before entering class. If you need to leave the class please exit with the least amount of disturbance as possible.

In general, please do not text, instant message, web surf, Facebook, tweet, e-mail, play games, etc. during class. It can be quite distracting.

Honor Code (http://www.honor.gatech.edu/plugins/content/index.php?id=9)
Adherence to the Georgia Tech Honor Code is expected and all suspected instances of academic misconduct will be reported to the Dean of Students. It is your responsibility to ask for clarification if collaboration guidelines, test-taking policies, etc. are not clear.

Georgia Institute of Technology

Spring 2017, ECE 8813 Special Topics Section A
Instructor: Brothers, Timothy (Primary)

There were: 44 possible respondents.

	Question Text	N	RR	Interpol. Median	0-3	3-6	6-9	9-12	12-15	15-18	18 +	N/A
1	Student: Hours per week	44	100%		4	8	11	12	5	4	0	0
					0-30	30-50	50-70	70-80	80-90	90-100	N/A	
2	Student: Percent attendance	43	98%		0	0	0	2	6	35	0	
3	Student: Percent homework completion	43	98%		0	0	0	1	2	40	0	
					5 Extremely Well	4	3	2	1 Completely Unprep	N/A		
5	Course: How prepared to take subject	44	100%	3.6	9	15	11	9	0	0		
					5 Exceptional Amt	4	3	2	1 Almost Nothing	N/A		
6	Course: Amount learned	44	100%	4.1	14	19	8	3	0	0		
					5 Exceptional	4	3	2	1 Very Poor	N/A		
7	Course: Assignments facilitated learning	42	95%	4.4	20	14	6	2	0	0		
8	Course: Assignments measured knowledge	44	100%	4.6	24	16	2	2	0	0		
					5 Strongly Agree	4	3	2	1 Strongly Disagree	N/A		
9	Course: Overall effectiveness	44	100%	4.3	19	17	4	4	0	0		
					5 Exceptional	4	3	2	1 Very Poor	N/A		
14	Instructor: Clarity (Brothers)	44	100%	4.2	15	20	8	0	1	0		
					5 Strongly Agree	4	3	2	1 Strongly Disagree	N/A		
15	Instructor: Communicated how to succeed (Brothers)	44	100%	4.6	25	14	3	1	1	0		
					5 Exceptional	4	3	2	1 Very Poor	N/A		
16	Instructor: Respect for students (Brothers)	44	100%	4.9	37	5	2	0	0	0		
					5 Extremely Enthus	4	3	2	1 Detached	N/A		
17	Instructor: Enthusiasm (Brothers)	44	100%	4.9	37	5	2	0	0	0		
					5 Made Me Eager	4	3	2	1 Ruined Interest	N/A		
18	Instructor: Stimulates interest (Brothers)	44	100%	4.5	23	14	5	1	1	0		
					5 Highly Accessible	4	3	2	1 Hard To Find	N/A		
19	Instructor: Availability (Brothers)	44	100%	4.9	34	7	3	0	0	0		
					5 Extremely Helpful	4	3	2	1 Not Helpful	N/A		
20	Instructor: Feedback helpfulness (Brothers)	44	100%	4.6	24	10	7	2	1	0		
					5 Strongly Agree	4	3	2	1 Strongly Disagree	N/A		
21	Instructor: Overall effectiveness (Brothers)	43	98%	4.6	25	12	5	0	1	0		

Instructor	Text Responses
	Question: Course best aspect
	Diverse range of topics covered. Flexibility in the class schedule to discuss more obscure points with practical examples.
	Approach to design and verilog
	I like that the class focuses on practical skills as opposed to theory.

	hands on
	the instructor is quite friendly and it was interactive course
	Practical and iterative assignments. Group effort was needed which helped interpersonal coordination skills. Totally industry oriented. Perfect!
	The projects all were based on real-time problems which were interesting to work on.
	Learning of the language Verilog through interesting assignments and a weekly assessment of self through quizzes.
	Very Good Assignments
	There were only few best aspect of this course: 1. Timing diagram 2. Algorithmic state machine 3. Verilog design standard
	Learnt good amount of data
	Some practical assignments and examples to practice.
	The class was set up to allow us to learn, to allow us to make mistakes and ask questions in class fearlessly. The weekly quizzes with a very small component going towards final grade is a great idea. It made sure I am up to date with the material. Yet, there was some flexibility for those hectic weeks and interviews.
	Dr Brothers is extremely enthusiastic and helps every single person with even the most basic questions. He is very easy to talk to and his classes are fantastic
	The HWs were very challenging. Quizzes every week kept us up to date with what was happening in class. Professor very approachable and responsive to doubts.
	The variety of assignments
	Design problems
	Quizzes and Discussions
	Quiz and homework
	Good learning experience
	The Quizzes were the best part! They were weekly held and motivated me to constantly work hard and learn as much as I could.
	The teaching methodology has been exceptional, creat ed an interest in me and everything that he has thought are directly being required in the CO-OP job as an asic design with INTEL
	Class Quizzes
	Weekly Quizzes, Doubt Sessions
	The best aspect of the course is that Professor really really wants us to learning how to design and be a good designer. He really wants that each and everyone in the class succeeds and learns the concepts. Also, Professor spends a lot of time (even 2-3 hours!) after every class for solving students' queries.
	design discussions, discussions emerging from quizzes
	Design techniques and coding styles
	Assignments with real life examples
	Prof is always available
	Question: Course improvements
	We never received any comments regarding our homework. This means I have no method for self improvement.
	less errors with homework and notes, too many corrections confused some of the concepts.
	Faster pace, more material. I feel like we had learned everything by the midterm (Top-down design, timing diagrams, ASMs).
	more coding teaching. I get that anyone could code but a lot of people could say anyone could figure out timing diagrams. Learning more coding during class means easier for us to do the homeworks and getting a good feel for verilog in general.
	Would have been nice to have actual FPGA hardware to target
	more preparation for the structured course and assignment
	More intuitive examples which give a directed effort towards some learning objective can be designed. Some examples which clearly point out the edge cases in learning should be included.
	Not everyone in class comes from verilog background, even though majority did, the projects became quite tough in the end. It should have been moderate.
	Could be improved by making the in-class course more challenging and at a higher level.
	Organizing the course contents
	It's definitely not a graduate level course... 1. It was not well formed.. 2. most of ths times we learn on our own.. 3. many time our learning is not aligned with instructor's intuition.. There was no documentation on the software that we were supposed to used.. initial homeworks were supposed to be simpler.. but it creat ed more chaos...
	Focus more on verilog, coding Take verilog examples from Computer Architecture world (Pipelines etc)
	Provide notes. we don't want to write down everything from board in our notebook. Either record lecture or provide all notes.
	Hope we can get more knowledge in FPGA, not only in verilog. Maybe we can try to perform our code on FPGA in the future.