Course Description:
The functionality and performance of today's computer system is increasingly dependent on the characteristics of the memory components. This course covers the semiconductor memory technologies from the device bit-cell structures to the memory array design with an emphasis on the industry trend and cutting-edge technologies. The first part of the course discusses the mainstream semiconductor memory technologies that enable various levels in the memory hierarchy, including SRAM, DRAM, and FLASH. Issues such as basic operation principles, device physics, manufacturing processes, bit-cell design considerations, array architectures and technology scaling trends will be discussed. The second part of the course discusses the emerging memory candidates that may have the potential to change the memory hierarchy, including STT-MRAM, PCM, and RRAM, as well as their new applications beyond the conventional applications, including reconfigurable logic, non-volatile logic, processing-in-memory, deep learning accelerators and neuromorphic hardware.

Prospective Students:
Graduate students in electrical and computer engineering program are welcome to take the course. Historically, the VLSI curriculum emphasizes on the logic components, e.g., the transistor technology at the device level or the microprocessor design at the architecture level. This course covers the overlooked part - the memory components, with a holistic view from the device level to the array architecture level. Therefore, the students majored in TIGs of nanotechnology and VLSI systems and digital design may be interested in taking this course to broaden their skills and vision. The course is a cutting edge technology-oriented course, thus the students are expected to actively read the related literature as part of the learning process.

Prerequisites
Undergraduate-level semiconductor device and digital circuit courses are required, e.g. ECE3040 Microelectronic Circuits, ECE3150 VLSI and Advanced Digital Design, or equivalence.
Graduate-level semiconductor device and digital circuit courses are recommended (not required though): e.g. ECE6450 Introduction to Microelectronics Technology, ECE6130 Advanced VLSI Systems, equivalence.

Assignments and Grading:
Homework 50%, 5 problem sets (10% each). Pre-knowledge about numerical tools such as MATLAB is required.
Midterm Exam 25%, close book and close lecture notes, one cheat sheet and a calculator allowed.
Final Exam 25%. close book and close lecture notes, one cheat sheet and a calculator allowed.

Outline

Semiconductor Memory and CMOS Scaling Overview
- Introduction, industry trend, technology trend

SRAM
- 6T cell operation
- Noise margin, stability, scaling issues, and layout
- Variability and reliability issues
- Recent trends: FinFET

DRAM
- 1T-1C cell operation
- Fabrication technology, structure, layout
- Recent trends: 3D TSV based DRAM

FLASH memory
- FLASH device physics
- NAND, NOR architecture
- Reliability, scaling issues
- Recent trends: 3D vertical NAND

Emerging memories
- Cross-point Array architecture
- RRAM
- PCM
- STT-MRAM

Memory Array Design
- Peripheral circuits
- Sense amplifier
- NVSim simulator

New applications
- Non-volatile cache/logic
- Programmable logic
- Hardware accelerator for deep learning