Digital VLSI-2: IC Validation and Characterization

Summary

ECE VLSI-1 and VLSI-2 constitute a comprehensive VLSI design experience for students involving theory, design, verification (in VLSI-1) and test of a fabricated CMOS digital VLSI design in (VLSI-2). The centerpiece of this course is a semester-long effort by student-teams to combine combine basic principles VLSI design with essential practices and principles that will allow a team of students to effectively validate and characterize a packaged silicon test chip which they have themselves designed in VLSI-1.

Upon successful completion of this course, students should be able to

1. Given a test plan, suitably equip a workbench to perform chip-testing, and write required programs in Python and C to generate test patterns for system validation and characterization.
2. Translate their understanding of hardware testing in the three various stages: Design (equipping a design with test features), Emulation (translating design descriptions into an FPGA) and finally Test Chip Validation to develop and execute a silicon "bring-up" plan.
3. Design, organize, contribute to and run effective test reviews to identify operational anomalies. Propose underlying causes and develop a test-flow to investigate these proposed mechanisms.
4. Communicate digital prototype function and performance using industry-standard charts and formats (Shmoo plots, f-V, f-Power, syndrome check, scan validation checks)

Lectures

Lectures/live-discussions for this class will be held **at dates and times TBD**

Instructors

Primary Instructor: Visvesh Sathe (sathe@gatech.edu)
Instructor office hours: The instructor will plan for two office hours per week. **Days TBD**
TA office hours: TA assignment for this class is **TBD**. If one is assigned, TA will offer 4 office hours. If one is not assigned, the instruction will increase office hours to 4 per week.

Pre-requisites

ECE4804-1 is the sole prerequisite. Students should be comfortable (or be willing to put in additional time and effort to be familiar) with basic FPGA implementation. Familiarity with a

scripting language (e.g. Python, Ruby), basic Git repository management, automated plotting (Matplotlib, pyplot) and productive editors (Sublime Text, Vim, Emacs etc.) are a huge design productivity booster and will be very helpful, though not required as prerequisites.

Grading

Students in this course will be graded based on 4 components:

- 1 midterm examination (70 minutes) administered between weeks 7 and 10 (15%)
- Individual test assignments of known-good-chips - 20%
- Individual design emulation assignments, where students will prepare their test plan on FPGA emulations of their designs - 15%
- Course participation: class involvement, contributing scripts, designs, use of discussion boards/online channels to disseminate useful tips, tricks and project related knowledge (10%)
- Final Chip-Testing project (team of 3) : Successful validation and implementation of test-plan objectives on the fabricated test chip. This effort includes a PCB daughter-card design and implementation component - (40%)

The VLSI-1 and VLSI-2 sequence together are very strenuous. In accordance, grading policy is expected to be liberal. The course is graded on a mean-adjusted bell-curve that is intended to yield higher grades. In effect, students with average performance in quizzes and homeworks, but a fully functional, verified, robust final project should expect an "A" in this class.

Bonus credits will be offered on multiple occasions to incentivize students to adopt techniques/methodologies and develop valuable industry-relevant skills for improving design quality/productivity. These Bonus credits will be awarded to provide a potential grade jump to students **after bell-curve based grade-assignment**.

Homework

Homework will take the form of assignments, provided to students to be worked on individually in the first half of the course. The objective of the assignments is to develop a firm grasp of (1) Basic functional test methodology; (2) Basic hardware characterization procedure; (3) Debug and hardware troubleshooting; Interpretation of measured silicon results.

IC design and test is a practitioner's art. Consequently, homework is not solely designed to facilitate mastering VLSI theory. Instead, homework is built to ***complement*** the theory taught in class to allow students to build hands-on techniques that are difficult to teach in a classroom setting. To complete these homework assignments, students will synthesize their (1) understanding of the theory covered in class lectures together with; (2) an ability to look through provided test plan and pattern generation documentation together with (3) skills they

will develop to effectively manage multiple designs, files, and tools to produce robust, functional designs.

Course Materials

Assignments, references, tutorials, lecture notes will be made available on Canvas. Students will submit their homework by placing their design and README files in assignment-designated directories.

Lecture videos will be recorded and provided. Because of the initial offerings of this class, and the technology-sensitive nature of some of it's content, the portal for viewing lecture material is TBD.

On-line communications will be conducted through MS-Teams. This communication will include announcements and Q&A. It is also intended to facilitate student-team communication during the course. *Please install and try out MS teams ahead of time if possible*

References: There are no required references for this class. Lecture notes, and reading assignments will be sufficient to understand the theoretical material I will cover in this class. Students who would like additional VLSI references can refer to the excellent and simply-written book by Weste and Harris or a more circuit-oriented book by Rabaey et al.

Course Expectations and Guidelines

Academic integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. It is expected that students will act in accordance with the highest ethical standards. Information on Georgia Tech's Academic Honor Code can be found here. Students suspected of cheating or plagiarizing on a quiz, exam, or assignment will be reported to the Office of Student Integrity without exception. The office will investigate the incident and identify the appropriate penalty for violations. **Distribution/Sharing course materials and/or using external sites for assistance (e.g., contributing to test banks, CourseHero, Chegg, or similar sites) is prohibited.**

Collaboration and group work

Students are **strongly** encouraged to discuss homework problem strategies and related concepts with one another. However, each student must formulate and turn in their own solutions written in their own words. Cases where scripts, programs, design descriptions, or any relevant material appear to be identical or nearly identical will be immediately referred to the Office of Student Integrity.

Absences, late assignments, and missed quizzes

Active participation in the class discussions is a factor in your grade. Attendance of lecture sessions is, however, **optional**. Please note that because quizzes are held at the beginning of

some lecture sessions, students who want to give the quiz but not attend the lecture are free to leave without any prejudice whatsoever. While your instructor would love, appreciate and try to elicit spirited discussion during lectures, it is appreciated that not all students will be comfortable with such a form of contribution. Students may contribute in other substantive ways, including sharing scripts, methodologies, answering questions posed by other students on MS teams etc.

As students in this course will hopefully eventually appreciate, homeworks constitute key checkpoints that contribute toward the timely construction of a quality design that will eventually be successfully tested. Maintaining a regular cadence toward project completion is critical. Submitting a late homework steals time from the next milestone, making it harder to meet, and so on until the executing the final project becomes un-viable. To actively avoid such a situation, late homeworks will be aggressively penalized with the intent of avoid your project spiralling out of control, and not serving as a punitive grade-discrimination mechanism.

Accommodations for students with disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404)894-2563 or disabilityservices.gatech.edu, as soon as possible, to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.

Student-Faculty expectations agreement It is important to strive for a atmosphere of mutual respect and responsibility between faculty members and students. In the end, a respect for knowledge and understanding, an appreciation for hard work, and respectful interactions all contribute to an environment conducive to learning and excellence. I encourage you to remain committed to the ideals of Georgia Tech while in this class. See www.catalog.gatech.edu/rules/22 for a description of some basic expectations that we can have of each other.

Outline

The outline below is to be treated as an approximation. Since this is the first offering of its kind ever, some run-time adjustments will be inevitable.

1. PCB design with an emphasis on signal and power delivery.
2. Packaging fundamentals.
3. Power delivery and regulation – supply noise (IR, LdI/dt), decoupling capacitance, best-practices.
4. Signal propagation – a designer's perspective on crosstalk and transmission line effects.
5. Standard interface protocols (SPI, USART, JTAG)

6. Test pattern generation for BIST, Scan-based validation