ECE 4833/8833: Advanced Glass-Core Package Technology

Fall 2024

Instructor: Dr. Mohanalingam Kathaperumal

Lecture Hours: Tuesday: 3.30-4.20 PM and Thursday, 3.30-4.20 PM

Lecture Location: Love Building Room # 299

Lab Hours: Tuesday, 4.35-7.20 PM. Wednesday 4.35-7.20 PM

Office Hours: Wednesday 3.00-4.30 PM

Office : Room 111, Pettit Microelectronics Building

Email: kmohan@ece.gatech.edu; Phone: (404)894-9394

Teaching Assistants: Lakshmi Narasimha Vijaykumar, Joon Woo Kim

Course Information:

Moore's Law has been a foundation for the semiconductor industry for more than 60 years enabling an unprecedent rate of improvement in monolithic integrated circuit (IC) performance and exponential increase in transistor density. However, due to several compounding effects, there is a very rapid and radical shift in the industry from the design and fabrication of complex monolithic ICs to heterogeneously integrated ICs. Where monolithic integration forms all circuit functions on a single common semiconductor (at the wafer scale), heterogeneous integration enables the concatenation of heterogeneous 'chiplets' of various functionalities (logic, I/O, memory, power conversion, passives, photonics, mm-wave, etc) and materials in a manner that mimics/exceeds monolithic-like performance and utilizing advanced off-chip '2.5D' and '3D' interconnects and packaging to provide flexibility in fabrication and design, improved scalability, reduced development time, and reduced cost. This new era of Moore's Law will be a game changer and will impact everybody.

The objective of this course is to introduce students to this 'new phase of Moore's Law' and to focus on the emerging field of glass-core packaging. This class will introduce students to various package substrate technologies, provide a detailed discussion of glass-core packaging processes and technologies through both lectures and labs, and introduce students to electrical and thermo-mechanical design considerations.

Week	Date	Lecture title	Lab

1	Aug 20 Aug 22	L1. Introduction (Prof. Bakir) L2. Introduction continued…(Prof. Bakir/Mohan)	No lab
2	Aug 27 Aug 29	L3: Electrical (Prof. Bakir/Lakshmi) L4: Electrical Continued….	Electrical Simulation: ADS and Sonnet Tutorial
3	Sep 3 Sep 5	L5: Overview of various Substrates L6: Glass Structuring; BC, TGC, TGV – Dry and Wet Proc	Glass cavity formation-fs laser fab
4	Sep 10 Sep 12	L7: Chip embedding-Tools embedding, alignment, adhesion L8: Materials for chip embedding..DAF, filling gaps-ABF. Die shift characterizations	Chip embedding/ABF lamination
5	Sep 17 Sep 19	L9: Embedded dies-passives, functional dies L10: Basics of Litho-reticle limit/Materials/General concepts	Warpage measurement/Shadow Moire (Labs 1-3: Report due)
6	Sep 24 Sep 26	L11: Litho continued…-MA/MLA/Direct write/Multi-photon L12: Seed layer metals/Tools/Sputtering/Eless..	PR/Lamination/Litho/ development
7	Oct 1 Oct 3	L13: Electroplating, 3D metal writing/printing L14: TGVs – Filling methods/reliability	Seed layer deposition/Plating of microvias

Week	Date	Lecture title	Lab
8	Oct 8 Oct 10	---------Exam 1 L13: Metrology -Warpage/Adhesion/Modulus/Stress	ABF lamination/microvia fabrication

9	Oct 15 Oct 17	L14: Metrology 2 - FIB/CSAM/Opt.Tomography L15: Microvias- Types Fab/Characterization/Images	Warpage and optical characterization of vias (Labs 4-8: Report due)
10	Oct 22 Oct 24	L16: Thermal Issues 1 L17: Thermal Solutions 2	HAST
11	Oct 29 Oct 31	L18: Thermo-mechanical reliability aspects – Incl modeling/simulations L19: Assembly-Materials-Solder/TIM/UF (Jack)	Capacitors-Characterization
12	Nov 5 Nov 7	L20: Assembly-Processes-CMP/TCB/Cu-Cu bonding (Jack) L21: Electrical Measurements of packages 1 (Paul Jo)	TGV drilling/sputtering vs eless
13	Nov 12 Nov 14	L22: Electrical Measurements of packages 2 (Paul Jo) L23:: Large (why) Packages for AI	Plating TGVs??
14	Nov 19 Nov 21	L24: Glass packages for RF/mm Wave Applications L26: Future of Glass packaging (?!)	Cross-section of fabricated panel (Optical/SEM)
15	Nov 26	L25-------Exam 2	(Labs 9-13: Report due)
16	Dec 5		Final Lab Report due: Abstract/ Introduction/Experimental/Results & Discussion and Summary

COURSE OUTCOMES

Upon successful completion of this course, students should be able to..

- perform signed and unsigned addition and subtraction, observing errors.
- analyze signals in terms of their frequency content.
- design discrete single-stage amplifiers using BJTs and MOSFETs.
- write laboratory reports and documentation conforming to technical writing standards.

- Explain the benefits and motivation of advanced packaging using glass core
- Design and analyze package architectures
- Design and characterization of material properties
- Explain fabrication steps and processes
- Explain methods of characterization
- Analyze fabricated glass-core packages
- Write laboratory reports and documentation conforming to technical writing standards.

Textbook Information:

Fundamentals of Device and Systems Packaging: Technologies and Applications, Rao R. Tummala, McGraw-Hill Education; 2nd edition (September 2, 2019)

Course Prerequisites:

CHEM 1211K

Prerequisites with concurrency: CHEM 1310, PHYS 2212

Course Grading:

Homework: 10%

Reports

Lab reports on the following topics as the lab work is completed (once in three weeks' time)

a) Chip Embedding module 8%
b) RDL Module 8%
c) Assembly Module 8%
d) Electrical characterization module 8%

- Final Report: 8%
  Including introduction, reports a-d (report of different modules) and conclusion (including references)
  Due on Final Exam (replacing the final exam)

Exams:

Exam 1: Lectures 1-13 20%

Exam 2: Lectures 13-25 20%

Attendance: 10%

Course Expectations & Guidelines

Commitment to Learning-Student Faculty Expectations

As the instructor for the course, I am devoted to introduce, educate, and provide resources to expand your knowledge in advanced packaging concepts. My intent in teaching this course is to make all the students taking this course to be as ready as possible to enter the workforce in leading industries working on semiconductor packaging including advanced glass core packaging.

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. For information on Georgia Tech's Academic Honor Code, please visit http://www.catalog.gatech.edu/policies/honor-code/ or http://www.catalog.gatech.edu/rules/18/.

Any student suspected of cheating or plagiarizing on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404)894-2563 or http://disabilityservices.gatech.edu/, as soon as possible, to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.