ECE4804/8804: Analog VLSI I – from Theory to Tapeout (Spring 2024)

MW 9:30am – 10:45am, Ford ES&T L1125

General Information

Instructor:

Primary: Shaolan Li, Assistant Professor in School of ECE
- Email: shaolan.li@ece.gatech.edu
- Office hours: TBD

TA: TBD

Course Summary

ECE 4804/8804 AVS constitutes a comprehensive analog IC learning experience for students involving theory, design, verification and test of a fabricated CMOS Analog VLSI prototype. The centerpiece of this course is a semester-long effort by student-teams to combine basic principles in analog design with essential practices and principles that will allow a team of students to produce quality designs productively. Designs built by individual student-teams will be fabricated in an industry standard CMOS process. The fabricated designs will be tested by student-teams to provide hands-on experience with a selection of industry standard test methodologies. This syllabus outlines the first part of the two-semester series, which focuses on design and tapeout.

Upon successful completion of this course, students should be able to:

1. Translate the high-level specification of an analog system in to building-block level specifications, and choose the appropriate topologies/architectures for each building block.
2. Efficiently size and bias an analog design for optimal, robust performance with Gm/ID methodology.
3. Manually layout analog circuits using best practices to mitigate systematic mismatch and layout-dependent effects.
4. Apply design strategies to minimize performance degradation from process-voltage-temperature variations.
5. Effectively scope and partition design construction, global place-and-route, and verification of hardware designs as part of a team effort.
6. Perform integration of various building blocks, peripheral circuits and I/O devices into a DRC, LVS clean GDS-II file as part of a team effort.
7. Understand and appreciate the logistics and procedures of an end-to-end tape out flow in context of analog circuit.

Prerequisites

For undergrad session: ECE3400 with a grade "B" or above is the sole prerequisite, though students may find this course easier if they have taken ECE4430. Students should be comfortable (or be willing to put in additional time and effort to be familiar) with basic command-line Linux usage. Basic familiarity with the SPICE simulator will be leveraged.

For graduate session, instructor permission is required to enroll.

Course Materials

Class Webpage
Canvas (https://canvas.gatech.edu/) is the primary means of distributing new information. **Homework assignments will be posted on Canvas and will not be handed out in class.** The following information will also be found on Canvas as it becomes available: (1) homework solutions, (2) tutorial materials, (3) class grades, (4) this syllabus, and (5) any supplementary materials relevant to this course.

On-Line Discussions
We will use **Piazza** (integrated in Canvas) to facilitate class discussions. We will try to check Piazza at least once a day. Please post questions about anything related to the course material, and also answer other students' questions, as long as you don't "give away the answer".

Textbooks
No textbook is required for this course. The instructor will rely on openly available reading-material that will be put together and made available on canvas.

Workload and Grading

Grading
Students in this course will be graded based on 4 components:

- Five 10-minute quizzes given between week 2 and week 12 in the class. The best four quizzes will be considered toward the final grade (15%)

- Homework assignments in the first half of the course (25%)

- Course participation, which may take one of several forms: (1) Involvement in lecture; (2) contributing the learning and design quality/productivity of the class on Piazza (the online communication medium for this class); (3) sharing scripts, methodologies, testbenches to improve outcomes for students. Lasting contributions to the course will be awarded bonus credit per the instructor's discretion. (10%)

- Final project work which includes design review presentations, design quality (correctness, robustness, performance, efficiency), final presentations and a test-chip bringup plan (50%)

The course is expected to be very strenuous. In accordance, grading policy is expected to be liberal. For instance, students with average performance in quizzes and homeworks and a fully functional, verified, robust final project should expect and "A" in this class.

Bonus credits will be offered on multiple occasions to incentivise students to adopt techniques/methodologies and develop valuable industry-relevant skills for improving design quality/productivity. Requiring them, however, constitutes too much effort for the number of credits awarded. Bonus credit will be awarded to provide a potential grade jump to students after initial bell-curve based grade-assignment.

Undergrad and grad session will be mainly differentiated through the efforts in the tapeout project. In this course, the project teams will be pre-formed to balance out the expertise such that each group's chance of success can be maximized. **Grad students will be assigned extra milestones, such as serving as chip**

captains. For this reason, we require grad students taking the course to have higher technical readiness. A screening and selection process are thus required for grad students before they are permitted to enroll. Undergrad students and grad students will be graded separately.

Homework

Students will find that homework is not limited to reinforcing the theory taught during lectures, as is typical of most courses. Instead homework will cover material which requires an understanding of some of the theory covered in class, but include additional components intended for hands-on learning. IC design is a practitioner's art. Consequently, homework is not solely designed to facilitate mastering VLSI theory. Instead, homework is built to complement the theory taught in class to allow students to build hands-on techniques that are difficult to teach in a classroom setting. To complete these homework assignments, students will synthesize their (1) understanding of the theory covered in class together with; (2) an ability to look through provided design and tooling documentation together with (3) skills they will develop to effectively manage multiple designs, files, and tools to produce robust, functional designs. The homework assignments in this class are staged to grow in scale and complexity to ramp student-teams up to project completion.

Each of you is expected to turn in homework that is completely your own work, but you are encouraged to discuss problems and solution approaches with others. You will be graded primarily on the method of your solution. The actual numerical answer accounts for only a small portion of the problem score. Organize your problem solutions in a logical step-by-step fashion to get the maximum number of points. I expect you to do your best professional looking work on your homework. POINTS WILL BE REDUCED FOR SLOPPY WORK. The easier it is to understand and follow the logic of your solution the more points you will receive. Be sure to put your name, date, section, and the assignment number on the front page or on a cover sheet.

As students in this course will hopefully eventually appreciate, homeworks constitute key checkpoints that contribute toward the timely construction of a quality design that will eventually be successfully tested. Maintaining a regular cadence toward project completion is critical. Submitting a late homework steals time from the next milestone, making it harder to meet, and so on until the executing the final project becomes un-viable. To actively avoid such a situation, late homeworks will be aggressively penalized with the intent of avoiding your project spiraling out of control, and not serving as a punitive grade-discrimination mechanism.

Quizzes

The quizzes are open-book. In the case of an excused absence from more than two quizzes, the final course grade will be based on the homework and the remaining quizzes scores. Unexcused absence from any quizzes will result in a grade of zero for that quiz. Note that excused absence will be made only in extreme circumstances (e.g., serious illness). Requests for excused absence should be made in writing and must be supported by appropriate documentation.

Course Expectations & Guidelines

Getting Help

The material in this course builds on earlier material, so it is very important to not get behind. Be sure to take advantage of office hours and other resources that are available. If you can't make office hours, email questions or arrange for an appointment.

Major Emergencies

If you have some sort of major life emergency – serious illness or injury, death in the family, house burns down or is flooded, etc. – that seriously impedes your progress in the class, please let us know as soon as possible so we can work something out. You will find professors can be quite reasonable if you keep us in the loop. Absence reporting procedures can be found in http://www.catalog.gatech.edu/rules/4/

On Things That Distract

Please silence all cell phones, tablets, pagers, etc. before entering class. If you forget to do so and receive a call, please shut the noisemaking device down as quickly as possible, and return the person's call *after* class. (Of course, there are reasonable exceptions for emergencies; in such cases leave your phone on vibrate, and answer it as quickly as possible and immediately step out of the room to handle the call.)

In general, please do not text, instant message, web surf, Facebook, tweet, e-mail, play games, etc. during class. It can be quite distracting. **Unless needed for class, the preferred position for laptops and tablets during class is in your backpack.**

Honor Code (http://www.policylibrary.gatech.edu/student-affairs/academic-honor-code)

Adherence to the Georgia Tech Honor Code is expected and all suspected instances of academic misconduct will be reported to the Dean of Students. It is your responsibility to ask for clarification if collaboration guidelines, test-taking policies, etc. are not clear.

Office of Disability Services (https://disabilityservices.gatech.edu/)

If you are a student registered with the Office of Disability Services (ODS), please make sure the appropriate forms and paperwork are completed by Prof. Li. We will abide by all accommodations required by ODS. It is the responsibility of the student to properly arrange test accommodations for each exam with ODS in sufficient time to guarantee space for exam administration. ALL exam accommodations must be handled through ODS. If the student does not register accommodations with ODS for the taking of an exam, then they will have to take the exam at the normally scheduled times without any additional accommodation unless the instructor is given specific directive from ODS on the student's behalf due to a mitigating circumstance.

Student-Faculty Expectations Agreement

It is important to strive for an atmosphere of mutual respect and responsibility between faculty members and students. In the end, a respect for knowledge and understanding, an appreciation for hard work, and respectful interactions all contribute to an environment conducive to learning and excellence. I encourage you to remain committed to the ideals of Georgia Tech while in this class. See www.catalog.gatech.edu/rules/22 for a description of some basic expectations that we can have of each other.

Analog VLSI I: From Theory to Tapeout Tentative Course Schedule (Sp2024)			
Class Date	**Lecture**	**Topic**	**Project Roadmap**
1/9	1	CMOS Modeling Recap	Tutorial 1: gm/ID
1/11	2	Gm/ID Method Part 1	
1/16	3	Gm/ID Method Part 2	Assignment 1
1/18	4	ADC High-Level	
1/23	5	Sample-and-Hold	Tutorial 2: SC Amp
1/25	6	Switched-Cap Amplifier Part 1	
1/30	7	Switched-Cap Amplifier Part 2	Assignment 2
2/1	8	OTA Design Flow	
2/6	9	Bias and CMFB	Tutorial 3: Layout, DRC, LVS
2/8	10	Introduction to Layout	
2/13	11	Design Rule and DFM	Assignment 3
2/15	12	LDEs and Layout Practices*	
2/20	13	SAR ADC Architecture	Tutorial 4: PEX
2/22	14	SAR Logic and DAC Switch	Assignment 4
2/27	15	Comparator Design	Tutorial 5: ADC Sim.
2/29	16	Parasitic Effects and Non-Idealities Modeling	Assignment 5
3/5	17	Non-Ideality Calibration	Tapeout milestone1
3/7	18	Common Design Mistakes*	
3/12	19	Global Floor-planning	
3/14	20	Guard Rings, Power and De-caps	Tapeout milestone 2
3/19	No Class	Spring Break	
3/21			
3/26	21	Monte-Carlo and PVT Corners	
3/28	22	Post-Layout Extraction and Sim.	
4/2	23	Design for Testability*	Tapeout milestone 3
4/4	24	Design Review	
4/9	25	Design Review	
4/11	26	Design Review	
4/16	27	Top-Level Integration	Tapeout milestone 4
4/18	28	Slack	
4/23	29	Slack	
5/2		Tapeout	

*Potential guest lectures by TI engineers

ECE 4804/8804 AVS Analog VLSI I: from Theory to Tapeout

Quick Introduction

Sponsored by Texas Instruments

Highlights

- A comprehensive end-to-end analog IC design training experience with industry sponsored resources
  - Focus on not just the core circuits, but also the things that make a working chip
  - Emphasize on theories and techniques for reliable design
  - Industry-standard workflow, toolchain and real PDK
  - Guest lectures from industry gurus

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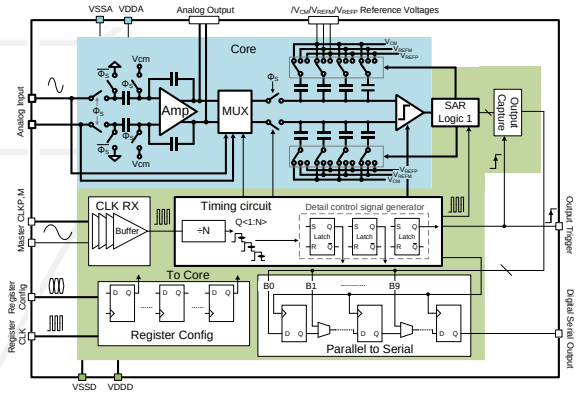
A Journey to Build and Bring Up Your Own ADC

Ramp Up
Tutorials & Assignments

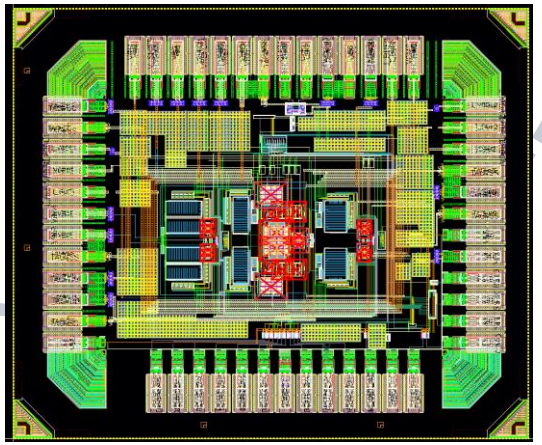


Milestone 1
Full Transistor-Level Schematic

Milestone 2
Global Floor Planning

Milestone 3
Block-Level Layout

Milestone 4
Full Chip Integration



Part 2: Measurement and Application

Fall 2024

Sign Off and Tapeout

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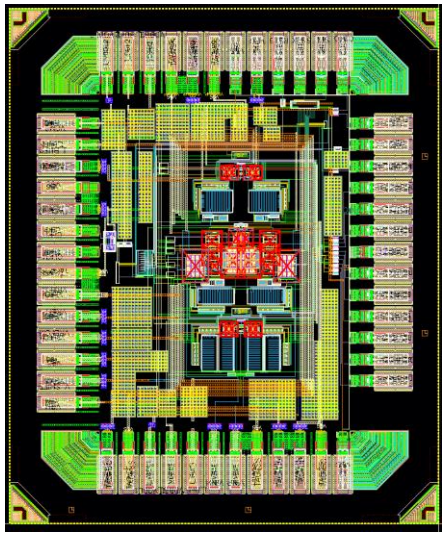
A Venue for Fostering Teamwork

Chip Captain：
Block A Design
Debug Planning
Chip Integration



Member 2
Block B Design
Layout
Documentation

Member 3
Block C Design
Layout
Documentation

Member 4
Block D Design
Layout
Documentation

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Key Topics

- Gm/ID Design Methodology
- Sample-and-hold circuits
- Successive Approximation ADC
- Layout Strategies
- Non-ideality and PVT Variation Management
- Design for testability

Important Notes for Graduate Students

- **8804 AVS** has a limited quota of 10. Enrollees will take on the role of chip captain to lead their team. 8804 students are thus required higher preparation, and will be graded by tougher milestones and rubrics. Students need to pass an application process to register for 8804.

- **4804 AVS** can be considered as an alternative for those that are less prepared, and it does not have an application process (you still have to register on your own) and the rubrics are slightly relaxed. It can be counted as an elective course for graduate students.

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FAQs

- Can I only take one part of the course?
  - Unfortunately, you have to take both parts (tapeout and measurement) in order to receive the final grade. Therefore, it is a two-semester commitment. If you are graduating in Spring 2024, this course might not be ideal for you.
  - If you are in the BS/MS program and plan to get the BS in Spring 2024, it is perfectly fine to take part 2 as MS student in Fall 2024.

- I have not taken the pre-requisite ECE 3400 at Georgia Tech. Can I still take the course?
  - For undergrade students, ECE 3400 is a must, or you don’t have the necessary background
  - For grad student, you can take 8804 when you pass the screen, or take 4804 after consulting with the instructor

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FAQs

- When will I know if I am accepted to take 8804
  - We will review the application as fast as we can and will notify the result before new year.
- When should I fill out the 8804 application form?
  - Please do so by Dec 15.
- When will we get the chip back?
  - The chips will be back before Fall 2024 for measurement. Since the chip is property of GT and TI, you cannot take it home though.

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How to Succeed in This Course?

- Dedication
  - Willing to spare considerable amount of time outside lecture hours to work on the project and self-study
  - The workload is nothing less than a capstone design
- Proactive and Corporative
  - Never freeride! The more you engage in teamwork the more you learn
  - Share your experience with the class
- Patience
  - You could be overwhelmed by circuit bugs and stringent schedule. Just be perseverant and patient. A composed mind will be your best friend

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Feel Free to Direct Any Questions to

- Instructor: Prof. Shaolan Li
- Email: shaolan.li@ece.gatech.edu

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