High efficiency screen-printed solar cells on textured mono-crystalline silicon

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Abstract

In this paper we report on high efficiency screen-printed 4 cm^2 solar cells fabricated on randomly textured float zone, magnetic Czochralski (MCz) and Ga-doped Cz silicon. A simple process involving $POCl_3$ emitters, low frequency PECVD silicon nitride deposition, Al back contact print, Ag front grid print followed by co-firing of the contacts produced efficiencies of 19.0% on textured float zone, 18.2% on MCz and 17.7% on Ga-doped Cz. A combination of high sheet resistance emitter (~100 Ω-/sq.) and the surface texturing resulted in short circuit current density of 37.3 mA/cm^2 for 0.6 Ω-cm float zone cell, 38.2 mA/cm^2 for 4.8 Ω-cm MCz cell and 37.4 mA/cm^2 for 1.5 Ω-cm Ga-doped Cz cell. Open circuit voltages were consistent with the base resistivity of the three materials. However, FF was highest for float zone (0.784) followed by MCz (0.759) and Ga-doped Cz (0.754). Model calculations performed using PC1D showed that, once the lifetime exceeds 200 μs for this cell design, the efficiency no longer has a strong dependence on the bulk lifetime. Instead, the performance is limited by the cell design including contacts, base resistivity, doping profiles, and front and back surface recombination velocities. Detailed analysis is performed to explain the high performance of these screen-printed cells and guidelines are provided for ≥20% efficient screen-printed cells.

Keywords: High efficiency silicon, textured, screen-printed, high sheet resistance emitter.

1. Introduction

The cost of photovoltaic (PV) needs to decrease by a factor of two to four within the next two decades for PV to become an attractive solution to the problems of fossil fuel depletion and growing energy demand. Crystalline Si has been the champion of PV industry, which has grown in excess of 30% per year in recent years. In the face of stiff competition from other materials, crystalline Si has shown uncanny ability to reinvent itself when challenged. Cost and technology roadmaps in this paper reveal that 18-20% efficient cells fabricated on 100-200 μm thick wafers using a low-cost technology like screen-printing can reduce the direct manufacturing cost below $1/Wp for a 500 MWp production capacity. This paper also reports on the development of 18-20% efficient cells on monocrystalline Si using the screen-printing technology. Three kinds of monocrystalline silicon wafers are used in this study: 0.6 Ω-cm float zone Si, 4.8 Ω-cm magnetic Czochralski (MCZ) silicon and 1.5 Ω-cm Ga-doped silicon. In the literature, greater than 20% efficient cells have been achieved on FZ [1], MCZ [1] and CZ [2] Si using photolithography contacts and multiple heat treatments and masking steps. In addition, it is well known that 1-2 Ω-cm high-oxygen CZ suffers from light induced degradation (LID) due to the formation of boron-oxygen complexes. This phenomenon can reduce the CZ cell efficiency by 0.5-1% absolute. Therefore we also investigated MCZ and Ga-doped CZ in this paper. Use of Ga as a dopant (instead of boron) and low oxygen (≤ 5 ppm) high resistivity (4.8 Ω-cm) MCZ can eliminate or significantly reduce the LID caused by the presence of boron and oxygen simultaneously. This paper shows an effort to bring the screen-printed cell efficiencies in the range 18-20% on monocrystalline Si. Guidelines are provided for achieving ≥20% screen-printed cells on all three materials through computer modeling and understanding of loss mechanisms.

2. Cost and Technology Roadmaps

We have established guidelines and requirements to reduce the direct manufacturing cost below $1/W by simulating a crystalline silicon manufacturing line based on screen-printing technology. If we assume 13.5% efficient 325 μm thick cells, 25 MWp production capacity, wafer, cell and modules yields of 92, 95 and 98%, and a low-cost Si with bulk lifetime of ~10 μs, we obtain direct manufacturing cost of ~$2/W. This is close to the current situation of most commercial Si cells. However, model calculations also show that if the cell thickness can be reduced to 100-200 μm, efficiency can be raised to 20% and production capacity can be increased to 500 MWp, then the direct manufacturing cost could fall below $1/W, giving a reasonable return on investment for a module sale price of ~$1/W. Silicon cell production capacities are already approaching 500 MW today with no technological barrier to go above that. In addition, 100-200 μm thick wafers can be sliced today. Therefore the main challenge is to raise the commercial cell efficiencies close to 20% using a low-cost technology like screen-printing.

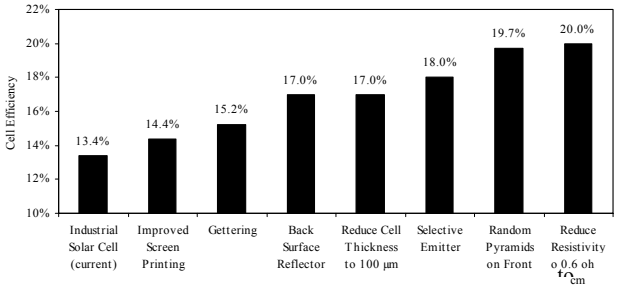

Figure 1 Technology roadmap to achieve 20%-efficient solar cells using a combination of manufacturable technologies.

Figure 1 shows a technology roadmap for raising the efficiency of screen-printed cells from 13.5% to 20%. According to this roadmap, if the screen-print technology can be improved to raise the average fill factor from 0.740 to 0.780 and lower the shading loss from 8% to ~5%, then the efficiency can increase from 13.5% to 14.4%. If the bulk lifetime can be increased to ≥100 μs (which is generally not a problem for monocrystalline silicon) then 15.2% efficient cells can be achieved. Now if the

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back contact technology can be improved to provide back surface recombination velocity (BSRV) of 100 cm/s in conjunction with 95% back surface reflector (BSR), then the efficiency can rise up to 17%. At this point, wafer thickness can be reduced from 325 µm to 100-200 µm, without any loss in efficiency. However, the cell performance gets limited by the emitter saturation current density, therefore increasing the emitter sheet resistance from 45 to 100 Ω/sq. can raise the efficiency to 18.0%. If the material can be textured (not a problem for <100> monocrystalline silicon) then 19.7% efficiency can be realized. If the above modifications can be achieved on 0.6 Ω-cm silicon, then the screen-printed cell efficiency can reach 20%.

3. Device Fabrication

Using the above guidelines, we first fabricated cells on 0.6 Ω-cm textured <100> FZ silicon. Cell thickness was kept at around 300 µm because manufacturable low-cost screen-printing technology is not yet fully developed for the back contact, which can give BSRV of ≤100 cm/s in conjunction with BSR of ≥95%. Without such a rear contact, thinning the wafer down to 100 µm may lead to appreciable reduction in cell efficiency. In addition to the FZ Si, we included 4.8 Ω-cm low oxygen MCZ and 1.5 Ω-cm Ga-doped CZ to investigate cheaper alternatives to FZ silicon that can give high efficiency and also avoid the light induced degradation. Cell fabrication involved chemical texturing the monocrystalline Si wafers on both sides followed by a clean in 1:1:2 H_2SO_4:H_2O_2:H_2O for 5 minutes and rinse in de-ionized water for 3 min. Next the wafers were dipped in 10% HF for 2 minutes, followed by a 30 second rinse in DI water. The wafers were loaded in the diffusion furnace for the n^+ emitter formation. A diffusion temperature of 843°C was used to achieve the 100-Ω/□ emitters. A 50 kHz PECVD SiNx AR coating was then deposited on the emitters. Next, an Al paste was screen-printed on the backside and dried at 200°C. The Ag grid was then screen-printed on top of the SiNx film, dried at 200°C and then the Ag and Al contacts were co-fired in a lamp-heated three-zone infrared belt furnace. The cells were edge isolated before forming gas anneal for 18 minutes and characterized by light I-V as well as the internal quantum efficiency (IQE) measurements.

4. Results and Discussions

Figure 2 shows the I-V data for the best cell achieved on 0.6 Ω-cm float zone silicon. This was tested and verified by NREL and also represents the highest efficiency fully screen-printed cell to date. Figure 3 shows the efficiency of the nine 4 cm^2 cells made on the 4-inch diameter FZ wafers. The 19.0% efficient cell was characterized and modeled to identify the loss mechanisms responsible for the difference between the 20% efficient cell on the technology roadmap (Figure 1) and the 19% efficient cell achieved in this study. Table 1 shows the results of modeling and characterization of the 19.0% efficient cell where number of measured and extracted input parameters are listed along with the modeled cell efficiency. Front surface recombination velocity (FSRV) of 60,000 cm/s and back surface recombination velocity (BSRV) of 600 cm/s were extracted by matching the measured IQE with the simulated IQE in the short and long wavelength range using the PC1D simulation program and the measured emitter doping profile, base thickness, base doping and bulk lifetime. The bulk lifetime was found to be ~250 µs by the photo-conductance decay (PCD) technique, after etching the cell down to bare Si. The junction leakage current (J_{o2}) of 2 nA/cm^2 and second diode ideality factor (n_2) of 1.65 was determined by Suns-V_{oc} technique. The back surface reflectance (BSR) was found to be 61.5% using the extended spectral analysis of the cell IQE [3]. With all the above input parameters, the PC1D model predicted a cell efficiency of 19.0% with V_{oc} of 640 mV, J_{sc} of 37.3 mA/cm^2 and a FF of 0.796 which agreed fairly well with the measured values of 643 mV, J_{sc} of 37.8 mA/cm^2, FF of 0.781, and efficiency of 19.0%. Figure 5 also shows a good match between the measured and simulated IQE over the entire range. From this analysis it is clear that the 19.0% cell fell short in the BSRV and BSR values required for 20% efficiency. This is also shown by the modeling curves in Figure 6, which indicate that by reducing the BSRV to 100 cm/s, increasing the BSR to 95% and reducing the thickness to 100 µm, screen-printed solar cells of ~20% can be achieved on FZ silicon. We are in the process of improving the rear contact by depositing an appropriate dielectric on the back surface, opening the contact windows through the dielectric by a screen-printing etching paste, depositing screen-printed Al on the entire back and then firing the contacts. This approach has been recently attempted by IMEC [4].

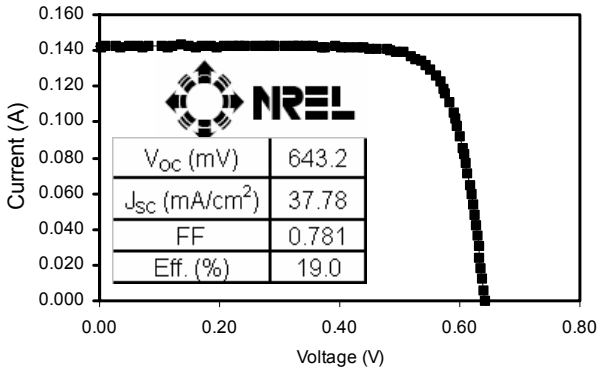

Figure 2 I-V measurements by NREL for the 19% textured front and back 100 Ω/sq emitter cell on 0.6 Ω-cm FZ Si.

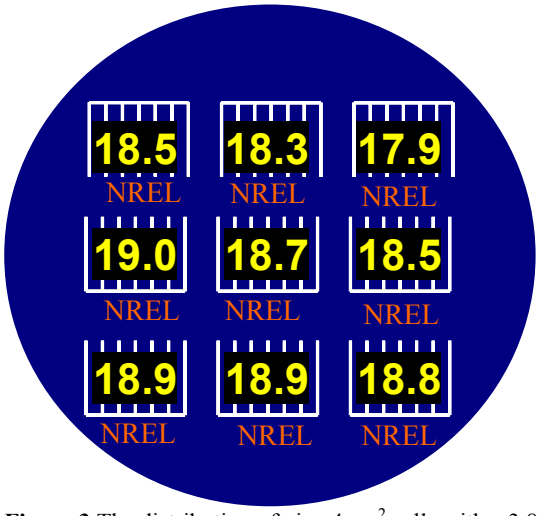

Figure 3 The distribution of nine 4 cm^2 cells with a 3.8 cm^2 mask on a 4 inch 0.6 Ω-cm FZ wafer textured on both sides.

Detailed analysis of emitter saturation current density also revealed that in the 19.0% cell, J_{oe} is 267 fA/cm^2 and J_{ob} is 166 fA/cm^2. Furthermore, J_{oe} is composed of J_{oe} contribution of 157 fA/cm^2 from the metal grid and 110 fA/cm^2 from the SiN in between the grid line. This suggests that by reducing the grid coverage or improving the front passivation cell efficiencies can by increased close to 21% (Fig.5).

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Table II shows the I-V data for the textured screen-printed MCZ and Ga-doped CZ cells made with 100 Ω/sq. emitter using the same technology as the float zone Si cells. MCZ Si gave 18.2% efficiency while the Ga-doped CZ gave an efficiency of 17.7%. The difference in efficiency between the three-monocrystalline Si cells is largely reflected in the difference in V_{oc} and fill factor. Table III shows the measured and modeled cell parameters to explain the lower efficiency of the MCZ and Cz cells relative to the FZ. High resistivity MCZ cell had higher series resistance, which lowered the fill factor. In spite of higher lifetime (506 µs) in the MCZ, its V_{oc} was lower than FZ because of the higher resistivity and higher base saturation current density (J_{ob}). Higher bulk lifetime did give higher J_{sc} for MCZ cell but it could not compensate for the V_{oc} and FF loss.

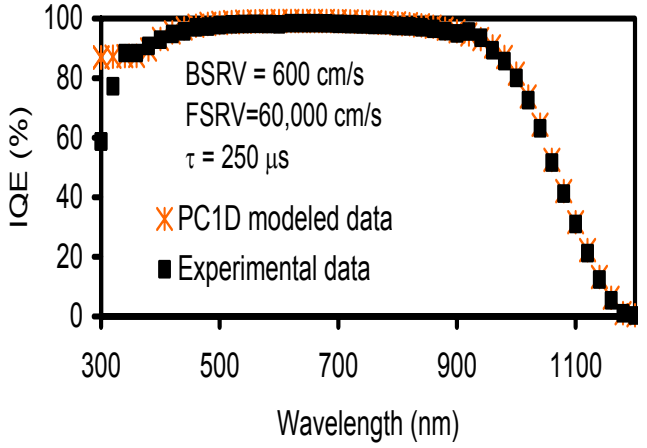

Figure 4: Measured and simulated IQE over the entire wavelength for the 19.0% FZ Si cell.

Table I Modeling parameters for the 19.0% textured 100 Ω/sq FZ cell

Cell Parameters	FZ Cell
Base Resistivity (Ω-cm)	0.6
R_s (Ω-cm^2)	0.79
R_{sh} (Ω-cm^2)	68,157
n_2	1.65
J_{o2} (nA/cm^2)	2
Emitter sheet resistance (Ω/sq)	100
Surface concentration (cm^3)	1.5x10^{20}
Texture angle (degrees)	54.7
Texture depth (µm)	3
τ_{bulk} (µs)	250
BSRV (cm/s)	600
R_{back} (%)	61.5
FSRV	60,000
Grid shading	~4-4.5%
Modeled V_{oc} (mV)	640.3
Modeled J_{sc} (mA/cm^2)	37.3
Modeled FF (%)	79.6
Modeled Efficiency (%)	19.0

Table IV shows a set of model parameters that can drive this MCZ efficiency to 20%. Table IV indicates that we need to improve the front contacts to lower the FSRV to 40,000 cm/s, reduce shading losses to 4.5%, and lower the series resistance to 0.6 Ω-cm^2. This can be achieved by reducing the front grid coverage and optimizing the Ag paste and firing conditions. We also need to lower the BSRV from 200 to 100 cm/s by using a dielectric rear passivation.

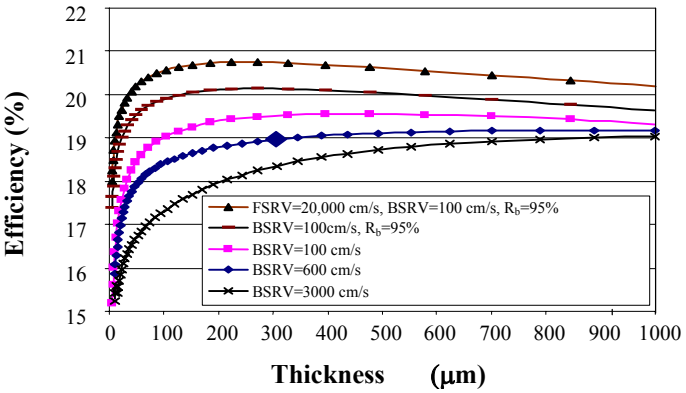

Figure 5: Simulated curves of screen-printed solar cell efficiency plotted as a function of (a) base thickness and BSRV.

Table II Electrical output performance of screen-printed monocrystalline silicon solar cells.

Material	Resistivity (Ω-cm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
Ga-doped CZ	1.5	627	37.4	75.4	17.7
MCZ	4.8	628	38.2	75.7	18.2

Table III PC1D modeled parameters

Material	BSRV (cm/s)	FSRV (cm/s)	BSR (%)	R_s (Ω-cm^2)	R_{sh} (Ω-cm^2)
Ga-doped CZ	950	60000	61.5	1.035	26656
MCZ	200	60000	66	0.926	68299
B-doped Float Zone	600	60000	61.5	0.79	68157

Table IV Modeling parameters for 20% SP cells on MCZ silicon

Cell Parameters	MCZ Cell
Base Resistivity (Ω-cm)	4.75
R_s (Ω-cm^2)	0.600
R_{sh} (Ω-cm^2)	68299
n_2	2.0
J_{o2} (nA/cm^2)	15
Emitter sheet resistance (Ω/sq)	100
Surface concentration (cm^3)	1.5x10^{20}
Texture angle (degrees)	54.7
Texture depth (µm)	3
τ_{bulk} (µs)	506
BSRV (cm/s)	100
R_{back} (%)	66
FSRV	40,000
Grid shading	4.5%
Modeled V_{oc} (mV)	639.4
Modeled J_{sc} (mA/cm^2)	39.7
Modeled FF (%)	78.8
Modeled Efficiency (%)	20

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Ga-doped CZ gave a screen-printed cell efficiency of 17.7%, largely due to very high BSRV of 950 cm/s compared to 600 cm/s for the lower resistivity float zone Si. We have frequently noticed this phenomenon and attribute this to the higher oxygen concentration in CZ, which may introduce recombination centers at or near the p-p^+ interface to raise the BSRV. Dielectric rear passivation may be able to eliminate this loss mechanism in CZ. Then improving the front contacts to lower the FSRV and FF can bring the CZ cell efficiency also close to 20% (Figure 6). Finally, all the three cells were light soaked under 1 sun illumination for 24 hours and showed no light induced degradation at all. Thus all the three-monocrystalline Si materials have the potential to reach 20% SP cell efficiency with no LID.

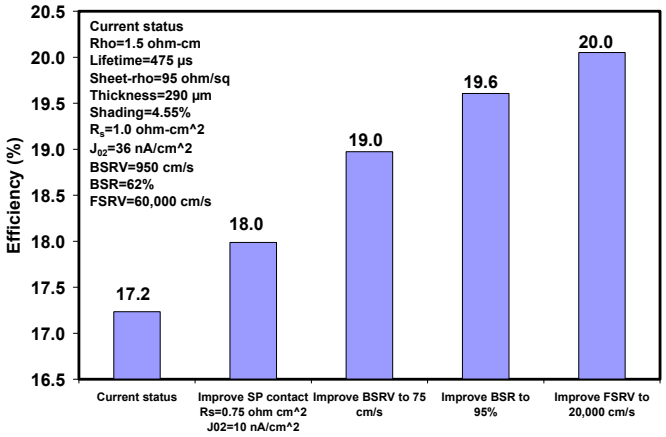

Figure 6 Roadmap for achieving 20% efficiency on CZ silicon.

5. Conclusions

Screen-printed 4 cm2 cell efficiencies of 19.0%, 18.2% and 17.7 were ahieved on FZ, MCZ, and Ga-doped CZ silicon, respectively. A technology roadmap is developed to achieve ≥20% efficient 100 µm thick monocrystalline Si cells. Detailed analysis of 19.0% efficient FZ cell indicate that we need to improve the rear contact technology to improve the BSRV from 600 cm/s to 100 cm/s and BSR from ~62% to 95% in order to raise the 19% efficiency beyond 20%. This can be achieved by dielectric passivation of the rear surface. Open circuit voltage and performance of 19% efficient FZ cell is also limited by Joe, therefore, reducing the grid coverage or improving the front surface passivation, in addition to BSRV and BSR, can improve the efficiency to about 21%.

High resistivity MCZ cell efficiency was lower because of high series resistance, low fill factor and higher BSRV and FSRV. Thus improving the front and back contacts by introducing dielectric rear passivation and optimized paste and firing conditions can push the MCZ efficiency to ~20%.

Ga-doped CZ showed much higher BSRV. Higher oxygen content is suspected to account for this effect. Thus incorporation of dielectric passivation instead of full Al BSF, along with improved front contacts and FF can bring the Ga-doped CZ cell efficiency close to 20%. Finally no LID was observed in all the three high efficiency screen-printed monocrystalline silicon cells.

6. REFERENCES

[1] J. Zhao, A. Wang and M. Green "24.5% Efficiency silicon PERT Cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates" Progress in Photovoltaics: Research and Applications; 7, (1999), 471-474.

[2] J. Knowbloch, S. Glunz, D. Biro, W. Warta, E. Schaffer and W.Wettling, "Solar Cells with efficiencies above 21% processed from Czochralski grown silicon" Proc. of the 25th IEEE Photovoltaic Specialists Conf. 1995: 405-408.

[3] P.A. Basore and D.A. Clugston, "PC1D Version 4 for Windows: from Analysis to Design," in *Proceedings of the 25th IEEE Photovoltaic Specialists Conf*erence, Washington, D.C., May 13-17, 1996, pp. 449-452.

[4] G. Agostinelli, J. Szlufcick, P. Choulat and G. Beaucarne "Local contact structures for industrial PERC-type solar cells" in Proceedings, 20th European PVSEC, Barcelona, Spain, 2005.

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