

UNDERSTANDING THE ROLE OF FORMING GAS ON THE SCREEN-PRINTED CRYSTALLINE SILICON SOLAR CELL FRONT GRID

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ABSTRACT: In this paper we report on the role of forming gas anneal on the fill factor of a small area cell and efficiency loss due to scaling the cell area. Solar cells that are under-fired and those fired at the optimum peak firing cycle showed very marginal response to forming gas anneal. Forming gas anneal is most effective for over-fired cells. The high temperature for the over-fired cells is believed to enhance Ag crystallites growth and the formation of a thick glass layer between the Ag front grid and silicon material. The forming gas anneal aids in reducing the glass to its metal, increase the conductivity of the glass and decrease the contact resistance. Solar cells with four different areas (4-cm², 49-cm², 100-cm² and 156-cm²) that were fired at the optimized peak firing temperature showed excellent fill factors without the forming gas anneal treatment. The fill factor was not a strong function of the area even though individually the n-factor and series resistance varied due to edge recombination. The efficiency and short circuit current density showed a quadratic relation with the cell area. The short circuit current density showed a difference of 3.2 mA/cm² between the 4-cm² and 156-cm² cells. The short circuit current density decreased with area due to shading, diffusion length and back surface recombination velocity or L_{eff} , front surface recombination velocity, and area loss due to edge isolation. Improved understanding of these effects coupled with grid design and process optimization can bridge the gap between the small and large area cells.

Keywords: screen-printed, solar cell, multi-crystalline, HEM, FGA, large area solar cells

1. INTRODUCTION

The primary loss mechanisms associated with screen-printed metallization are grid line resistance, contact resistance, and junction leakage and shunting. The grid line resistivity and the contact resistance depend on the contact firing cycle, the Ag paste and emitter surface concentration. The Ag paste in turn depends on the silver particle size, the amount and nature of glass frit and its transition temperature, as well as the type and level of additives and dopants. The silver particle size controls the nature and amount of Ag crystallites formed during the firing process. The amount of glass frit dictates the final glass thickness at the interface between silicon and silver grid, which controls the contact resistance. The nature (mild or aggressive) of the frit and glass transition temperature determines the optimum peak firing temperature. Therefore, the choice of Ag paste based on these key parameters can facilitate optimization of the firing cycle. However, without the adequate characterization and understanding of the Ag paste and proper monitoring of the wafer temperature, the cells can either be over or under fired. This paper shows that over fired cells due to non-optimum firing cycle usually require a forming gas anneal to reduce the contact resistance.

Hilali [1] used high resolution TEM to study the structure of the glass and Ag crystallites at the contact interface before and after forming gas anneal. It was concluded that the Ag crystallites precipitate from the glass layer into the Si emitter and the glass layer has mainly Pb and Bi detected by EDS after firing. Other elements like Ag, O, Si, and N were also present. Pb/Bi precipitates of ~5 nm size were observed before the forming gas anneal. It was noted that the metal precipitates were much smaller after the forming gas anneal. These metal precipitates were roughly 5 Å after undergoing ~10 times reduction in size due to FGA. This was attributed to the presence of hydrogen in the forming gas ambient because an anneal in nitrogen ambient

showed no reduction in the specific-contact resistance or enhancement in the fill factor [2]. Hydrogen anneal works probably because it can diffuse through the screen-printed contact and glass regions to act as a reducing agent for the metal oxides present in the glass layer [3].

In this study, we first investigated several Ag pastes for the front contact grid and optimized the firing cycle for large area (156-cm²) cast multi-crystalline Si cells with 45-Ω/ emitter. Next we fabricated and analyzed four different area solar cells; 4-cm², 49-cm², 100-cm² and 156-cm² as shown in Fig. 1. These cells were printed on 125 mm x 125 mm multi-crystalline silicon wafers and fired at the peak firing temperature optimized for large area cells.

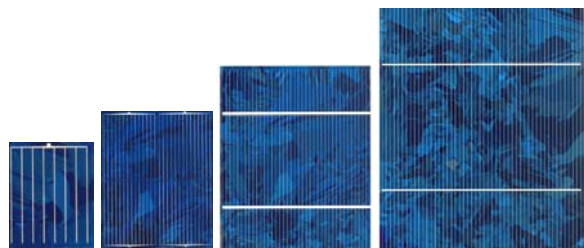


Figure 1: 4-cm², 49-cm², 100-cm² and 156-cm² cells fabricated on cast multi-crystalline silicon material.

2. EXPERIMENTAL

Cast multi-crystalline or HEM silicon wafers were etched in KOH solution for 3 minutes to remove saw damage and then cleaned in 1:1:2 H₂SO₄:H₂O₂:H₂O for 5 minutes, followed by a 3-min rinse in de-ionized (DI) water. This was followed by a clean in 1:1:2 HCl:H₂O₂:H₂O for 5 minutes and a 3-min rinse in DI water. A final dip in 10% HF for 2 minutes was performed, followed by a 30 second rinse in DI water. The emitters were formed in conventional tube furnace

using POCl_3 at a set temperature of 877°C , which resulted in a $45\text{-}\Omega/\text{square}$ emitter. The wafers designated for 156-cm^2 cells were edge isolated using a chemical method. This was followed by the phosphorus glass removal and DI water rinse before a single layer low frequency PECVD SiN anti-reflection coating was deposited on the front at 400°C . Next, the Al back contact was printed and dried at 200°C . This was followed by front Ag grid printing of each of the four areas and dried at 200°C . Next, the samples were co-fired in the IR belt furnace at a peak firing temperature optimized for the 156-cm^2 multicrystalline solar cells. The 4, 49 and 100-cm^2 solar cells were isolated using a dicing saw to define the active cell area. All cells were characterized by light current-voltage.

3. RESULTS AND DISCUSSION

3.1 Front Ag paste and firing cycle optimization

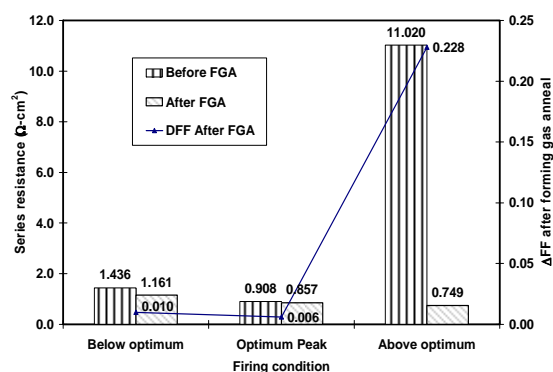


Figure 2: Effect of forming gas anneal on series resistance and fill factor of under-fired, optimum and over-fired solar cells.

The peak temperature of the wafer was monitored with thermocouple in conjunction with a Datapaque data logger. Based on the glass transition temperature for the Ag paste, three firing profiles were designed with temperatures varying by $\leq 30^\circ\text{C}$. After firing at each peak temperature the cells were tested and then subjected to a forming gas anneal. Fig. 2 is the summary of the results, showing the change in fill factors and series resistance, before and after forming gas anneal. Cells fired at 15°C below the optimum peak firing temperature showed a marginal change in both the fill factor (0.010) and series resistance after forming gas anneal. The poor response to forming gas treatment could be due to insufficient Ag crystallites to enhance carrier transport. Very small change was also observed in fill factor and series resistance for cells fired at the optimized peak firing temperature because the glass layer at Ag grid and silicon interface may be thin enough for sufficient carrier conduction through this interface. Cells fired at 15°C above the optimum temperature exhibited the most improvement in the fill factor. In this case, it is believed that the higher temperature causes formation of thick glass at the interface of Ag front grid and the silicon which leads to high series resistance. Therefore, the forming gas anneal aids in reducing the glass to its metal (e.g. PbO to Pb), which increases the conductivity of the

glass and decreases the contact resistance. This may also promote multi-step tunneling through the glass.

3.2 Characterization of four solar cells with different areas before forming gas anneal.

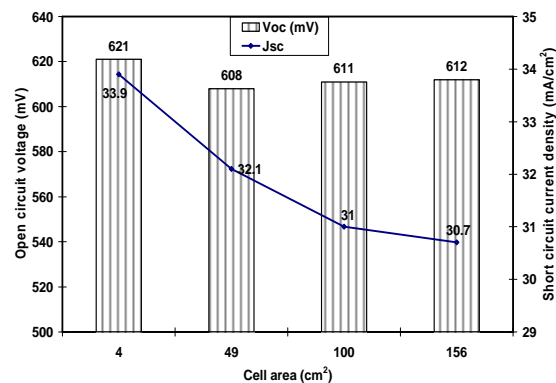


Figure 3: Effect of area on open circuit voltage and short circuit current density.

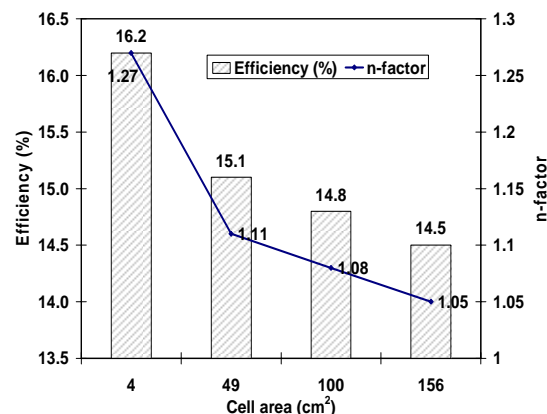


Figure 4: Effect of area on efficiency and n-factor of a silicon solar cell.

Figs. 2-4 show the open circuit voltage, short circuit current density, efficiency, ideality factor, fill factor and the series resistance as a function of area of a solar cell. The open circuit voltage does not show significant dependence on the cell area, although the 4-cm^2 cell gave the highest open circuit voltage. However, the short circuit current density varied strongly with the area; the 4-cm^2 cell produced the highest current. The short circuit current density showed a difference of $3.2\text{ mA}/\text{cm}^2$ between the 4-cm^2 and 156-cm^2 cells. The efficiency was also a strong function of the cell area; the 4-cm^2 cell gave the highest efficiency. The efficiency difference between the 4-cm^2 and 156-cm^2 was $\sim 1.7\%$ (Fig. 4) when no additional design or process optimization is done for area difference. It was noted that both short circuit current density and efficiency related quadratically with the cell area. The ideality factor decreased as the cell area increased but did not show any detrimental effect on the small area cell. Note that the high n-factor in the 4-cm^2 cell caused only a small reduction in fill factor. The fill factor did not show any dependence on the cell area.

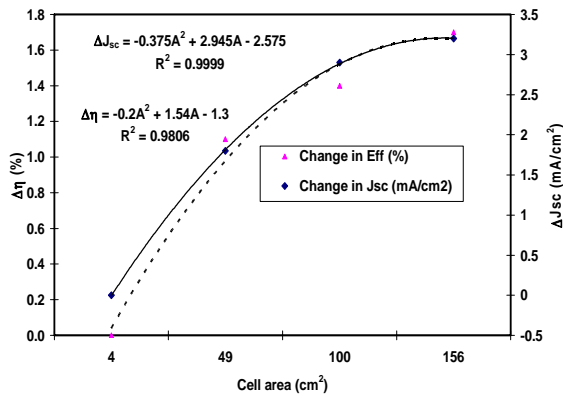


Figure 5: Effect of area on short circuit current density of solar cells fabricated on cast multi-crystalline silicon.

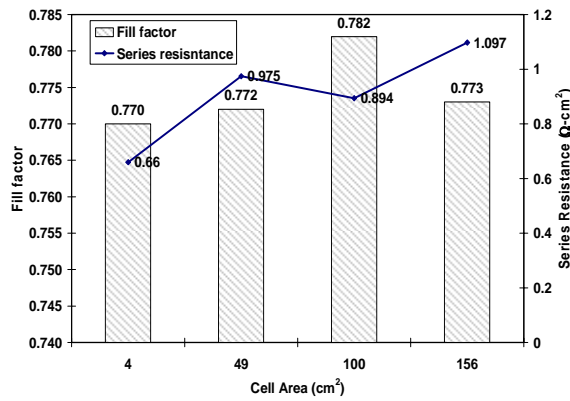


Figure 6: Effect of area on fill factor and series resistance of a silicon solar cell.

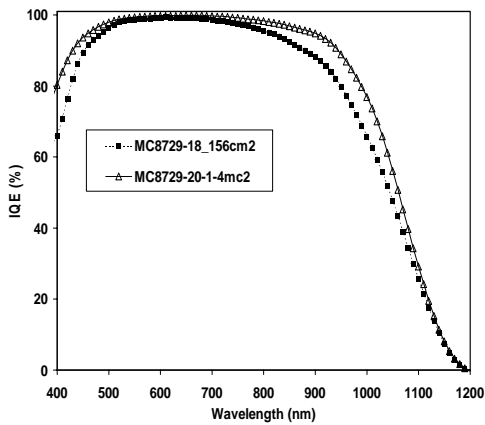


Figure 7: Internal quantum efficiency of 4-cm² and 156-cm² cells fabricated on multi-crystalline silicon wafer.

The short wavelength IQE measurements were slightly in favor of small area cells (Fig 7). Since the emitters were formed at the same time, this loss may be related to the difference in FSRV. The IQE analysis gave a loss of 0.78mA/cm² due to FSRV. LBIC analysis revealed that an inactive region with an area of about 3-cm² is formed at the edge of the cell. This inactive area is responsible for a loss in J_{sc} of 0.6 mA/cm². Measurements of grid shading showed no appreciable difference to account for the loss in J_{sc} of large area cells. Since the very long wavelength response (> 1.1μm) was

nearly identical, we can eliminate any loss due to BSR. Thus the remaining 1.6 mA/cm² loss in J_{sc} (3.2 -0.78-0.6-0-0) is attributed to the combined effect of diffusion length and BSRV or the L_{eff}. This effect may be partly due to the non-uniformity of cast mc-Si material which can get somewhat amplified when dealing with large area cells. More work is needed to understand the reasons for these losses in order to bridge the gap between the performance of small and large area mc-Si cells.

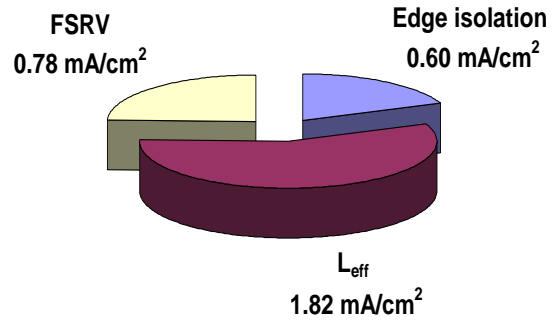


Figure 8: Components of the 3.2 mA/cm² ΔJ_{sc} between 4-cm² and 156-cm² solar cells fabricated on cast multi-crystalline silicon.

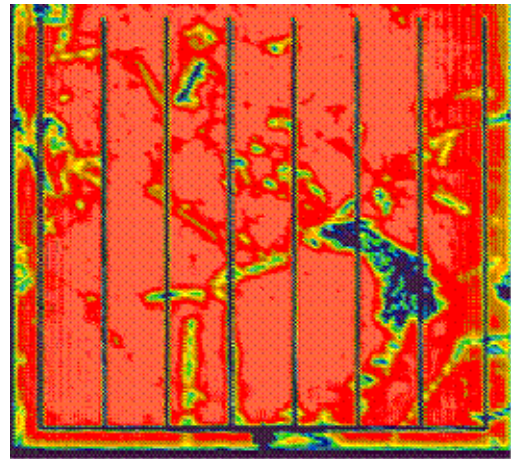


Figure 9a: LBIC scan for 4-cm² solar cells fabricated on cast multi-crystalline silicon.

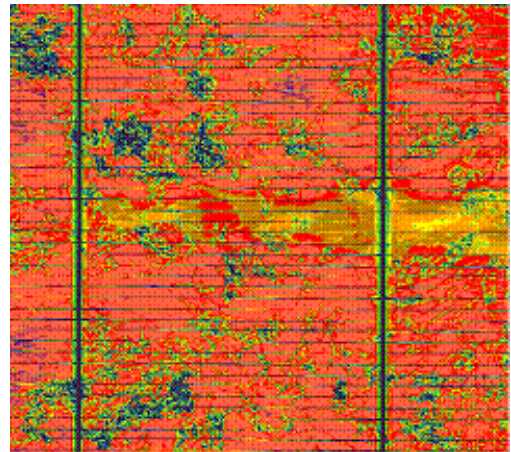


Figure 9b: LBIC scan for 156-cm² solar cells fabricated on cast multi-crystalline silicon.

Since the diffusion length and back surface recombination velocity or L_{eff} dominated the difference in short circuit current density between the 4-cm² and 156-cm² cells, an LBIC analysis was carried out to further elucidate the L_{eff} difference, Figs. 9a and 9b. The average response on both small and large area cells were the same ~ 0.52 A/W. It should be noted that only ~ 100 -cm² of the 156-cm² was scanned. More analysis will be carried out with these images in conjunction with the inhomogeneity model developed by Nakayashiki et al [4] to separate the effect of bad region in both cells.

3.3 Characterization of four solar cells with different areas after forming gas anneal

After forming gas anneal treatment, the open circuit voltage, short circuit current density, n-factor and the fill factor remained almost the same, irrespective of the area. This confirmed the observation made in section 3.1 for cells fired at the optimum peak firing temperature that did not respond significantly to forming gas anneal.

4. CONCLUSIONS

Forming gas anneal can raise the fill factor of an over-fired screen-printed multi-crystalline silicon cell from 0.585 to 0.766. The $\sim 30\%$ improvement in fill factor is mainly due to the series resistance reduction from 11.02 $\Omega\text{-cm}^2$ to below 1- $\Omega\text{-cm}^2$. The reduction in series resistance is attributed to FGA-induced reduction of metal oxides into metal in the glass layer in conjunction with over-firing induced high density of Ag crystallites at the Ag grid/silicon interface which enhances the conduction. When cells are under-fired or fired at the optimized peak firing temperature, there is very marginal improvement in the contact properties after the forming gas anneal. For the under-fired cells there are not enough Ag crystallites to promote conduction to enhance the FGA effect. For the cells fired at the optimized condition, series resistance is reasonably low to begin with due to large number of crystallites and thin glass layer, therefore we observe at most a small effect due to FGA anneal with series resistance decreasing by less than 20%.

Fill factor and V_{oc} were not appreciably affected by the area. However, the short circuit current density and the efficiency showed a quadratic relationship with the mc-Si cell area for the cell design and process used in this study. The short circuit current density showed a difference of 3.2 mA/cm² between the 4-cm² and 156-cm² cells. The difference in the short circuit current density was attributed to emitter recombination, diffusion length, back surface recombination velocity and loss of active area during edge isolation. The front surface recombination velocity contributed to a 0.78 mA/cm² loss in J_{sc} while edge isolation inactive area accounted for 0.60 mA/cm². The difference in the diffusion length and BSRV or L_{eff} accounted for about 1.82 mA/cm² loss in J_{sc} of these mc-Si cells. Exact reasons for these loss mechanisms are not yet fully understood. They are partly related to the non-uniformity of the cast mc-Si. Attempts are underway to bridge the gap between small area and large area cells through better understanding and process optimization of large area devices

4.1 Acknowledgements

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4.2 References

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