Silicon vs. Organic Interposer: PPA and Reliability Tradeoffs in Heterogeneous 2.5D Chiplet Integration

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***Abstract*—The optimal selection of an interposer substrate is important in 2.5D systems, because its physical, material and electrical characteristics govern the overall system performance, reliability and cost. Several materials have been proposed that offer various tradeoffs including silicon, organic, glass and etc. In this paper, we conduct a quantitative comparison between two 2.5D IC designs based on silicon vs. liquid crystal polymer (LCP) interposer technologies in the overall system level for the first time. We also investigate tradeoffs in power, performance and area (PPA), signal integrity (SI) and power integrity (PI) depending on the interposer technologies. Through our flow, we generate a large-scale benchmark architecture with commercial-grade GDS layouts of interposer and chiplets using two different interposer substrates. Then, we model transmission lines and power delivery network (PDN) of each 2.5D IC design. Finally, we perform PPA analysis, SI and PI on both 2.5D IC designs to observe the quantitative tradeoffs between two designs. Our experiment shows that silicon interposer-based design has 10.46% less power, 0.25× smaller area and 0.57× shorter average wirelength compared to LCP interposer-based design. However, LCP-based design has 0.59× smaller PDN DC impedance and 0.75× shorter worst delay of interposer wire while maintaining the power delivery efficiency. Lastly, our cost analysis of 2.5D IC design indicates that the overall cost of organic LCP technology, if both the chiplets and their interposer costs are combined, is 2.69× higher than the silicon even the cost of LCP interposer is 1.91% of silicon interposer. This indicates that LCP technology is prohibitive unless the interconnect and bump dimensions are dramatically reduced.**

***Index Terms*—2.5D IC, silicon interposer, liquid crystal polymer (LCP), tradeoff, PPA, signal and power integrity.**

I. Introduction

Interposer technology has gained a lot of traction lately as the leading contender for heterogeneous component integration. Fig. 1 shows the vertical stack-up of an interposer-based 2.5D IC design. This technology enables not only the reuse of existing IP blocks, but also the heterogeneous integration using a proper technology choice for each chiplet. This approach significantly reduces the design time and design complexity by re-utilizing pre-designed chiplets as plug-and-play modules. Intel's recent FOVEROS technology and AMD's Zen 2 micro-architecture indicate that the 2.5D IC technology is no longer an alternative to the traditional 2D ICs, but a new trend in SoC design.

There exist various kinds of interposer substrate materials such as silicon, organic, and glass [1]. Silicon substrates offer the best performance and interconnect density but with high cost, while organic substrates show low cost but relatively low performance and density. In case of glass substrates, they offer low cost, reasonable performance, and compatible co-efficient of thermal expansion (CTE) to silicon. However, glass suffers from processing difficulties and poor thermal conductivity when compared with silicon. Thus, the overall performance, reliability, and design cost of 2.5D ICs vary significantly depending on which substrate technology is chosen.

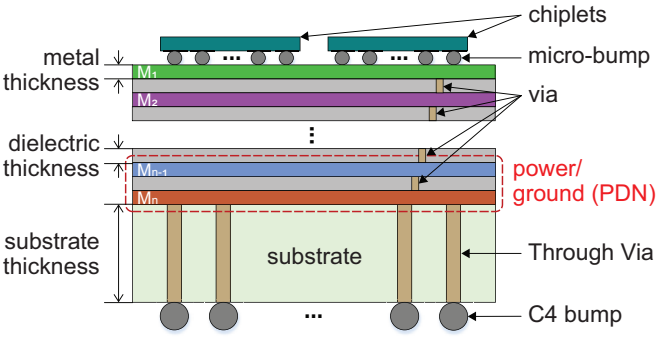


Fig. 1: Vertical stack-up of an interposer-based 2.5D IC designs.

Previous studies have investigated the characteristics of these interposer technologies and their pros and cons. However, they have not carried out their studies at full-system level, nor provide detailed power, performance, area (PPA) comparisons with other substrate technologies. Instead, they have focused primarily on signal integrity (SI) and power integrity (PI) from a given substrate technology [2], [3]. Moreover, the tradeoffs between silicon and organic interposers are generally well known, however, a thorough and quantitative analysis in the system level has not been conducted.

In this paper, we make a significant leap towards the goal of conducting high-quality system-level comparative studies between silicon vs. liquid crystal polymer (LCP) organic interposer technologies. We claim our contributions:

1) We design large-scale heterogeneous 2.5D IC with commercial quality of chiplet and interposer layouts targeting silicon LCP substrates for our study. Intel's Advanced Interface Bus (AIB) [4] is used as I/O drivers for interconnections in the interposer layer.
2) We perform power, performance, area (PPA) analysis, signal integrity (SI) and power integrity (PI) on our 2.5D

TABLE I: Design rules of interposer technologies.

	Silicon	Organic (LCP)
Metal layer #	4	5
Metal thickness	$1\mu m$	$9\mu m$
Dielectric thickness	$1\mu m$	$25\mu m$
Dielectric constant	3.9	3.1
Min. line width/spacing	$0.4\mu m/0.4\mu m$	$4\mu m/4\mu m$
Via size	$0.7\mu m$	$6\mu m$
Through-via size/depth	$10\mu m/100\mu m$	$40\mu m/100\mu m$
Die-to-die spacing	$100\mu m$	$150\mu m$
micro bump pitch	$40\mu m$	$150\mu m$
C4 bump pitch	$400\mu m$	$800\mu m$
PDN width/spacing	$80\mu m/200\mu m$	$80\mu m/200\mu m$

IC designs to show tradeoffs between silicon and LCP interposers. PPA calculations are done with commercial EDA tools. We integrate our PDN and power delivery models into PI analysis which results are in time and frequency domains.

3) We estimate the manufacturing cost of each 2.5D design based on the recent technologies. From the estimation, we offer fabrication cost vs. PPA tradeoffs between silicon and LCP designs.
4) Our study shows that PPA is in a trade-off with SI, PI and manufacturing cost depending on interposer technologies. A key part of this tradeoff study is to quantify the tradeoffs with high-quality designs and simulation results for the first time.

II. Design and Simulation Setup

In our 2.5D IC designs, we choose ROCKET-64 [5] as a benchmark design. This architecture has 8 Rocket tiles each consisting of octa-core RocketCore and L2 cache, a centralized network-on-chip (NoC) as an arbiter and a 4-channel memory controller to access external memories. Each chiplet contains AIBs as I/O drivers to deliver signals in proper timing through the interposer layer.

We create two 2.5D IC designs based on silicon and LCP interposer technologies. The design rules for our interposer designs in this paper are shown in Table I. We choose silicon interposer technology with $0.8\mu m$-pitch RDLs and $40\mu m$-pitch micro bumps based on TSMC Chip-on-Wafer-on-Substrate (CoWoS®) technology [6]. We also choose LCP interposer technology which has $8\mu m$-pitch RDLs and $150\mu m$-pitch micro bumps based on Panasonic R-F705S [7].

Fig. 2 shows the overall design and analysis flow based on the vertically-integrated flow [5]. First, we design the interposer with interposer design rules and micro bump assignments of each chiplet. Then, we generate a transmission line model in the interposer layer and PDN model for the timing, signal integrity (SI) and power integrity (PI) analyses, respectively. Before the chipletization step, we perform I/O driver optimization stage which we explain later. With optimized AIBs, we design chiplets and perform the analysis: IR-drop analysis on chiplets, SI and PI analysis on the interposer and PPA analysis on the overall 2.5D design.

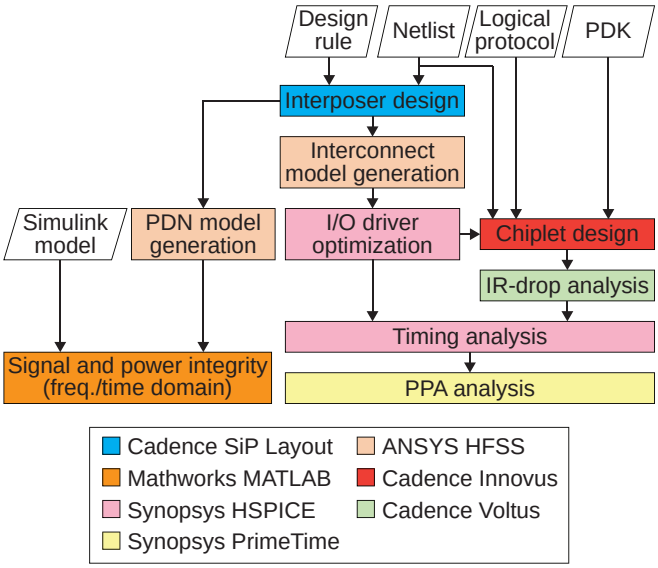


Fig. 2: Our 2.5D IC design and analysis flow using commercial tools.

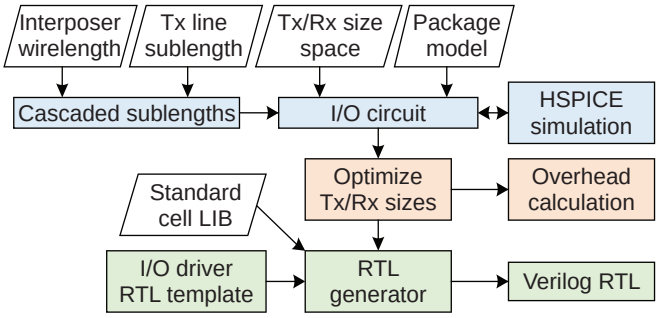


Fig. 3: I/O driver optimization flow.

It is essential to optimize the design of I/O driver for a wide range of wirelengths in 2.5D design to achieve high data rates. Therefore, we add I/O driver optimization stage as illustrated in Fig. 3 to generate multiple sizes of AIBs according to the wirelength distribution of interposer connections. First, the target interposer wirelength is implemented as a SPICE subcircuit of cascaded Tx line models obtained from HFSS. A SPICE netlist is then generated for entire system similar to [8]. Finally, the netlist is simulated in HSPICE over the wide search space of Tx/Rx sizes and the combination resulting in the minimum propagation delay is selected. Verilog RTL for the resulting Tx/Rx sizes are generated using a RTL template for the I/O macro generation.

III. Interposer-based 2.5D IC Design

A. Chipletization of the IPs

During our chipletization step, we perform IC place-and-route (P&R) with the selected protocol translator and optimized AIBs. As the interface protocol for 2.5D systems is important, we choose Hybrid-Link [5] which reduces the I/O count of each chiplet with a flit size of 40. Moreover, chiplet-to-chiplet interconnections are implemented through

the interposer which has larger dimensions and longer wire-length compared with monolithic 2D design. Therefore, we implement well-optimized AIBs as I/O drivers for each input and output to drive the signals without any loss.

A bump assignment is also a key factor to optimize the length of signal connection because each chiplet is connected to the interposer through micro bumps. Therefore, we choose the regular bump assignment which places the minimum 100 P/G bumps at periphery and signal bumps in the center of chiplet and use area I/O placement to minimize the distance from each AIB to its corresponding signal bump.

The GDS layouts and IR-drop maps of chiplets with $1GHz$ target frequency in our benchmark design are shown in Fig. 4 and the detailed chipletization results are summarized in Table. II. We use commercial 28nm and 130nm as the technology nodes for logic and power management chiplets such as integrated voltage regulators (IVRs). In LCP design, the footprint of each chiplet has increased because the pitch of micro bump is 3.75× larger than silicon design. In case of NoC and memory controller (MC) chiplets where the area of micro bump array is dominant over the logic area, the chiplet area has increased by 14.06×.

As chiplets in LCP design have larger footprints, the total cell counts have increased up to 1.6% except L2 cache chiplet to meet the target frequency of $1GHz$. Moreover, the switching power of each chiplet has increased up to 30.4% due to the longer wires, which leads to the increase in total power. In case of MC chiplet, the total power has increased by 16.3%. All chiplets have positive slacks which satisfy the target timing.

For the efficient power delivery in chiplet designs, we use M5 and M6 layers to generate the chiplet PDN mesh. We set the maximum PDN occupancy as 20% for the routability of each chiplet and allow the worst IR drop as 5% of the supply voltage. In LCP design, the worst IR-drop happens at MC chiplet which is 1.30× higher than Silicon design, however, it still satisfies the allowance of $45mV$.

Our IVR chiplet contains a power stage, a feedback/control loop and an LC filter at the output node [9]. The feedback/control loop consists of ADC, type-III proportional integrate-differential (PID) controller and a digital pulse width modulation (DPWM) block. The voltage error calculated from the reference and the output voltages, is compensated by the PID compensator, the output of compensator is fed to a DPWM engine, generating gate signals with a duty cycle based on control word. IVR chiplet in our designs is designed using a commercial 130nm technology node to take advantage of heterogeneity of 2.5D integration.

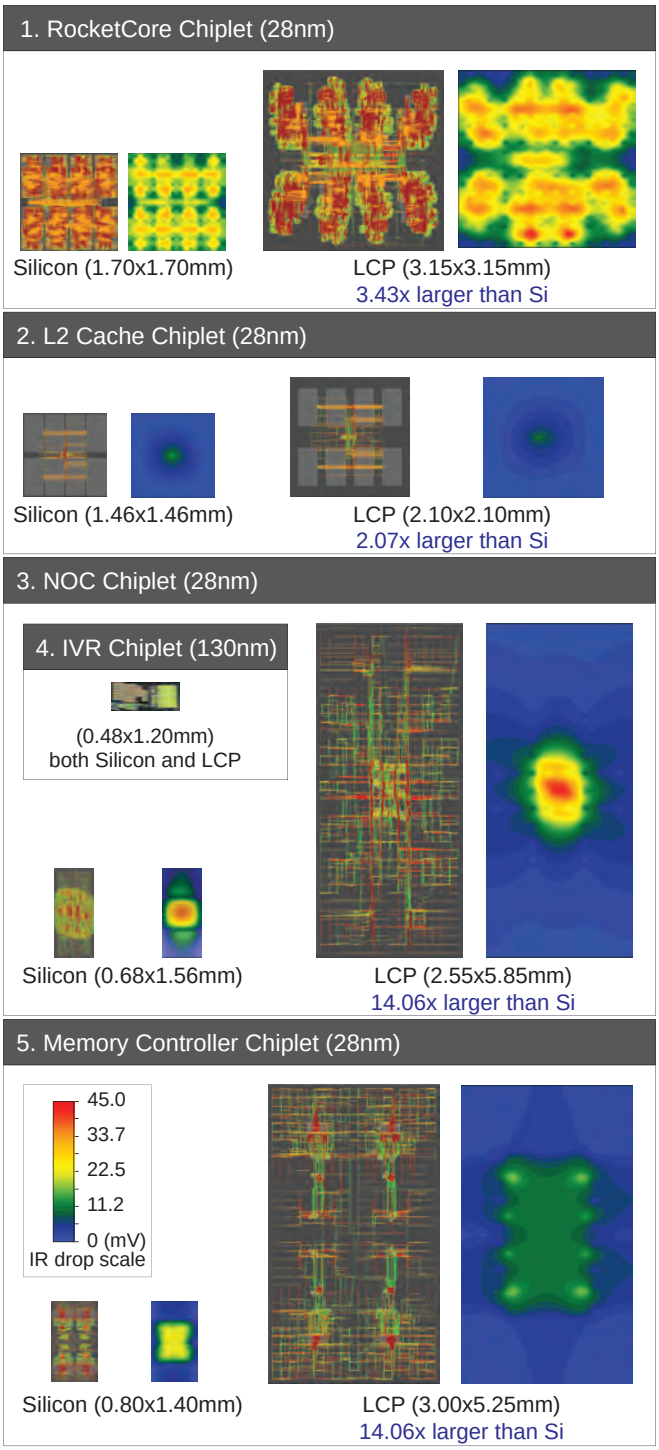


Fig. 4: Physical layout and IR drop map of each chiplet in silicon (left) and LCP (right) designs.

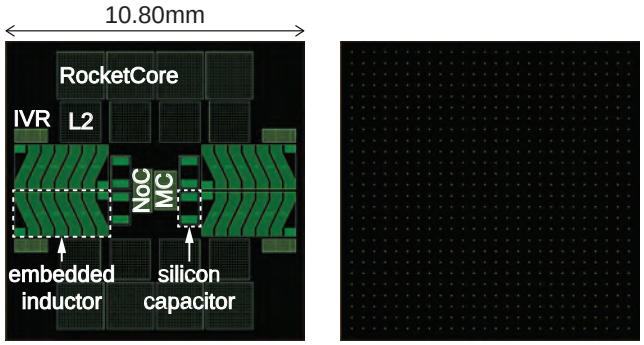
B. Interposer Placement and Routing

GUI-based chiplet placement and interposer routing are done using Cadence SiP Layout XL. Fig. 5 shows the floorplan of our silicon interposer design. We place all chiplets and passive components on the top side of interposer, and all 676 of C4 bumps at the bottom. For passive components, we choose the solenoidal inductor with Nickel-Zinc (NiZn) ferrite magnetic core [10] and integrate on the top metal layer of interposer. We also choose the silicon capacitor which has a low profile down up to $80\mu m$. Considering the IVR configuration with inductor and capacitor, we place both inductors and capacitors closest to the corresponding IVR chiplets.

TABLE II: Chipletization results including the worst IR-drop of chiplet PDNs.

		Rocket Core	L2 cache	NoC	Memory controller
Silicon design					
Cell count (#)		923,764	3,670	80,986	52,074
Worst slack (ps)*		90.81	120.78	113.17	97.99
Total power (mW)		1,034.83	18.52	68.05	45.50
LCP design					
Cell count (#)		938,919	3,555	81,555	52,272
Worst slack (ps)*		157.84	254.92	178.94	208.86
Total power (mW)		1128.69	19.17	75.78	52.92
IR-drop analysis					
PDN M5/6 width (μm)		0.45	0.45	0.45	0.45
PDN M5/6 pitch (μm)		5.0	5.0	5.0	5.0
PDN utilization (%)		18.05	18.02	18.04	18.04
Worst IR-drop (mV)	Silicon	29.51	12.42	32.94	21.20
	LCP	42.20	11.20	42.72	17.67

* The positive slack is used in the table.



(a) top side (chiplets) (b) bottom side (C4 bumps)

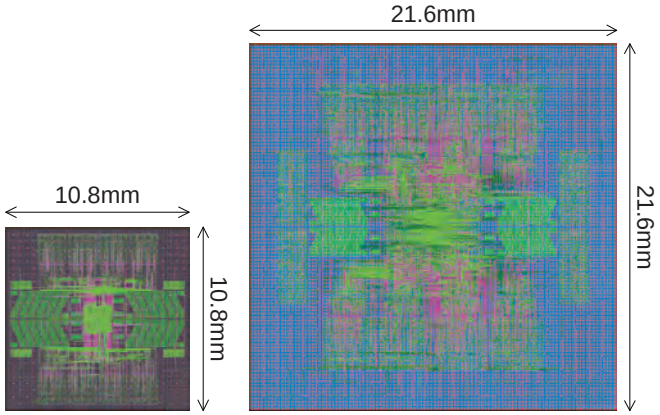
Fig. 5: Chiplet and passive placement in Silicon design: top and bottom side.

In interposer routing, we perform Manhattan routing same as on-chip routing for interconnections in the interposer layer using Automatic Router in Cadence SiP Layout XL. The results of our interposer designs are shown in Fig. 6 and Table III. 1,420 nets are routed through the interposer layer, and 4 and 5 metal layers are used in each design and lower 2 metal layers are reserved for the mesh-type interposer PDN. The silicon interposer has the area of $116.64mm^2$ and the maximum wirelength of $6.97mm$. As design rules in LCP interposer technology are larger than silicon interposer, the area of LCP interposer is larger than silicon interposer by $4.00\times$. Moreover, the maximum wirelength in LCP interposer design is $1.80\times$ longer than silicon interposer design as shown in Fig. 7.

IV. PPA, Signal and Power Integrity Analysis

A. Timing and Power analysis

We perform the timing and power analysis on interposer designs by generating transmission line models in the interposer layers. To run the timing analysis, we generate the unit length model of interposer transmission line as shown in Fig.



(a) silicon (b) organic (LCP)

Fig. 6: Interposer placement and routing results (GDS layout) of silicon and LCP interposers including mesh-type PDNs.

TABLE III: Interposer design (area and wirelength) comparison.

	Silicon	LCP
Metal layers used	4	5
Routed net #	1,420	1,420
Min wirelength (mm)	0.14	0.43
Ave wirelength (mm)	2.83	4.95
Max wirelength (mm)	6.97	12.67
Via usage	5,518	23,237
PDN occupancy (%)	61.65	61.65
PDN DC resistance (mΩ)	17.24	10.08
Area (mm^2)	116.64	466.56

8(a). The unit length is set as $200\mu m$ which is a spacing of power delivery network. We then model the unit cell of transmission line with interposer PDN mesh using ANSYS HFSS. Finally, we extract S-parameter of unit length model and convert this model to SPICE model with $RLGC$ values using the broadband SPICE generator of Keysight ADS.

We perform the timing analysis of interposer channels with a testbench as shown in Fig. 8(b). From the wirelength distribution of interposer wires, we cascade unit length models to generate the target length and incorporate it into HSPICE simulation. The worst propagation delays of silicon and LCP interposer designs are $174.90ps$ and $131.66ps$ respectively which are well within the target timing to meet the setup and hold times.

In power analysis, we obtain the power consumption of logic chiplets by using Synopsys PrimeTime and IVR chiplets from the power delivery efficiency. Moreover, we run HSPICE simulations of AIBs and transmission lines to reflect the effect of interposer wires. Therefore, we estimate the total power of 2.5D system as follows:

$$P_{2.5D} = P_{CORE} + P_{I/O} + P_{PM} \quad (1)$$

where, $P_{2.5D}$ is the total power of 2.5D IC design, P_{CORE} is the power of logic chiplets, $P_{I/O}$ is the power of AIBs and P_{PM} is the power loss from IVRs which are power management chiplets. The analysis results of Silicon and LCP

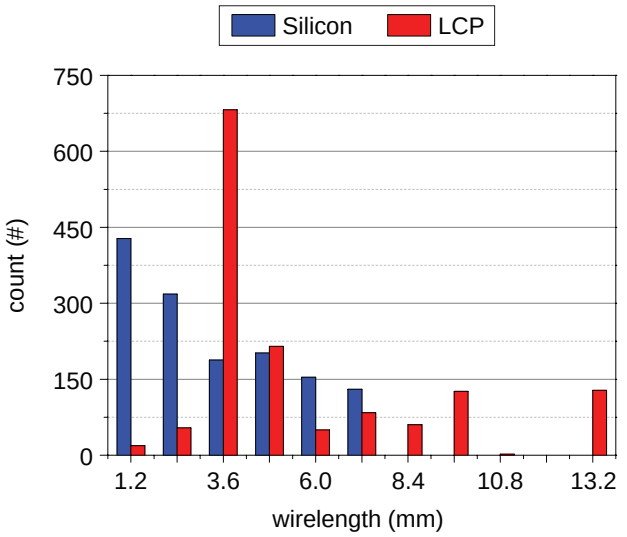


Fig. 7: Wirelength distributions of interconnections in silicon and LCP interposer designs.

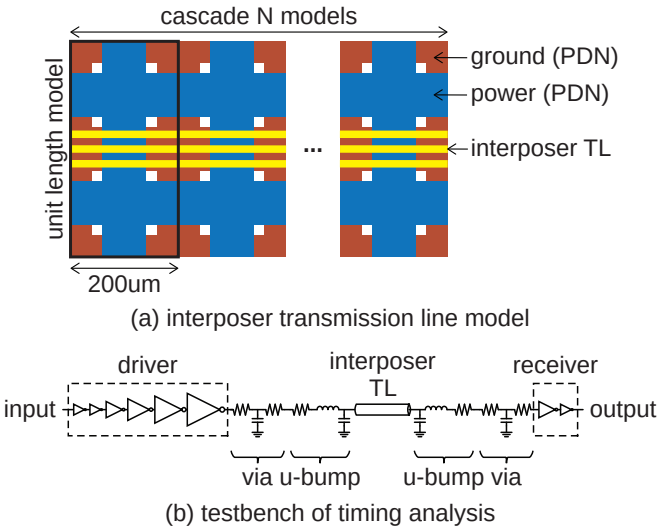


Fig. 8: Testbench for timing analysis of interposer transmission line.

designs are shown in Table V and the detailed discussion is given in Section V-A.

B. Signal and Power Integrity Analysis

For signal integrity (SI) analysis, we extract S-parameter of the transmission line model and generate eye diagrams of each interposer design. We first pick the complex channel model from the dense area of interposer routing as shown in Fig. 9(a). Then, we divide this transmission line model into 5 segments and extract S-parameter of each segment by using ANSYS HFSS. Finally, we import S-parameter models of all segments into Keysight ADS and run the simulation with the data rate of $1Gbps$, the crosstalk model at each input of aggressors, the I/O driver impedance of 50Ω as the ideal case on the transmitter side and $2pF$ for the chiplet pad parasitic on the receiver side. The transmission line in the middle is set as

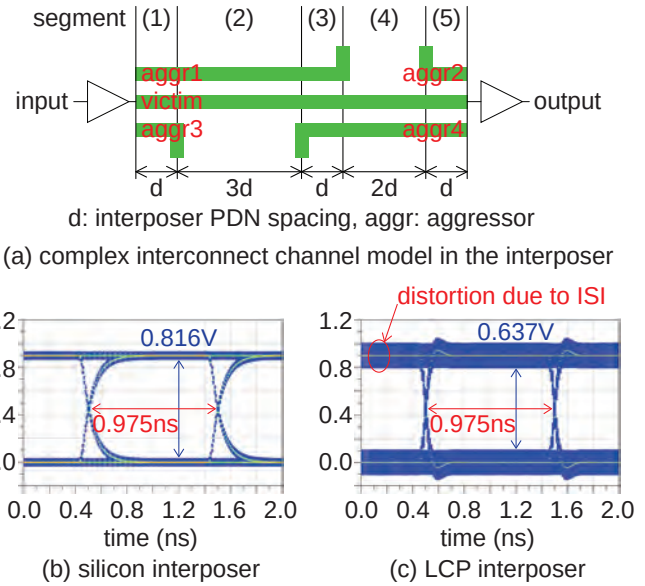


Fig. 9: Complex channel model and eye diagrams of silicon and LCP interposers.

a victim and the top and bottom lines as aggressors to see the crosstalk response. The simulation results of Silicon and LCP designs are shown in Fig. 9(b) and (c), and the detailed comparative analysis of the results is given in Section V-A.

We adopt a mesh-type PDN which is commonly used for the on-chip power delivery solution in our interposer designs. The modeling and analyzing interposer PDN require enormous computing resources since the P/G mesh becomes a large structure. Therefore, in power integrity (PI) analysis, we choose Transmission Matrix Method [11] to divide interposer PDN into M×N unit cells as shown in Fig. 10. Each unit cell is modeled as a lumped Π model which consists of frequency dependent $RLGC$ elements as follows:

$$R = R_s \cdot \frac{S}{4W} \tag{2}$$

$$L = S\left[0.13\epsilon^{(-S/45)} + 0.14ln(\frac{S}{4W}) + 0.07\right] \tag{3}$$

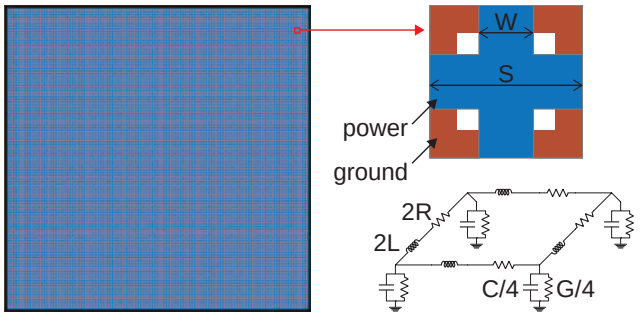
$$C_i = \frac{\epsilon_r}{10^3}\left[(44-28H)W^2 + (280+0.8S-64)W... \\ ... + 12S - 1500H + 1700\right] \tag{4}$$

$$C_f = \epsilon_0\epsilon_r 10^9\left[\frac{4SW\left(ln\frac{S}{S'}+e^{-1/3}\right)}{W\pi+2H\left(ln\left(\frac{S}{S'}+e^{-1/3}\right)\right)} \\ +\frac{2S}{\pi}\sqrt{\frac{2H}{S'}}\right] \tag{5}$$

$$C = C_i + C_f \tag{6}$$

$$G = 2\pi \cdot f \cdot C \cdot tan\,(\delta) \tag{7}$$

where R_s is the surface resistance, W and S are the width/spacing of PDN mesh, $S' = S - 2W$, H is the separation between power and ground layers, and $tan\,(\delta)$ is the loss tangent of dielectric layer. We generate the unit cell model of interposer PDN using ANSYS HFSS, cascade the multiple



(a) mesh-type interposer PDN (b) interposer PDN unit cell

Fig. 10: The modeling of interposer PDN mesh.

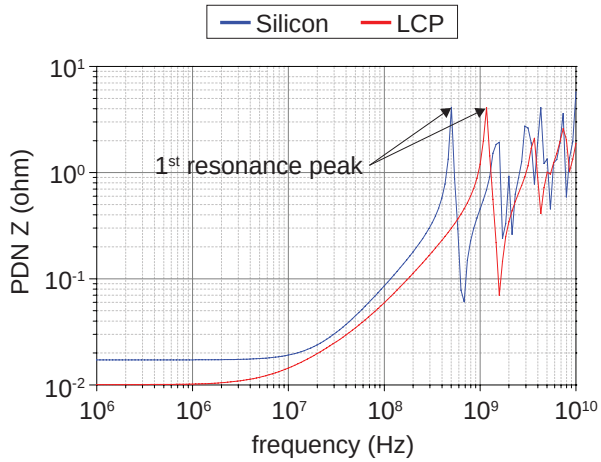
TABLE IV: $RLGC$ values extracted from S-parameters of interposer PDNs at $f_{SW} = 125MHz$.

	R	L	G	C
Silicon	$18.59m\Omega$	$136.13pH$	$18.13mS$	$1.61nF$
LCP	$18.95m\Omega$	$89.35pH$	$2.89mS$	$0.44nF$

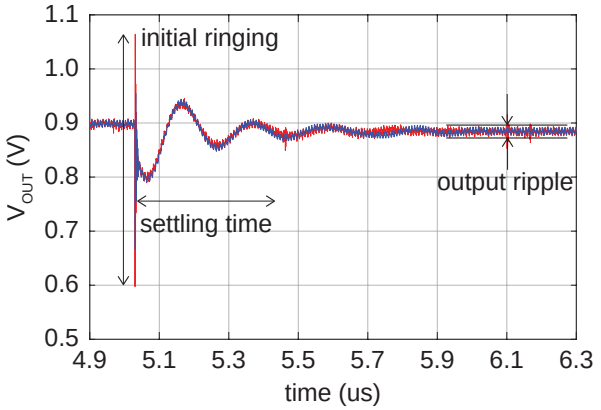
of unit cells and extract S-parameter of the full PDN model using Keysight ADS.

To evaluate the performance of our PDN designs, the current path is identified as micro bumps of IVR chiplets, via, P/G mesh on interposer, via and micro bumps of target chiplets. In PI analysis in frequency domain, all physical parameters in Table I are used for evaluating PDN impedance in interposer designs. Fig. 11(a) shows the PDN impedance comparison between silicon and LCP designs with 10×10 elements of micro bump, via, TSV and C4 bump arrays each.

For PI analysis in time domain, we extract $RLGC$ values from S-parameter at the switching frequency of IVR using Keysight ADS. The calculated $RLGC$ values of interposer PDN in Table. IV and the target load current are imported into the transient simulation with custom Simulink models to estimate the voltage settling time, the initial voltage ringing, output voltage ripple and voltage conversion efficiency. Our Simulink models for IVR chiplet are adopted from CoPEC [12] and the results of transient simulation are shown in Fig. 11(b) and Table V. The detailed comparison of PI results between the two designs are given in Section V-A.



(a) interposer PDN impedance plot



(b) IVR transient simulation

Fig. 11: Power integrity analysis results of silicon and LCP interposers.

V. Design Comparison between 2.5D IC Designs

A. 2.5D IC PPA Comparison

In this section, we perform comparative analysis between our silicon and LCP designs. Table V summarizes our analysis results of silicon and LCP designs so far. The area of LCP design has increased by 4.00× when compared with silicon design due to the larger physical dimensions of LCP interposer technology as shown in Table. I. As the area of LCP design has increased, the average wirelength of interposer wires has also increased by 1.80×. Most of long wires in the interposer are the external interconnections from the memory controller (MC) chiplet to the interposer. Since the pitch of C4 bump is increased in LCP interposer, the lengths of these connections increase, which in turn increases the average wirelength in LCP interposer. As shown in Fig. 12(a), the delay of LCP interposer wire is smaller than Silicon design due to the smaller resistance and capacitance from the fatter wires in the same wirelength. Even though the maximum wirelength is 1.80× higher, the worst propagation delay of LCP design is 0.75× lower than Silicon design.

In LCP design, the logic chiplet power has increased by 1.09× due to the larger sizes of chiplets. As the sizes of chiplets increase, the switching power has increased by 1.15×, which led to the increase in overall chiplet power. As shown in Fig. 12(b), interposer wires of LCP design consume less power than those of Silicon design with the same wirelengths. However, the I/O power has increased by 1.33× in LCP design because LCP interposer has longer interconnections than silicon interposer. Finally, the total power of LCP design is $13.959W$ which is higher than silicon design by 10.46% with 0.02% reduction in power delivery efficiency as well as the increases in chiplet power and I/O power.

Our signal integrity (SI) analysis shows that LCP design has smaller eye height than Silicon design by 21.94% and the same eye width as Silicon design. In our testbench of SI, the

TABLE V: 2.5D IC design results comparison of silicon vs. LCP interposers.

	Silicon	LCP	
Area, Timing, Metal Layer Usage			
Area (mm^2)	116.64	466.56	4.00×
Frequency (GHz)	1.0	1.0	-
Interposer metal layer (#)	4	5	+1
Interposer worst delay (ps)	174.90	131.66	0.75×
Routed Wirelength in Interposer			
Min wirelength (mm)	0.14	0.43	2.99×
Avg wirelength (mm)	2.81	4.95	1.76×
Max wirelength (mm)	7.05	12.67	1.80×
Power Consumption			
Total power (W)	12.636	13.959	1.10×
Logic power (W)	8.540	9.312	1.09×
I/O power (W)	0.530	0.705	1.33×
IVR power (W)	3.566	3.942	1.11×
Signal Integrity			
Eye width (ns)	0.975	0.975	1.00×
Eye height (V)	0.816	0.637	0.78×
Power Integrity			
Interposer PDN occupancy (%)	61.65	61.65	1.00×
Interposer PDN DC R($m\Omega$)	17.24	10.08	0.59×
Conversion ratio (V/V)	3.6/0.9	3.6/0.9	-
Inductor (L,nH)	25	25	-
Capacitor (C,nF)	200	200	-
f_{SW} (MHz)	125	125	-
Decap. (nF)	25	25	-
Output voltage ripple (mV)	12	16	1.33×
Initial ringing (V_{PP}, mV)	288	467	1.62×
Power efficiency (%)	71.78	71.76	-0.02%
Settling time (ns)	298	298	1.00×
DVFS (mV/ns)	200/439	200/439	1.00×

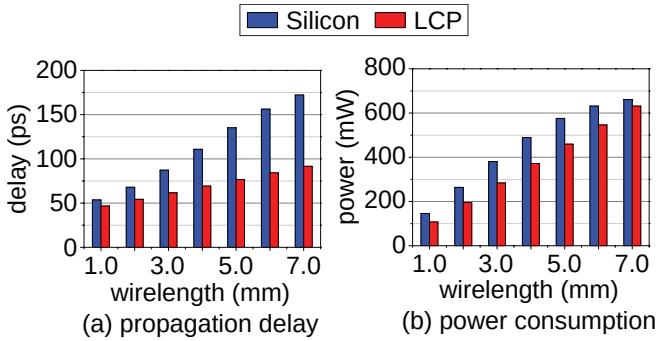


Fig. 12: Power comparison of interposer wires in Silicon and LCP design.

receiver side has $5pF$ capacitor without any shunt resistor. Due to the impedance mismatch at the receiver side, the signal of the victim line reflects and propagates back to the transmitter side when it arrives to the capacitor. Therefore, the reflected signal distorts other signals in the victim line which is an intersymbol interference (ISI).

As the length of complex channel model is same in each designs, the transmission line in LCP design has the resistance of 1.45Ω which is 2.01% of Silicon design because of the larger dimensions of wires as shown in Table VI. In Silicon design, the reflections attenuate faster than LCP design because

TABLE VI: $RLGC$ values extracted from S-parameters of transmission line at $1GHz$.

	R	L	G	C
Silicon	72.06Ω	$525.31pH$	$165.48\mu S$	$0.36pF$
LCP	1.45Ω	$502.58pH$	$162.06\mu S$	$0.26pF$

the transmission lines are lossy. However, in LCP design, the reflections play a much bigger role than Silicon design due to the smaller resistance. Therefore, the eye distortion in LCP design becomes worse due to the effect of ISI.

In terms of PDN impedance, Silicon design has a higher impedance than LCP design as shown in Fig. 11(a). The PDN in Silicon design shows $17.24m\Omega$ of DC impedance compared to $10.08m\Omega$ in LCP design. Moreover, the first resonance peak in Silicon design comes at $0.50GHz$, whereas at $1.17GHz$ in LCP design. It shows that LCP design has 2.34× better bandwidth than Silicon design approximately.

For the PI analysis in time domain, we use $25nF$ of decoupling capacitor and give the load jump from $250mA$ to $1.55A$. In both Silicon and LCP designs, the voltage settling time is $289ns$ and dynamic voltage and frequency scaling (DVFS) is evaluated as $200mV/439ns$. However, LCP design shows 1.62× higher initial ringing and 1.33× larger output ripple at the output node of IVR chiplet as shown in Fig. 11(b) due to the high reduction in C as shown in Table IV. When comparing LCP design to Silicon design, L has been reduced by 0.66×, but C is also reduced by 0.27× because of lower dielectric constant and higher dielectric thickness.

Silicon design shows 71.78% of voltage conversion efficiency, while LCP design has 71.76% similar to Silicon design. This efficiency loss of 0.02% in LCP design happens because DC resistance of interposer PDN is smaller than Silicon design, but the loss due to the output voltage ripple is more significant. These comparisons between Silicon and LCP designs show the tradeoffs in terms of PPA, SI and PI depending on the interposer technologies.

B. 2.5D IC Manufacturing Cost Comparison

In this section, we perform the overall manufacturing cost analysis on silicon and LCP designs to investigate the cost benefit of interposer technologies. The fabrication cost of each 2.5D design is estimated as follows [13]:

$$N_{chiplet} = \frac{\pi \times (\phi_{wafer}/2)^2}{A_{chiplet}} - \frac{\pi \times \phi_{wafer}}{\sqrt{2 \times A_{chiplet}}} \tag{8}$$

$$C_{chiplet} = \left(\frac{C_{wafer}}{N_{chiplet}} + C_{test} \right) / Y_{chiplet} \tag{9}$$

$$C_{2.5D} = \frac{\frac{C_{interposer}}{Y_{interposer}} + \sum_{i=1}^{n} \left(\frac{C_{chiplet,i}}{Y_{chiplet,i}} + C_{bond_i} \right)}{{Y_{bond}}^{n-1}} \tag{10}$$

where, $N_{chiplet}$ is the number of chiplets on a single wafer, $A_{chiplet}$ is the die area of each chiplet, ϕ_{wafer} is the diameter of wafer, and C and Y are the cost and yield.

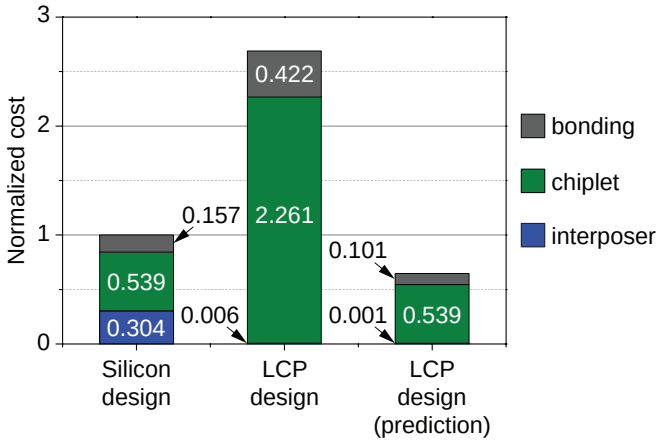


Fig. 13: 2.5D IC manufacturing cost comparison between silicon vs. LCP interposers.

TABLE VII: Parameter assumptions for 2.5D IC cost analysis.

Cost Analysis Parameter Assumptions			
	diameter	cost	yield
28nm technology wafer	12inch	$3,500	98%
130nm technology wafer	8inch	$2,000	98%
silicon interposer wafer	12inch	$700	98%
LCP interposer cost		$\$5/ft^2$	[14]
micro-bump bonding yield		99%	

The total cost of 2.5D design can be divided into interposer, chiplet and bonding costs for simplicity, and we estimate the cost of our 2.5D designs as shown in Fig. 13 with parameters in Table VII. The total cost of LCP design is 2.69× more expensive than Silicon design even though the LCP interposer cost is 1.91% of silicon interposer. This increase comes from the cost of chiplets which is 4.20× higher than Silicon design. It is caused by larger areas of chiplets due to larger design rules in LCP interposer technology.

We also estimate the total cost of LCP design assuming improvements of interposer technology same as silicon interposer, which has reduced by 0.64× compared with silicon design. As the footprint of LCP interposer has decreased due to improved dimensions, the interposer cost has decreased by 0.25× and the cost of chiplet by 0.24×. This predicted result indicates that the dimension improvement is necessary to maximize the low-cost benefit in LCP interposer technology.

VI. Conclusion

In this paper, we conduct quantitative comparisons in terms of power, performance and area (PPA), reliability, and cost between silicon and organic interposer-based 2.5D systems using commercial quality designs and simulations. We develop a power delivery network (PDN) analysis framework that integrates frequency domain component models into time domain simulations for the analysis of PDN and power delivery modules. Our experiments showed a wide range of tradeoffs in terms of PPA, SI and PI between the two interposer material choices. LCP-based 2.5D design has 4.00× larger area and 1.10× higher power consumption than silicon-based design. However, LCP design has 0.75× less delay in interposer layer and 0.59× lower impedance of interposer PDN when compared to Silicon design. Surprisingly, our cost analysis indicated that the overall cost of organic LCP technology, if both the chiplets and their interposer costs are combined, is 2.69× higher than silicon technology even if the interposer cost is 1.91% of silicon interposer. Our predictive cost of LCP interposer-based design indicates that the interconnect and bump dimensions should be dramatically improved to maximize the cost benefit of LCP interposer technology.

Acknowledgements

This research is funded by the DARPA CHIPS program under Award N00014-17-1-2950.

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