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Distinguished Lecture

Design Methodology Challenges for Large-Scale Chiplet Assemblies
Professor Puneet Gupta
Electrical and Computer Engineering Department
University of California, Los Angeles (UCLA)
December 9, 2021 at 8:00am PDT / 11:00pm EDT
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Abstract:

As conventional technology scaling becomes harder, 2.5D integration provides a viable pathway to building larger systems at lower cost. We start with discussing challenges in designing large chiplet assembly-based systems drawing from our ongoing effort to build a 2000 chiplet waferscale processor system. Next, we describe a cross-stack pathfinding framework for large distributed 2.5D/3D systems, identifying areas where technology development would help design metrics substantially.

Bio:

Puneet Gupta received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Delhi, New Delhi, India, in 2000, and the Ph.D. degree from the University of California at San Diego, San Diego, CA, USA, in 2007. He is currently a Faculty Member with the Electrical and Computer Engineering Department, University of California at Los Angeles. He Co-Founded Blaze DFM Inc., Sunnyvale, CA, USA, in 2004 and served as its Product Architect until 2007. He has authored over 170 papers, 18 U.S. patents, a book and a book chapter in the areas of design-technology co-optimization as well as variability/reliability aware architectures. Dr. Gupta was a recipient of the NSF CAREER Award, the ACM/SIGDA Outstanding New Faculty Award, SRC Inventor Recognition Award, and the IBM Faculty Award. He currently co-leads the multi-university CDEN+ Center which focuses on future semiconductor technologies.

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