A Reconfigurable Hybrid Low Dropout Voltage Regulator for Wide-Range Power Supply Noise Rejection and Energy-Efficiency Trade-Off

Saad Bin Nasir, *Student Member, IEEE*, Shreyas Sen, *Senior Member, IEEE*, and Arijit Raychowdhury, *Senior Member, IEEE*

***Abstract*—A scan-reconfigurable hybrid low dropout (LDO) macro with four operating modes to support tuning across a wide range of power supply noise rejection and power efficiency is presented. The configurations include: 1) a full-digital LDO; 2) an analog loop in parallel with a digital loop in switched mode control; 3) an analog LDO in parallel with discrete current sources; and 4) discrete current sources with an analog LDO in shunt with the load. Measurements on a 130-nm CMOS test chip show a wide power supply noise rejection range of −9 dB to −34 dB and a corresponding power efficiency range of 87% to 56%.**

***Index Terms*—Linear voltage regulator, LDO, noise rejection, on-chip power management, hybrid design.**

I. Introduction

DIGITAL low dropout (LDO) linear voltage regulators serve as key enablers for fine-grain power management right at the point-of-load (PoL) inside complex multi-core processors and system-on-chip (SoC) platforms [1]. They offer digital process flow synthesis, automated placement and routing, large operational voltage range and fast transient performance making them suitable for digital load circuits. On the downside, they suffer from steady state voltage ripple and low power supply noise rejection (PSR) due to their digital control and fully-on or fully-off quantized power stage. These limitations make the application of digital LDOs to power noise sensitive analog circuits infeasible. To address these limitations, this brief presents a hybrid LDO using both analog and digital LDO operational principles while keeping the benefits of a digital LDO [2]–[4]. In this design, we trade-off energy efficiency and area to improve PSR of a digital LDO across a wide-range to enable optimal power delivery for both noise-sensitive analog and fast-transient digital load circuits.

The presented hybrid LDO is especially suited for wide operational range analog circuits like multi-standard, multi-rate I/O [5] and wireless links. In these designs, the high-performance modes necessitate inclusion of LDOs with high PSR over the entire spectrum. These LDOs use high dropout voltages and increased bias currents resulting in low power efficiency. On the other hand, there are a number of low power modes that can operate at a lower PSR but need high power efficiency. Due to the lack of availability of LDOs with wide-range of programmable PSR and power efficiency, it is common practice to include a high PSR LDO and enable it only in the high-performance modes [5]. This results in lower power efficiency in low power modes if the same high PSR LDO is employed. To address this shortcoming, a reconfigurable LDO macro is presented that can switch across four different topologies through scan reconfiguration. These topologies are based on all-digital and analog topologies that are operated using switched-mode-control [6], [7] and represent different PSR vs. energy efficiency vs area trade-offs. Key circuit blocks are shared and these blocks are enabled or disabled as required to minimize area and power overhead. This hybrid design does not serve as a replacement for high PSR analog LDOs but highlights the improvement achievable in PSR over baseline digital LDOs using SMC.

Measurement results from a 130nm CMOS test-chip demonstrates a wide-dynamic range of PSR from -9dB to -34dB at 100MHz and correlated power efficiency of 87% to 56%, respectively. The LDO drives a ring-oscillator based voltage controlled oscillator (VCO) and a linear feedback shift register (LFSR) load circuit. We measure the VCO phase noise and the eye-opening at the output of the LFSR under application of supply noise. We demonstrate that the reconfigurable LDO macro can be configured to enable varying levels of PSR, which results in a minimum eye opening of 25mV/350ps and a maximum eye opening of 150mV/1.9ns under iso-supply noise conditions (15mVp-p).

After this brief introduction, Section II elaborates the architecture and operational modes of the hybrid LDO macro. In Section III, we explain the analog components of the design followed by measurement results in Section IV and conclusion in Section V.

II. LDO Architecture and Configuration Settings

The LDO macro leverages recent advances in energy efficient all-digital LDOs [2], high-PSR analog LDOs [4] and

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S. B. Nasir and A. Raychowdhury are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: saadbinnasir@gatech.edu).

S. Sen is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA.

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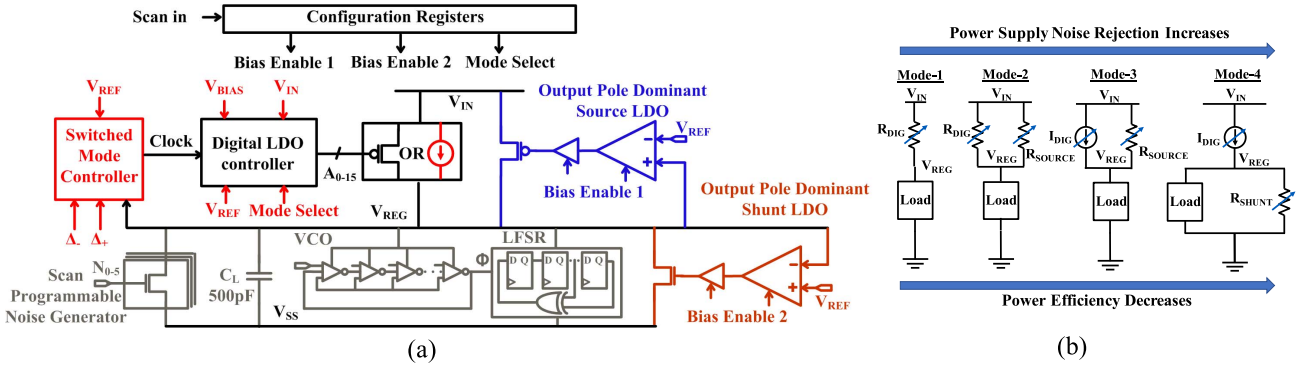
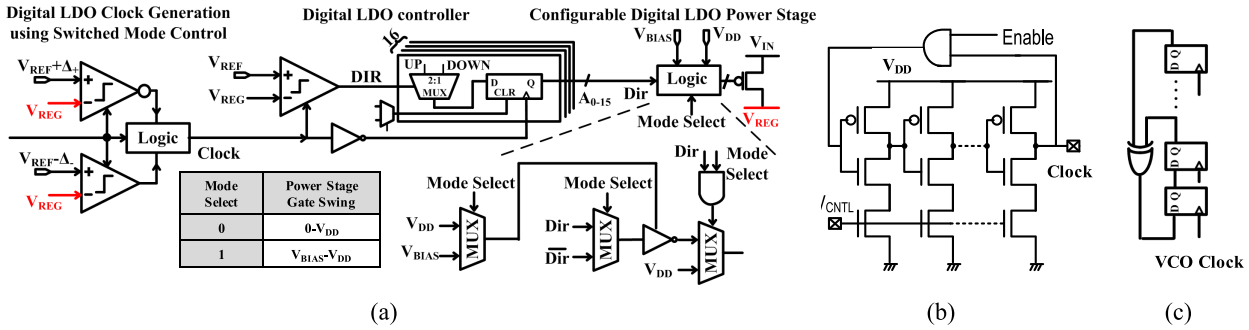


Fig. 1. Hybrid low dropout (LDO) voltage regulator design with scan reconfigurable operational modes and PSR vs energy efficiency trade-offs.



Mode Select	Power Stage Gate Swing
0	0-V_{DD}
1	V_{BIAS}-V_{DD}

Fig. 2. (a) Full-digital LDO architecture with current sources/switch programmability (b) Current starved VCO load circuit (c) 9-stage linear-feedback shift register (LFSR) load circuit.

switched mode control (SMC) [6], [7]. It supports four scan programmable modes of operation by enabling or disabling relevant circuit blocks to meet load PSR requirement. These four distinct sections in the system-level LDO schematic are shown in different colors in Fig. 1a. These four modes achieve noise rejection on regulated voltage (V_{REG}) from supply node V_{IN} by modulating the current delivery between supply (V_{IN}) and V_{REG}, and V_{REG} and ground as shown by the simplified graphical schematics in Fig. 1b. These four modes, their circuit implementations and key design principle are described below.

A. Mode-1

In mode-1, an all-digital design with an array of PMOS power MOSFETs operating in the linear region supplies the load current. A clocked sense-amplifier based comparator compares the output voltage (V_{REG}) with the reference (V_{REF}) and controls a shift register which turns-on or turns-off the power MOSFETs as required (see Fig. 2). This mode shows highest power efficiency and input voltage (V_{IN}) scalability but low PSR. The digital LDO clock (F_{CLK}) is set at 10MHz for the current design to meet a target limit-cycle oscillation (and hence output ripple of <5mV) [8]. It is generated through a current-starved ring oscillator. Design details of the digital loop and its control settings are shown in Fig. 2.

B. Mode-2

In this mode, the digital power MOSFETs of mode-1 are supplemented with an analog LDO (source LDO) running in parallel. The source LDO supplies a part of the total load current (10-50%). The instantaneous small-signal gain of the analog loop increases the PSR at the cost of higher power. Two comparators compare V_{REG} with $V_{REF} \pm \Delta_{\pm}$ and run the digital LDO only when $V_{REG} < V_{REF} - \Delta_{-}$ or $V_{REG} > V_{REF} + \Delta_{+}$ via SMC (see Fig. 2). During steady-state operation only the analog LDO regulates and the digital LDO shares a part of the load current. During current transients, the digital loop is activated and provides additional current. This control topology provides: (1) Fast transient response under load steps by turning the digital devices on or off without bandwidth limitation and (2) No output ripple, as the digital loop is frozen and does not undergo limit cycle oscillations in the steady-state. SMC combines the excellent small signal characteristics of an analog LDO with the high current driving capability of the digital power MOSFETs. The digital loop is clock gated when the output voltage is within the dead-zone reducing the controller current. Interested readers are referred to [6] and [7] for more details on SMC and its associated design and stability which is not a part of this brief.

C. Mode-3

In mode-3, the digital LDO power MOSFETs are reconfigured into discrete current sources running in saturation mode, by biasing their gates through mux-logic (see Fig. 2). The mux-logic either biases the gates at V_{BIAS} (mode-3) or at ground (mode-2). This topology also follows SMC configuration. In mode-3, the LDO consumes higher bias/controller current (i.e., exhibits lower power efficiency) but has significantly

$$\omega_{DOM} = \frac{1}{R_{LOAD}C_{LOAD}} \qquad \omega_2 = \frac{1}{R_{OUT,OTA}C_{P2}} \qquad \omega_3 = \frac{1}{R_{OUT,BUFF}C_{P3}}$$

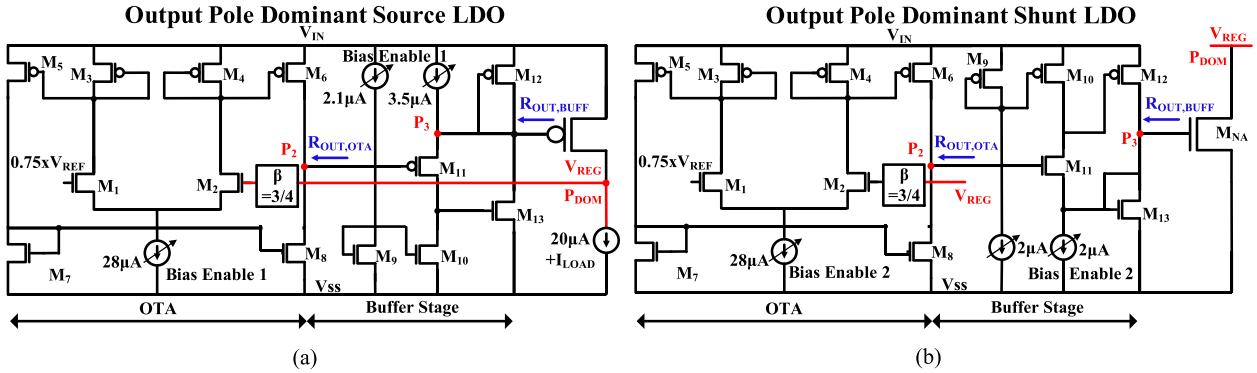


Fig. 3. Design schematic of output pole dominant analog voltage regulators acting as (a) source and (b) shunt LDOs. Source LDO topology is based on [6] and [7].

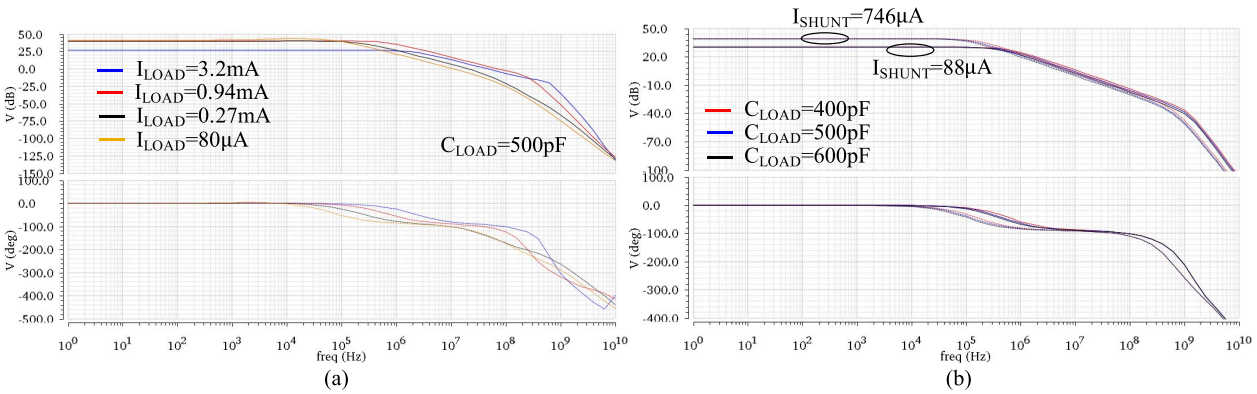
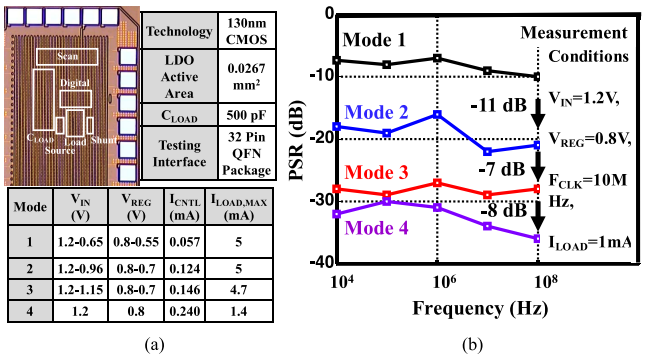


Fig. 4. Simulated open loop bode plots of (a) source LDO under varying load current conditions (b) shunt LDO under varying load capacitance values.



Mode	V_{IN} (V)	V_{REG} (V)	I_{CNTL} (mA)	$I_{LOAD,MAX}$ (mA)
1	1.2-0.65	0.8-0.55	0.057	5
2	1.2-0.96	0.8-0.7	0.124	5
3	1.2-1.15	0.8-0.7	0.146	4.7
4	1.2	0.8	0.240	1.4

Fig. 5. Chip micrograph with test interface and operational range of the LDO macro in different modes (b) Measured PSR.

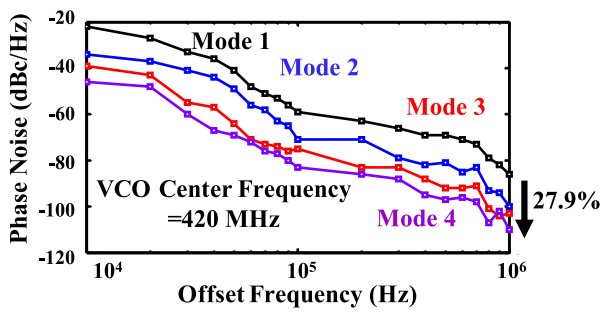


Fig. 6. Measured phase noise of the designed VCO is shown. Measurements with 15mVpp ripple at 100 MHz on the supply.

improved PSR as the discrete digital devices are biased in saturation offering inherent noise resilience. Due to decreased current supply from these biased digital power MOSFETs, the total operating current range of the LDO is lower than that in mode-2.

D. Mode-4

The role of improved PSR is to suppress noise at the output of the LDO (V_{REG}). Apart from coupling and switching noise at the line voltage (V_{IN}), a significant component of line noise is self-inflicted, i.e., the load switching (di) at V_{REG} causes noise at V_{IN} (due to package and PCB parasitic inductance) [5]. Hence, reducing noise at V_{IN} will itself lower the noise at V_{REG}, and will add to increased PSR of the LDO. In mode-4, we address this issue by (1) supplying constant current through discrete current sources from V_{IN} to V_{REG} and (2) regulating V_{REG} with an NMOS LDO operating in shunt with the load in SMC configuration. This topology: (1) reduces V_{REG} noise through the high PSR shunt LDO and

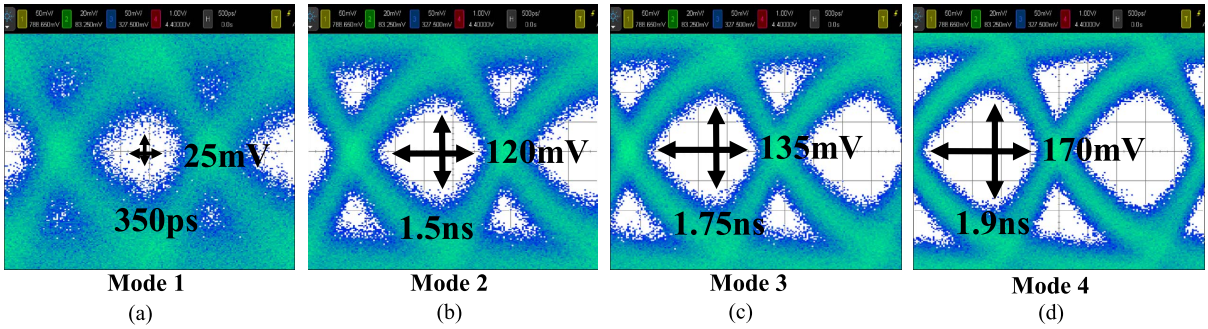


Fig. 7. Measured LFSR eye plots, generated using 1000 cycles and 15mVpp ripple on the supply, show the gradual performance improvement from (a) mode 1 to (d) mode 4.

(2) eliminates self-injected noise at V_{IN} by redirecting current from the shunt LDO to load under load current changes. The shunt LDO consumes 10-25% (depending on the work-load) of the load current (see Fig. 4a) and provides the highest noise rejection at the cost of power efficiency.

Critical circuit blocks, including the error amplifiers, biasing arms, digital power devices, scan blocks are shared among the four modes to minimize area and power (leakage) overhead.

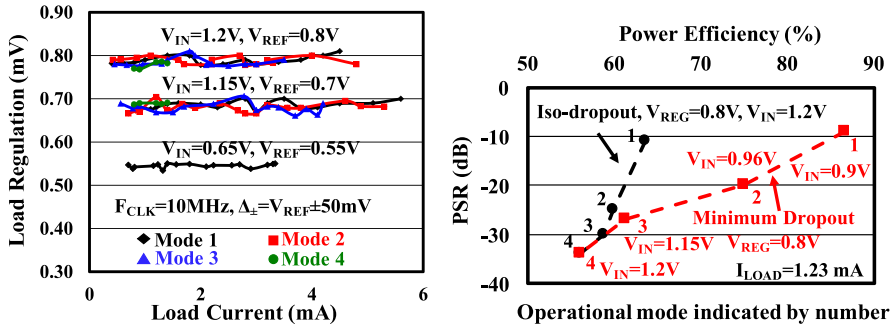
III. Design of Analog Regulation Loops

The load sharing between discrete devices (in linear for mode-2 or saturation for mode-3) and the analog loop (source for mode-2 and mode-3 or shunt for mode-4) reduces the current demand on the analog power MOSFETs. The small dynamic current (15-20% of the total load current) can be delivered by a smaller power PMOS (source LDO) or NMOS (shunt LDO) resulting in smaller internal capacitor at the gate of these power MOSFETs. This allows us the opportunity to realize output pole dominant analog LDOs without using bulky off-chip capacitors. A shunt buffer between an operational trans-conductance amplifier (OTA) and the power MOSFETs (see Fig. 3) further pushes the internal poles to higher frequencies. This results in output pole of the LDO being the dominant pole with only 500pf (at 1V) of on-die MOS capacitor. This topology shows: (1) High bandwidth noise rejection (2) No PSR peaking, which is a typical challenge for conventional internal pole dominant analog LDOs [9] (3) Unity-gain bandwidth increase with increasing load current and (4) Added supply noise rejection beyond unity-gain bandwidth of analog LDOs as the power MOSFETs gates modulate in-phase with noise thanks to the design of buffers controlling the power MOSFETs.

The design of the source LDO (mode-2 and mode-3) is based on [6] and [7] and the shunt LDO features a complementary NMOS design. Two replicas of a PMOS analog LDO act as the source LDO capable of providing up to 3.2mA of load current. A load current of 40μA is drawn to maintain stability at a low V_{IN} of 0.96V. The design offers greater than 28dB open loop gain at 3.2mA load current while maintaining a phase margin of greater than 70° as shown in simulation results of Fig. 4a. A single NMOS analog LDO acts as a shunt LDO capable of sinking up to 750μA load current. At 746μA, a gain in excess of 40dB is achieved with a phase margin of over 70° as shown in Fig. 4b.

IV. Measurement Results

The test-chip is fabricated in GF 130nm CMOS (Fig. 5a). The maximum load current that can be delivered decreases as discrete devices are biased as current sources (mode-3) and further when the shunt LDO is activated (mode-4). Correspondingly, the bias/controller current increases from mode-1 to mode-4. This results in decreasing current efficiency from mode-1 to mode-4. The minimum dropout increases from mode-1 (80mV) to mode-4 (400mV). Thus, we observe a monotonic increase of current and power efficiency as the LDO is reconfigured from mode-4 to mode-1. The plot of PSR vs frequency in Fig. 5b (measured with 80mVp-p injected input noise at V_{IN}) demonstrates: (1) Programmable and increasing PSR from mode-1 (−9dB at 100MHz) to mode-4 (−34dB at 100MHz), (2) PSR improvement from mode-3 to mode-4 through reduction of self-injected noise at V_{IN}, (3) High PSR bandwidth and no PSR peaking, consistent with an output pole dominant LDO loop. To understand the efficacy of the design, we measure the performance of the LFSR and VCO circuits (see Fig. 6 and Fig. 7) under 15mV p-p input line noise (at V_{IN}). The single sideband phase noise of the free-running VCO illustrates 27.9% improvement at 1MHz from mode-1 to mode-4. It should be noted that the phase noise measurements were performed with injected noise at V_{IN} as well as switching load at V_{REG}. This captures the true phase noise when a digital load circuit operating on a shared V_{IN} injects switching noise to the supply. Oscilloscope captures of the LFSRs output running at 420MHz shows an increasing eye-opening for 1000 cycles from mode-1 (25mV/350ps) to mode-4 (150mV/1.9ns). Measured load regulation is shown in Fig. 8a with near-threshold operation in mode-1. The LDO macro provides a wide range of PSR and power efficiency. PSR and power efficiency is measured for iso-dropout ($V_{IN} = 1.2$V and $V_{REG} = 0.8$V) and minimum dropout (at $V_{REG} = 0.8$V) that can be supported in each mode as shown in Fig. 8b. From mode-1 to mode-4, the PSR increases monotonically (peak PSR is −34dB at 100MHz). Within each mode, we observe increasing PSR with increasing dropout thus providing the flexibility of selecting a desired PSR. Correlated with decreasing PSR is an increase in power efficiency as the macro is reconfigured. Peak power efficiency of 87% (mode-1), 75% (mode-2), 61% (mode-3) and 56% (mode-4) are measured. Area overhead for each mode compared to the baseline mode-1 is summarized in Fig. 8c. A Figure-of-Merit (FOM) that



(a) (b) (c)

Mode	Total Area (mm^2)	Area Overhead
1	0.0140	1x
2	0.0153	1.096x
3	0.0267	1.909x
4	0.0261	1.867x

Fig. 8. (a) Measured load regulation across the complete operational range shows high DC accuracy. (b) A programmable range of 23dB PSR is measured with a change of 35.6% power efficiency. (c) Silicon area trade-off for different modes of operation.

TABLE I
PERFORMANCE COMPARISON

Parameter	This Work	[5]	[4]	[8]	[10]
Technology	130nm CMOS	22 nm CMOS	65nm CMOS	130 nm CMOS	180nm CMOS
LDO Type	Digital, Hybrid	Hybrid	Analog	Digital	Analog
Reconfiguration	Yes	No			No
PSR (dB)	-9 to -34 at 100MHz	-30 at DC	~-22.5 at 100 MHz	NA	-76 at 1 MHz, 0 at 100 MHz
Load Capacitance (nF)	0.5	NA	0.14	1	0.1
Maximum Load Current (mA)	5	NA	10	4.6	100
Min. Quiescent Current (mA)	0.057	NA	0.05	NA	0.071
Reconfiguration Range	PSR (3.7X), η (1.55X)	No reconfiguration range			
Peak Current Efficiency	98.86	85-90	99.5	98.3	99.93
FOM= (Peak Linear |PSR|*.η) at Frequency	28.06 at 100MHz	25.36 at DC	11.05 at 100 MHz	NA	0 @ 100MHz, 5602 @ 1MHz

η = Peak Power Efficiency, * Linear $|PSR| = \frac{\Delta VIN}{\Delta VREG}$ across the complete frequency range
NA = Not Available

captures the wide tunable range of PSR is defined in Table I. The design shows competitive performance compared to recent LDO designs [4], [5], [8], [10].

V. CONCLUSION

This brief presents a scan-programmable hybrid LDO macro which provides a wide range of power supply noise rejection and power efficiency trade-off. Such a design is suitable for wide operational range analog or digital load circuits like I/O circuits. Measurements on a 130nm test-chip show a PSR (Power efficiency) range of -9dB (87%) to -34dB (56%).

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