A 65nm Compressive-Sensing Time-Based ADC with Embedded Classification and INL-Aware Training for Arrhythmia Detection

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***Abstract*—In-sensor analytics are in high demand to avoid high computation at server back end. Traditional analog sensors require high supply voltage in the range of 1-1.2V even when digital supplies are scaled down to 0.4V-0.6V. We propose a time-based compressed-domain analog-to-digital (ADC) based encoder with parallel processing units for arrhythmia classification. The computationally enhanced ADC performs in-situ compression along with analog to digital conversion. An accuracy of 84% accuracy is achieved with 10.5nJ energy per classification for an 8X compression ratio.**

***Index Terms*—Smashed-filter, time based ADC, low power**

I. Introduction

In electrocardiogram (ECG) systems, compressive sensing (CS) based signal acquisition has been proposed to reduce the power of the sensor front-end [1]. Additionally, enabling machine learning algorithms to perform in-sensor classification has also gained momentum [2]. Low power and low supply voltages are crucial for embedded sensors and systems.

Recent work on compressive sensing encoders [3] demonstrates data compression to reduce telemetry bandwidth using Quasi-Cyclic Array Code (QCAC) matrices. Streaming principle component analysis (PCA) based data compression technique is proposed in [4] for neural local field potentials. It achieves 8X compression with 3% reconstruction error. However, performing classification in the compressed domain enables even greater power savings [5]. There has been recent work on ADC based in-sensor compressive sensing circuits as reported in [6] [7] [2]. All of the reported works perform computation in voltage domain along with data-conversion. However, the minimum supply required in all of these reported circuit architectures [7] is 1-1.2V. However, a lower supply voltage is preferred for V^2 power savings. Also, a low supply voltage is compatible with traditional digital scaling. Hence, voltage controlled oscillator (VCO) based ADC's have become attractive for both low supply operation and process scalability [8] [9]. Fig. 1 (a) shows a traditional sensor system with an ADC and a CS encoder. While it reduces the power in telemetry, it doesn't perform any classification. Also, traditional sensor interface requires the ADC to operate at a higher supply [5] while the digital back end operates at a low supply (0.4-0.6V). This architecture is not efficient in terms of power. Fig. 1 (b) shows the proposed embedded sensor/classifier interface. We propose a sensor interface where both the ADC sensor and the classifier can operate on the digital supply. This is achieved by a novel time based compressive sensing ADC. Compared to traditional voltage mode amplifier based ADCs, time-based ADCs can operate at lower supply and provide in-situ compression of the sensor data. We use the MIT ECG database for analyzing the accuracy of the classifier classifier. The task of the binary classifier is to classify whether the recorded ECG has arrhythmia or not. Fig. 2 (a) shows a recording of an arrhythmia signal. A 10sec frame of the recorded period is used. It has 208 normal and 96 abnormal beats. Fig. 2 (b) shows the compressed ECG compressed with a $+1, -1$ random signal with compression ratio (CR) of 3.

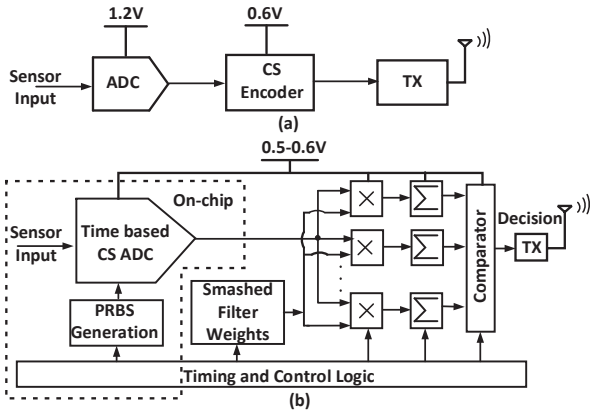

Fig. 1: a) Traditional sensor/classifier interface [1] b) Proposed sensor/classifier interface

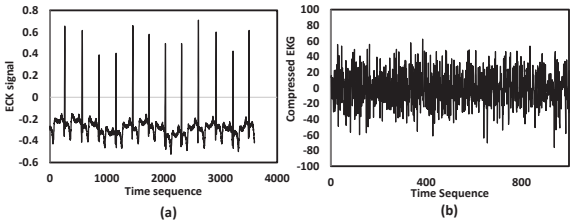

Fig. 2: a) Arrhythmia ECG signal b) Compressed ECG signal with programmable compression ratio

A VCO based ADC is shown in Fig. 3. It consists of a Voltage to Frequency (V to F) converter and Frequency to Digital Converter (FDC). The V to F converter is achieved using a VCO. The FDC is a counter operating at the VCO frequency. Hence, the counter output is proportional to the input Voltage. With the proposed architecture, the sensor front-end can operate at a scaled digital supply. Such a digital ADC is easily portable from one technology to another and easy to interface with the digital back-end circuits. We propose

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a mixed-signal time-based compressed domain (CD) pipeline which includes (1) in-situ random compressive measurements along with A to D conversion and (2) efficiently computing programmable compressive measurements in a time slice, and (3) digital smashed filter based classification with a Winner-Take All (WTA) back-end classifier. The design features a low voltage time based programmable compressive measurement ADC and a digital smashed filter classifier followed by a Winner Take All (WTA) circuit. The proposed hardware, fabricated in $65nm$ CMOS provides reconfiguration between compression ratio and power with a graceful control of energy-accuracy trade-off. Section II describes the mathematical background of smashed filter based object classification. Section III describes the circuit implementation. Section IV describes experimental results and section V concludes the paper.

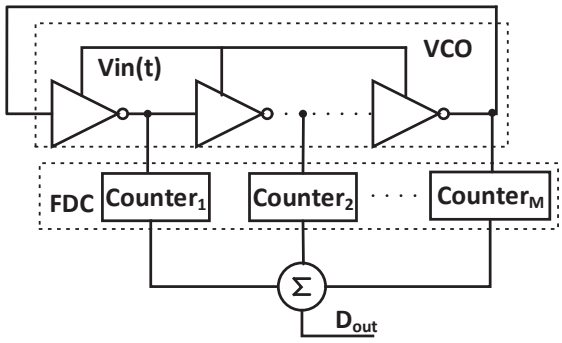


Fig. 3: Traditional VCO based ADC [5]

II. Smashed filter based classification

If we assume an ECG signal recording of N number of samples as $D = D_{i1}, D_{i2}, ..., D_{iN}$ where D_{i1},...,D_{iN} recording indicates the value at each time point. In the compressed domain the distances between the vectors are preserved [10].

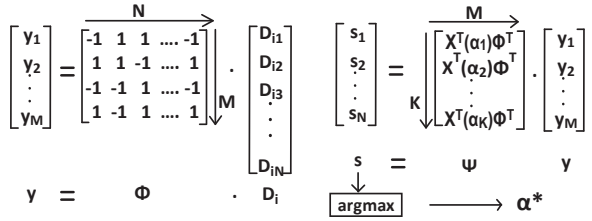


Fig. 4: (a) Compressed Measurements (b) Classification of compressed measurements using smashed filter

To transfer D into the CD, we construct a random matrix Φ of size $M \times N$. Fig. 4 (a) shows the compressed measurements. The compression ratio is given by M/N. Each entry of Φ is uniformly chosen from $\{+1, -1\}$ at random. The projection of the input ECG vector in the compressed domain is calculated as:

$$y = \Phi D \tag{1}$$

Any compressed domain ADC that performs in-situ compression must have multiple inputs or should perform parallel processing (multiple compressive measurements) to reduce the number of conversion cycles [11] [7]. Reported CS front ends, as has been discussed before, operating in the voltage domain suffer from lack of scalability. On the other hand, the proposed time-based CS front end can perform time-based compression with programmable parallel compressive measurements (y_1 to y_M). M is the no. of compressive measurements which is equal to number of parallel processing units. Vectorized K templates as $X(\alpha)$, where α represents the training set elements.

$$\hat{\alpha}^* = \arg\max_{\alpha} X^T(\alpha)\Phi^T.y = \arg\max_{\alpha} \Psi(\alpha)\Phi D \tag{2}$$

The above process is known as smashed filtering [10] which is akin to matched filtering in the CD. It can be decomposed into multiplication with a compression matrix Φ, a smashed filter matrix Ψ (α), followed by WTA (Fig. 4 (b)). The features for Ψ (α) are derived from compressing various segments of ECG signal [12].

III. Hardware Implementation

Fig. 5 (a) shows the proposed differential circuit topology for compressive sensing. The input voltage is fed to a ring VCO. The VCO produces a frequency proportional to the differential input voltage ($V_{in} = V_p - V_n$) and is given by:

$$F_t = K_{VCO} * V_{in}(t) \tag{3}$$

where K_{VCO} is the linearity co-efficient of the VCO. The VCO output drives an up-down 10bit counter. The counter value is proportional to the input voltage. A PRBS sequence acts as the sign for the counter. 0 of PRBS sequence indicates down count and 1 indicates an up counting. The counter in itself acts as an accumulator. The accumulated digital value of the counter for i^{th} measurement (for CR=3) is given:

$$y_i = \sum_{k=1}^{3300} K_{VCO} * \Phi_i(+1, -1) * V_{in}(t_k) \tag{4}$$

where $k = 3300$ is the number of conversion cycles. $V_{in}(t_k)$ is the input voltage at k^{th} interval of time. The VCO phase is fed to M number of counters for parallel compressive measurements.

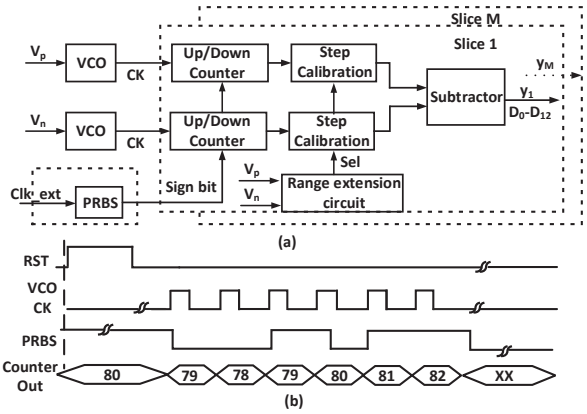


Fig. 5: (a) Proposed differential architecture for compressive sensing using time based technique (b) Timing diagram for the proposed circuit

Parallel Compressive Measurement Fig. 6 illustrates the details of the time based PRBS and input mixing circuit. We convert input voltage to current using a V to I converter. The V to I converter acts as a current source to the VCO. Hence,

the frequency of the VCO is directly proportional to the input voltage in the linear range of the VCO $(250mV - 500mV)$. With M number of PRBS generators and counters we have M different compressive measurements in a given time interval. The matrix multiplication is a true mixed signal (MS) time domain implementation where digital PRBS signals are combined with the absolute value of analog sensor inputs.

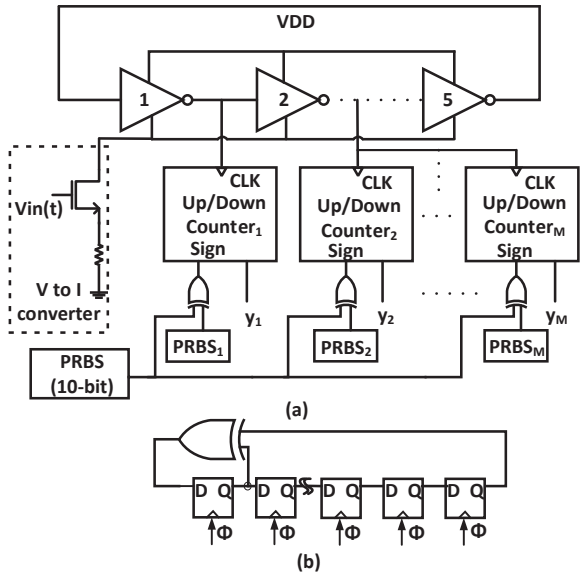


Fig. 6: (a) Time based PRBS and input value mixing circuit (b) PRBS generator

Input range extension:

The range of input voltages over which a VCO is linear is limited. Fig. 7 shows the proposed input range extension circuit. Fig. 8 (a) shows the measured single ended VCO transfer characteristic. The single ended VCO has a linear range of 250mV. Fig. 8 (b) shows the differential VCO transfer characteristic. The differential VCO has a linear range of 400mV. After 700mV on either side the slope of VCO transfer characteristic drastically reduces. Therefore, we propose to scale the output by a factor of 4 based on the input level. The proposed circuit uses a clocked comparator which outputs high if the input voltage goes above 700mV, otherwise it stays at 0. This allows us to avoid the saturation of the VCO and extend the operating range by simply scaling the digital output step. The die photo and chip characteristics are shown in Fig. 9.

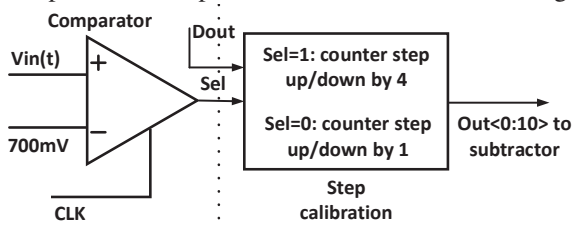


Fig. 7: Input range extension and calibration via scaling of the counter output based on the input level

IV. Experimental Results

Fig. 10 (a) shows the DNL of the proposed CS time-domain ADC. The DNL is less than 1.5LSB. Fig. 10 (b) shows INL

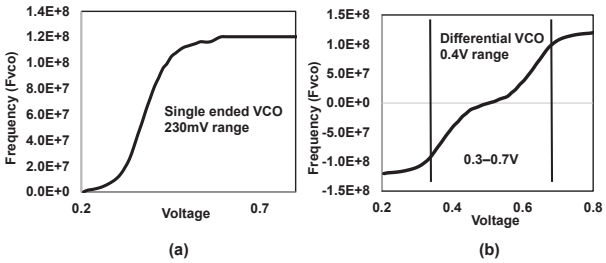
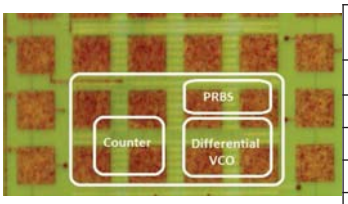


Fig. 8: (a) Measured single ended VCO transfer characteristic (b) Measured differential VCO transfer characteristic



Process	GF 65nm CMOS 8M
Active Area	0.03mm^2
VCO Area	0.003mm^2
PRBS,Counter	0.02mm^2
Packaging	LCC
No. of Pads	32

Fig. 9: Die picture of the chip

of the proposed CS time-domain ADC. The INL is less than 7LSB. High INL is caused for non-linearities of V-I converter and VCO. Even with an INL of 7LSB, we achieve high classification accuracy via a non-linearity aware training and classification, as explained below. Table I shows the power drawn by the various blocks of the proposed ADC at an operating voltage of 0.5V for a single bit slice. The VCO is common for all the slices. For a 250nsec pulse width of PRBS (4MHz of operation), the proposed design has $1.25pJ$ of energy for M=160 parallel processing units. Fig. 11 (a) shows the VCO frequency of 400kHz at 360mV. Fig. 11 (b) shows the VCO frequency of 1.2MHz at 430mV. Fig. 12 (a) shows the digital code vs differential input voltage of the CS-ADC with and without the calibration for range-extension. Without calibration the slope of the curve after 200mV is 4X less compared to slope before 200mV (400mV range). With calibration the slope of the curve after 200mV is comparable to slope before 200mV (600mV range in total). Fig. 12 (b) shows the energy (normalized to the number of parallel multiply and accumulate (MAC) units) and energy (CS for 3300 beats vs no. of parallel processing units). As the number of parallel processing units goes up, the VCO power becomes less significant compared to the counters and the PRBS generators.

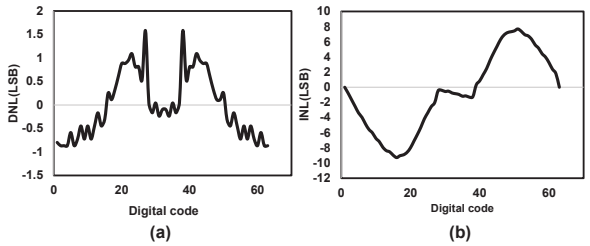


Fig. 10: (a) Measured DNL of the proposed front-end, (b) Measured INL of the proposed front-end

Component	Power
VCO	500nA
Counter	20nA
PRBS	7nA
Adder/Sub-tractor	4nA

TABLE I: Measured power drawn by various components

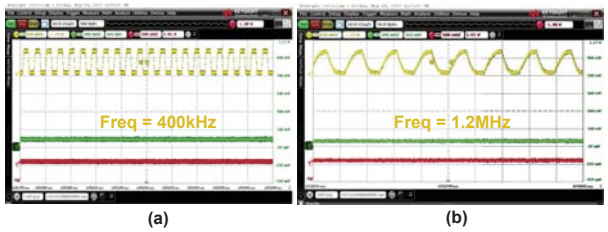


Fig. 11: Scope captures: a) VCO frequency at 360mV b) VCO frequency at 430mV

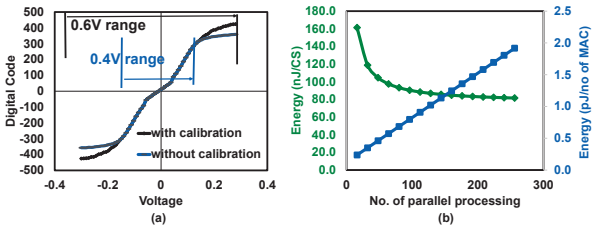


Fig. 12: a) Measured digital code vs differential input (V_{in}) without and with calibration b) Energy (MAC, CS) vs No. of parallel processing units

Fig. 13 (a) illustrates the classification accuracy vs compression ratio. Fig. 13 (b) illustrates energy (nJ) vs compression ratio. At 8x compression ratio the energy is 10.5nJ for classification (with 2.5% accuracy reduction compared to no compression) . Fig. 14 (a) shows proposed technique which includes INL of the ADC while training and testing. Fig. 14 (b) shows classification error vs INL with and without INL-aware training. We can observe that INL aware training maintains error level within 2%. We note that the time-domain computational ADC even with significantly high non-linearity can achieve high accuracy if the training is performed considering the INL. We assume front-end amplifier with gain of 100 to be present before ADC. The proposed design shows competitive figures of- merit in terms of power, lower supply voltage when compared to previously published works on CS encoder (Table. II).

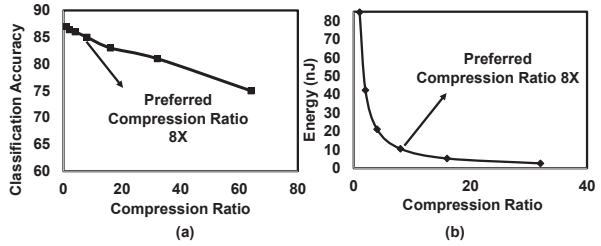


Fig. 13: a) Classification accuracy vs Compression Ratio b) Energy vs Compression Ratio

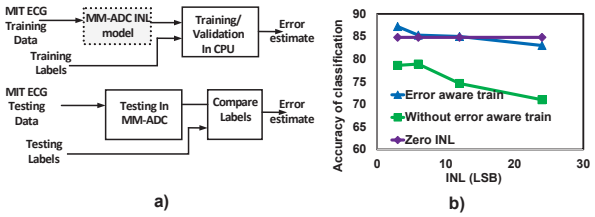


Fig. 14: a) INL aware training and classification b) Classification accuracy vs INL

	Oike [7]	Guo [6]	TCAS-I [5]	TBCAS[1]	This work
System	Image sensing	Radar	EEG Classification	EEG Classification	ECG/EEG Classification
Technology	150nm	130nm	130nm	180nm	65nm
A/D Rate No. of bits	1MHz 12	1MHz 10	NA	20kHz	500kHz 6bits
Supply	1.2V	1V	1V	1V,0.6V	0.5V
No. of parallel processing	1	4	1	Nil	160
Capacitance	NA	272C	NA	516C	0
Power(μW/MHz)	66.3	58	260	13	1.3
Resolution	Analog/12b	Analog/10b	14b	9b	Mixed signal/6b
Area/CS channel	15μm* 15μm	NA	10μm* 15μm	4μm* 200μm	5μm* 50μm

Table II: Comparison with work on compressive sensing

V. Conclusion

This paper presents a ECG classification front end with mixed-signal CS encoder and classification demonstrating an energy-efficiency of 10.5nJ/frame at 8X compression ratio, thus making it suitable for low power sensor front-ends.

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