19.3 A 7nm All-Digital Unified Voltage and Frequency Regulator Based on a High-Bandwidth 2-Phase Buck Converter with Package Inductors

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Conventional processors regulate the supply voltage (V_{DD}) and clock frequency (F_{CLK}) in two separate and independent control loops. A buck converter, switched-capacitor, or low-dropout (LDO) voltage regulator are example control loops for regulating V_{DD} based on a reference voltage (V_{REF}). Processors commonly integrate a phase-locked loop (PLL) to separately regulate F_{CLK} based on a reference clock frequency (F_{REF}), where the F_{CLK} control loop is unaware of the impact of dynamic parameter variations such as V_{DD} droops or temperature changes on the path-timing margin because the PLL voltage-controlled oscillator (VCO) operates on a separate analog voltage. For this reason, conventional processors require either V_{DD} or F_{CLK} guardbands or adaptive and resilient circuits to ensure correct functionality while in the presence of worst-case dynamic parameter variations [1].

Recent work [2-5] combines the regulation of V_{DD} and F_{CLK} in one control loop to reduce the guardbands for V_{DD} and temperature variations, while protecting the processors from path-timing violations. These techniques enable a tight relationship between V_{DD} and F_{CLK}. These previous single V_{DD} and F_{CLK} regulation designs employ either a buck converter [4], an LDO [3], or a switched-capacitor [2], [5] voltage regulator. Today's high-performance SoC processors require the high efficiency of a Buck voltage regulator with a fast-transient response. The design with a Buck converter in [4] uses a large external inductor of 10μH and a large capacitor of 10μF to provide a peak power efficiency of 96.3%, but at the expense of a 20μs settling time for a 90mA load step with a 1ns rise time. Although this design effectively demonstrates high efficiency and guardband reduction with the unified V_{DD} and F_{CLK} control loop, the long settling time during a V_{DD} droop is a major concern for a commercial processor because the V_{DD} droop magnitude may exceed the minimum operating V_{DD} for memory circuits, resulting in failures, and sustained performance degradation of 20μs is unacceptable for some applications. While the design in [4] operates the processor at a faster F_{CLK} after recovering from the V_{DD} droop, this performance loss may exceed the minimum requirements for applications with real-time deadlines. Recent advances of integrating inductors into the package [6] provide an opportunity to significantly improve the transient response for the unified V_{DD} and F_{CLK} control loop during a V_{DD} droop. This paper describes an all-digital unified voltage and frequency buck regulator (UVFBR) with in-package inductors in a 7nm [7] test chip to enable a fast-transient response to V_{DD} droops as required for high-performance processors.

The 7nm test chip (Figs. 19.3.1,19.3.7) contains the UVFBR, performance counters, and a programmable noise generator. The UVFBR design extends the unified voltage and frequency regulator in [3] with a Buck converter, consisting of two in-package inductors. The UVFBR controls both the output clock frequency (F_{OUT}) and output voltage (V_{OUT}) for the digital load in one loop. The UVFBR generates the clock from a tunable-replica circuit (TRC) oscillator and supplies the regulated V_{OUT} to power both the TRC oscillator and the digital load. In the UVFBR control loop, F_{OUT} is divided by a programmable F_{REF} multiplication factor (N) to produce F_{OUT}/N. The UVFBR continuously monitors F_{OUT}/N and adjusts V_{OUT} to lock F_{OUT}/N to a target F_{REF}, resulting in the optimum V_{OUT}. Since V_{OUT} is regulated to achieve a target F_{OUT}, a V_{REF} is not required. F_{OUT} dynamically adapts to V_{OUT} and temperature variations to compensate for delay changes in critical paths to maintain a nearly constant timing margin [1-5]. When a V_{OUT} droop occurs, the TRC oscillator slows down and provides a larger clock cycle time to the load until UVFBR raises V_{OUT} to satisfy the desired F_{OUT}. During a V_{OUT} overshoot, the critical-path delays become faster and compensate for the TRC oscillator speeding up and generating a higher F_{OUT} until UVFBR lowers V_{OUT} back to the nominal value.

The UVFBR includes two 4b Johnson counters with one counter clocked by F_{REF} and the other clocked by F_{OUT}/N. The Johnson counter produces 4 phases of each F_{REF} and F_{OUT}/N. The UVFBR is a 2-phase Buck regulator, with each phase separated by 180°. Each XNOR logic gate produces a signal representing the difference in phase between F_{REF} and F_{OUT}/N to drive the Buck converter output stage to supply the necessary output current load for a target F_{REF}. To avoid phase aliasing associated with the XNOR comparison, the Johnson counter uses an overrun protection (OP) scheme [3]. The OP design holds the Ri value if Li=Ri and propagates the previous stage value (Ri-1) to Ri if Li≠Ri. In addition, the OP holds the Li value if Li≠Ri and propagates the previous stage value (Li-1) to Li if Li=Ri. If F_{OUT} considerably slows down with respect to F_{REF} due to a large load current demand, the phase difference may saturate to 180°, thus increasing the duty cycle to ~100% and maximizing the time for enabling the high side of the output stage. On the contrary, if F_{OUT} speeds up with respect to F_{REF} due to a large V_{OUT} overshoot event, the duty cycle may reduce to ~0%, minimizing the time the high side of the output stage is enabled.

The TRC oscillator enables the interdependent relationship between V_{OUT} and F_{OUT} in the UVFBR. The TRC contains configurable delays to calibrate the oscillator clock period to match the critical-path delay of the digital load (i.e., processor). Each coarse tuning-bit (Coarse_s[3:0]) adjusts the TRC oscillator cycle time by ~30ps, and each small-tuning bit (S[0:12]) adjusts the TRC oscillator by ~4ps resulting in a worst-case timing inaccuracy of ~1.0% at 3.0Ghz. The performance counters allow an on-die measurement of F_{OUT}, which is scanned out of the chip to capture the TRC oscillator frequency. The UVFBR can operate in single-phase mode by either asserting phase1a_select or phase1b_select or in 2-phase mode by asserting both signals. Six programmable noise generators provide the ability to stress UVFBR with variant load currents.

The three-turn inductors (Fig. 19.3.2) are in package and each use six levels of copper metal, where the last three metals constitute the three turns. The simulated DC resistance at room temperature is ~50mΩ and the simulated inductor quality (Q) factor at the UVFBR operating frequencies varies between 17 and 30. Fig. 19.3.3 describes the UVFBR small signal s-domain model. Simulations indicate more than 100° of phase margin at the unity gain bandwidth. While there are two complex poles that sharply drop the phase at high frequencies, these poles are far from the unity gain bandwidth and below -20dB.

The UVFBR is implemented in a 7nm test chip (Fig. 19.3.7). It occupies 6,478μm². To distribute the UVFBR output to the regulated region, the UVFBR components are distributed along the height of the regulated region, thus increasing the effective area to 50,004μm². The area of the package inductors matches the area of the UVFBR regulated region of 639,000μm². Fig. 19.3.4 captures the UVFBR V_{OUT} transition from 0.9V to 0.55V (1.4GHz) in single-phase and 2-phase modes as an example of a dynamic voltage-frequency scaling (DVFS) transition. The settling time is measured at 510ns for the 1-phase mode and 250ns for the 2-phase mode. UVFBR demonstrates a settling time of 60ns and a voltage droop magnitude of 55mV at an F_{OUT} of 2GHz with a current load step from 1mA to 178mA at a rise time of 500ps. This fast-transient response is critical for high performance processors to limit the voltage-droop magnitude and the time while operating at a lower $F_{OUT.}$ Fig. 19.3.5 describes the UVFBR F_{OUT} regulation vs. output load current from 1mA to 900mA with temperature ranging from -15°C to 105°C across 24 dies, demonstrating consistent and highly accurate F_{OUT} regulation for a target F_{OUT} from 1.0GHz to 3.0GHz in steps of 500MHz across a wide range of process, temperature, voltage, and load current. Fig. 19.3.6 plots the measured and simulated power efficiencies for loads between 10mA and 600mA with a 1.6nH inductor, indicating agreement between measurements and simulations. Since the measured peak power efficiency of 60% for a 1.6nH inductor is too low for a processor, simulations indicate that power efficiencies of 90% require an ~10× larger inductor to guide future designs. The small test-chip area allocated and regulated by the UVFBR limits the size of the inductor to 1.6nH and the number of phases to only two. From these simulations, the 1.6nH inductor size limits the measured power efficiency in the UVFFBR implementation. For a high-performance processor, the area is much larger than the test chip area allocated to the UVFBR, therefore allowing for a larger inductor size and/or a greater number of phases to provide acceptable power efficiencies. Fig. 19.3.6 also provides a comparison table with state-of-the-art designs, highlighting the UVFBR fast-transient response.

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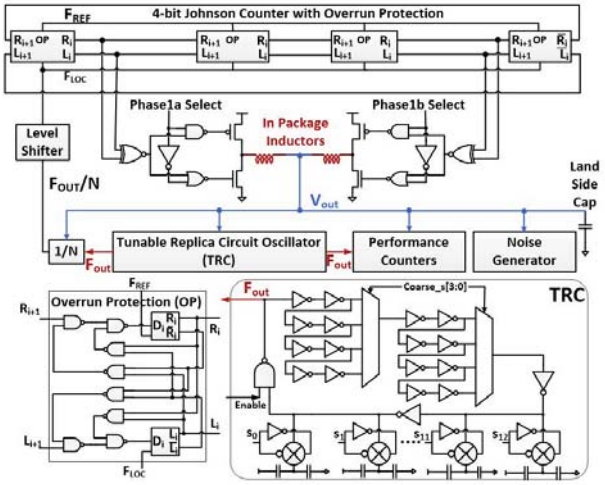


Figure 19.3.1: Test-chip block diagram of the UVFBR with two in-package inductors, performance counters, programmable noise generators, and schematics of the 4b Johnson Counter with overrun protection, and the tunable-replica circuit (TRC) oscillator.

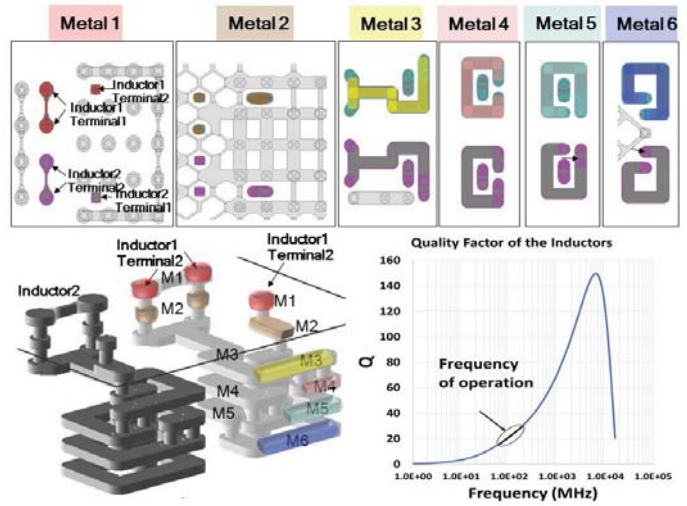


Figure 19.3.2: 3D view of the six metal levels for the two in-package inductors, a detailed view of each metal layer, and the simulated inductor quality (Q) factor. Q ranges from 17 to 30 in the region of operation.

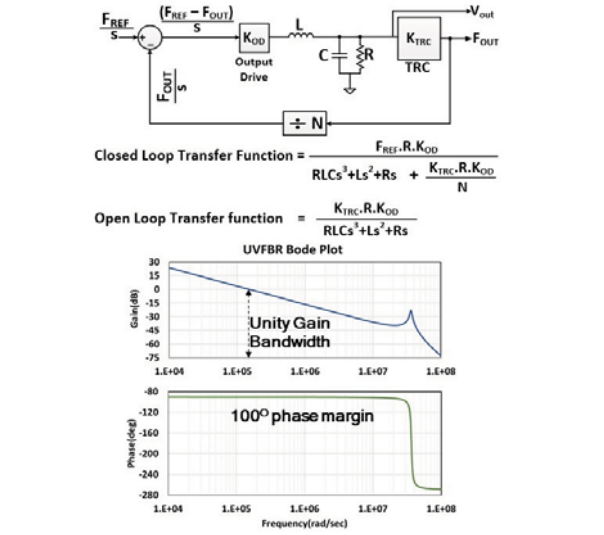


Figure 19.3.3: UVFBR small signal analysis and simulated UVFBR loop gain and phase.

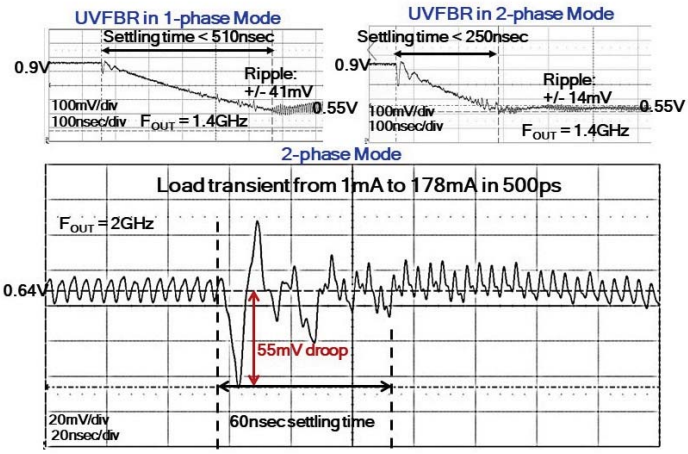


Figure 19.3.4: Measured oscilloscope captures the UVFBR 1-phase and 2-phase modes during a 0.9V to 0.55V (F_{OUT} =1.4GHz) transition and the UVFBR transient response (F_{OUT}=2GHz) in 2-phase with a current load step from 1mA to 178mA at a rise time of 500ps.

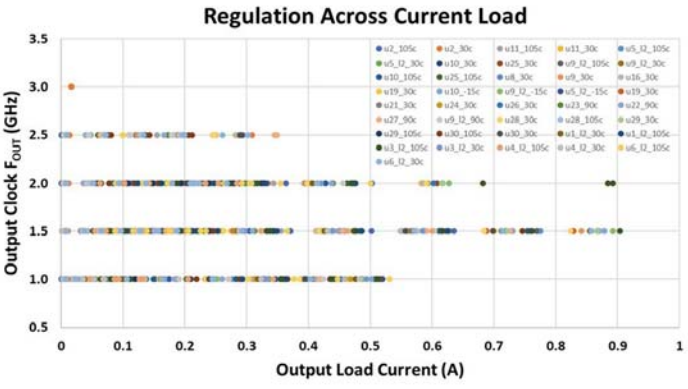
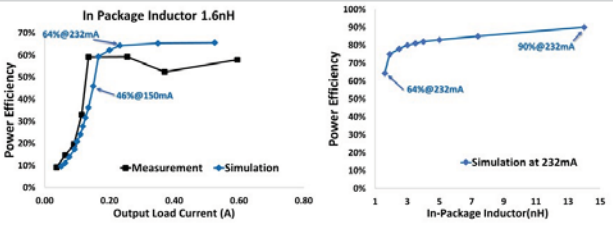
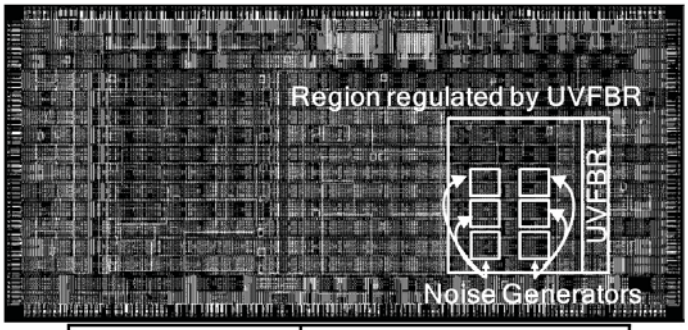


Figure 19.3.5: Measured UVFBR output clock frequency (F_{OUT}) regulation vs. output load current for temperature ranging from -15°C to 105°C across 24 dies.



	[3]	[4]	[5]	This Work
Process Technology	130nm CMOS	65nm	65nm CMOS LP	7nm FinFET CMOS
Input Voltage (V)	0.6 - 1.0	1.2	1.2	1.1-1.3
Topology	LDO	Buck	Switched capacitor	Buck
Output Voltage (V)	0.38 - 0.81	0.6 - 1.0	0.44 - 0.56	0.45 - 0.9
All Digital	Yes	Yes	Yes	Yes
Unified Voltage-Frequency Regulation	Yes	Yes	Yes	Yes
Settling Time (current step)	180ns (3mA/0.5ns)	20,000ns (50mA/ns)	N/A	60ns (178mA/0.5nsec)
Peak Efficiency	99.4% (current efficiency)	96.3%	82.4%	64% with 1.6nH/470nF (measured) 90% with 1nH/47nF (simulated)
I_{out}(mA)	0.1 - 6	1 - 100	N/A	1 - 900
Inductor Technology	N/A	External	N/A	In-Package
Inductor /Capacitor	N/A	10μH/10μF	N/A	1.6nH/470nF

Figure 19.3.6: Measured and simulated UVFBR power efficiency vs. output load current and in-package inductor size and comparison table with other unified voltage-frequency regulation designs.



Technology	7nm FinFET CMOS
Chip Area	8mm^2
TRC Area	48μm^2
UVFBR Area	6,478μm^2
UVFBR Distributed Area	50,004μm^2
Region Regulated by UVFBR	639,000μm^2
Area of Noise Generators	32,571μm^2 X 6

Figure 19.3.7: Test-chip die micrograph and characteristics.

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