A 7nm Leakage-Current-Supply Circuit for LDO Dropout Voltage Reduction

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Abstract

A 7nm leakage-current-supply (LCS) circuit tracks leakage across process and temperature variations and controls PFET block-head switches (BHS) to supply the slow-changing leakage current while an analog low-dropout (LDO) voltage regulator supplies the fast-changing dynamic current to reduce the LDO maximum current demand (I_{MAX}) and minimum dropout voltage ($V_{DO,MIN}$). Measurements demonstrate a 70mV (44%) $V_{DO,MIN}$ reduction, enabling 14-22% power savings.

Introduction

System-on-chip (SoC) processors integrate a limited number of input voltage (V_{IN}) rails due to high costs, where many cores share the same V_{IN}. LDOs [1]-[5] and dedicated phase-locked loops (PLL) allow each core on a shared V_{IN} to employ a unique supply voltage (V_{DD}) and clock frequency (F_{CLK}). The core requiring the highest V_{DD} and F_{CLK} sets the shared V_{IN} value. A core with a lower target V_{DD} and F_{CLK} operates at the lower F_{CLK} to reduce power. If target $V_{DD} \leq V_{IN}$-$V_{DO,MIN}$, the LDO lowers the core V_{DD} to the target V_{DD} to reduce power further. Otherwise, the core V_{DD} operates at V_{IN} via the PFET BHS between V_{IN} and V_{DD} while disabling the LDO. Premium-tier SoC CPU and DSP cores prefer analog LDOs to achieve high bandwidth (BW) for fast-transient response [1]-[2]. Since the LDO bandwidth decreases as the power-PFET width increases in this design (Fig. 1), the maximum V_{DD}-droop specifications limit the power-PFET width. Alternatively, the stability of an output-pole-dominant LDO constrains the power-PFET width. Thus, analog LDOs require a large $V_{DO,MIN}$ of 150-200mV [2]-[3] to supply the core I_{MAX} at worst-case dynamic and leakage conditions. The large $V_{DO,MIN}$ limits LDO usage and is a key challenge with analog LDOs in SoC cores. Although all-digital LDOs reduce $V_{DO,MIN}$, these designs suffer from low gain and high output ripple, thus degrading core performance. Hybrid LDOs [1] employ digital and analog loops to trade-off the strengths and weaknesses of traditional digital and analog designs. The challenge with hybrid LDOs is managing the complex load sharing between the analog and digital loops while maintaining high BW and stability. This paper describes an all-digital LCS circuit in a 7nm [6] test chip to only supply the leakage current to reduce the analog LDO I_{MAX}, and consequently $V_{DO,MIN}$, resulting in higher LDO usage for core power savings [5].

Design and Implementation

Implemented in a 7nm FinFET CMOS technology [6], the test-chip (Figs. 2, 3) features the LCS with a BHS and analog LDO between V_{IN} and V_{DD} to power a CPU IEEE-compliant floating-point multiply-accumulate (MAC) unit, a built-in self-test (BIST), and noise generators. The MAC performs single- and double-precision IEEE floating point multiply, fused multiply-add, and register load/store instructions to represent core functionality. A PLL generates the MAC F_{CLK}.

The LCS (Figs. 2, 4) includes a leakage-current-starved ring oscillator (RO) to generate an RO frequency (F_{RO}) to track leakage, a frequency counter to measure F_{RO}, control logic to map the frequency counter output (CNT_{OUT}) to a BHS configuration (lcs_bhs_cfg) to supply the leakage, and a BHS. The RO contains a NAND gate and 50 inversion-delay stages with each stage consisting of a leakage-current-starved inverter followed by a Schmitt Trigger (ST) to provide a critical hysteresis for increasing the RO-delay dependency on leakage. As the input (a) of the current-starved inverter transitions from 0V to V_{DD}, the output (ab) experiences a charge sharing effect with node mn that quickly changes the ab voltage from V_{DD} to ~$0.7V_{DD}$. The leakage from the bottom NFET slowly completes the ab voltage transition from ~$0.7V_{DD}$ to 0V. Without the ST circuit, the delay dependency on leakage only occurs when ab changes from ~$0.7V_{DD}$ to ~$0.5V_{DD}$ to transition the next inverter stage. A similar effect happens when the input transitions from V_{DD} to 0V. The ST creates a hysteresis to require a larger ab voltage change beyond ~$0.5V_{DD}$ to transition the ST circuit. As a result, the bottom NFET and top PFET leakage currents of the current-starved inverter dominate the stage switching delay to accurately map leakage to F_{RO}. The frequency counter measures F_{RO} over a target delay (e.g., 1ms) and then triggers the control logic to map CNT_{OUT} to lcs_bhs_cfg to supply the leakage. The control logic performs this mapping with look-up tables based on post-silicon characterization of F_{RO} vs leakage and BHS settings vs leakage. The LCS reconfigures the conventional BHS to reduce the area overhead. The analog LDO (Fig. 5) is a symmetrical operational transconductance amplifier followed by a power PFET. With post-layout extraction and no external capacitor, the phase margin is 92° at the unity-gain BW (Fig. 6).

Test-Chip Measurements

From an Advantest 93K production tester, measurements (Fig. 7) demonstrate F_{RO} closely tracking leakage across 30 dies from -15°C to 105°C at 15°C steps (270 data points) at 0.8V. Linear-regression models derived from measurements of F_{RO} vs leakage and BHS settings to supply the leakage for 30 dies from -15°C to 105°C consistently result in an R^2 of 0.99 (Fig. 8). This characterization enables one set of look-up tables for every part to avoid expensive per part calibration.

The worst-case process, temperature, and activity conditions define the $V_{DO,MIN}$ applied to software drivers for every part in commercial SoC processors. At these conditions, leakage is a major contributor to I_{MAX}. From maximum F_{CLK} (F_{MAX}) measurements (Fig. 9), the LDO F_{MAX} vs reference voltage (V_{REF}) remains constant and below the BHS F_{MAX} vs V_{IN} until V_{REF}=0.9V-$V_{DO,MIN}$. At 105°C, LCS reduces $V_{DO,MIN}$ by 70mV. LCS decreases the $V_{DO,MIN}$ variation from 55mV to 10mV (5.5X) and lowers $V_{DO,MIN}$ by 43-50% across V_{IN} (Figs. 10, 11). From measured power (Fig. 12) across target V_{DD}-F_{CLK} states, the MAC operates at the target F_{CLK} while V_{DD} remains at 0.9V unless target $V_{DD} \leq V_{IN}$-$V_{DO,MIN}$, allowing LDO operation at the target V_{DD}. LCS enables a 70mV wider V_{DD} range of LDO usage for 14-22% power savings. From oscilloscope captures (Fig. 13), LCS does not degrade the LDO transient response. Comparison with prior work (Fig. 14) indicates low $V_{DO,MIN}$.

References

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[2] W.-C. Chen *et al.*, *ISSCC*, Feb. 2018, pp. 436-437.
[3] Y. Lu *et al.*, *ISSCC*, Feb. 2014, pp. 306-307.
[4] Y.-J. Lee *et al.*, *ISSCC*, Feb. 2016, pp. 150-151.
[5] S. Gangopadhyay *et al.*, *CICC*, May 2017.
[6] S.-Y. Wu *et al.*, *IEDM*, Dec. 2016, pp. 43-46.

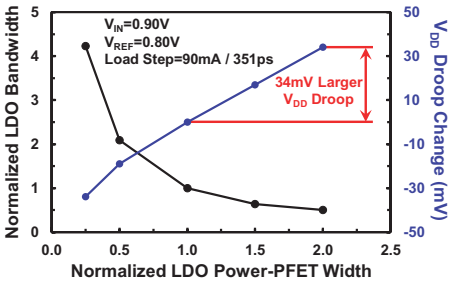


Fig. 1: Simulated analog LDO bandwidth and V_{DD} droop change vs power-PFET width.

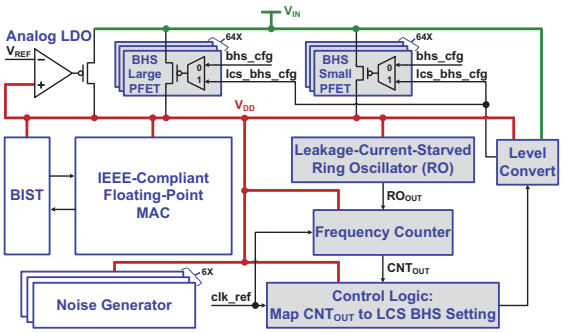
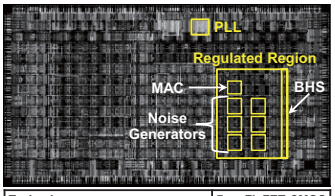


Fig. 2. Test-chip block diagram: LCS integrated with BHS and analog LDO to power a CPU IEEE-compliant floating-point MAC, BIST, and noise generators.



Technology	7nm FinFET CMOS
Chip Area	8mm²
Regulated Region Area	639,000μm²
MAC Area	22,545μm²
Noise Generator Area	32,571μm² x 6
LCS Area	1,014μm²
Leakage-Current-Starved RO Area	154μm²
LDO Area	665μm²

Fig. 3. Test-chip die micrograph and characteristics.

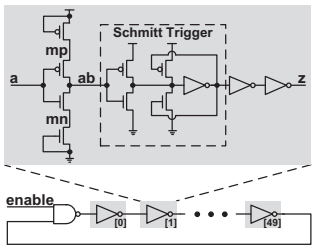


Fig. 4. Leakage-current-starved ring oscillator (RO).

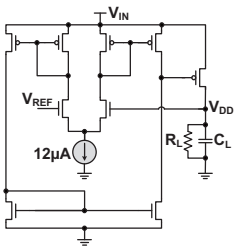


Fig. 5. Analog LDO.

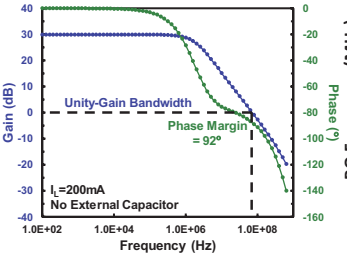


Fig. 6. Simulated analog LDO loop gain and phase.

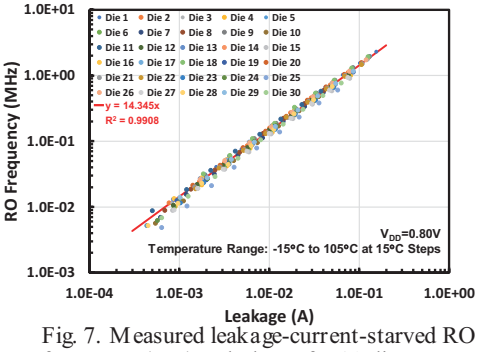


Fig. 7. Measured leakage-current-starved RO frequency (F_{RO}) vs leakage for 30 dies.

V_{DD} (V)	0.85	0.80	0.75	0.70	0.65	0.60	0.55
Slope = RO Frequency / Leakage (MHz / A)	13.237	14.345	15.545	16.872	18.342	20.000	21.913
R^2	0.99	0.99	0.99	0.99	0.99	0.99	0.99

V_{IN} (V) : V_{REF} (V)	0.90 : 0.80	0.90 : 0.75	0.80 : 0.70	0.80 : 0.65	0.70 : 0.60	0.70 : 0.55
Slope = BHS Settings / Leakage (# BHS Large PFETs / A)	153.44	100.87	176.85	117.88	218.01	146.97
R^2	0.99	0.99	0.99	0.99	0.99	0.99

Fig. 8. Slope and R^2 results from linear-regression models derived from measured RO frequency vs leakage across V_{DD} and measured BHS settings vs leakage across V_{IN} and V_{REF} combinations for 30 dies with temperature ranging from -15°C to 105°C.

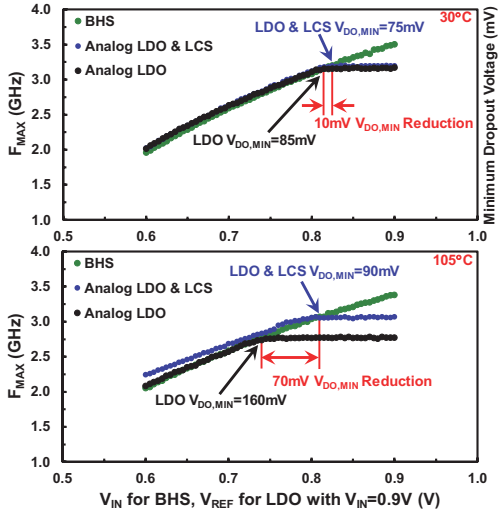


Fig. 9. Measured F_{MAX} for the IEEE-compliant floating-point MAC vs V_{IN} for BHS and V_{REF} for LDO with V_{IN}=0.9V at 30°C and 105°C.

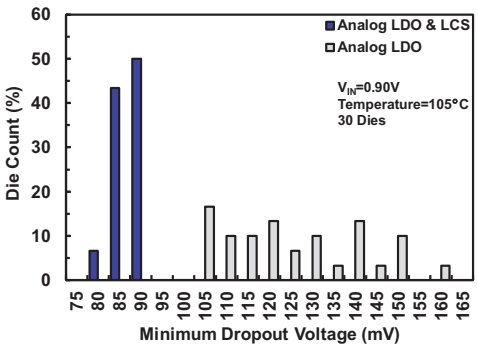


Fig. 10. Measured $V_{DO,MIN}$ distribution for 30 dies.

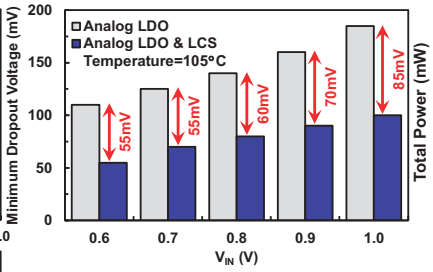


Fig. 11. Measured $V_{DO,MIN}$ vs V_{IN}.

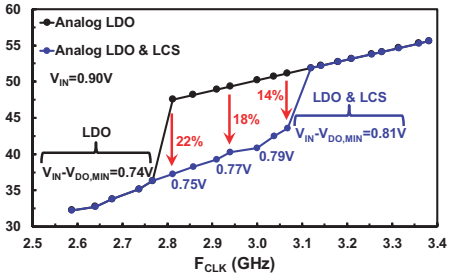


Fig. 12. Measured total power vs F_{CLK}.

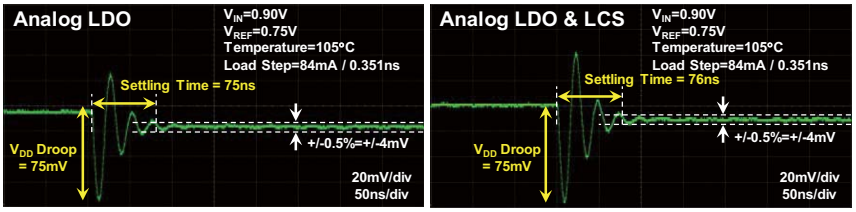


Fig. 13. Measured oscilloscope capture for the analog LDO without and with LCS, demonstrating the LCS does not degrade the LDO transient response.

	This Work	[2]	[3]	[4]
Technology	7nm	150nm	65nm	28nm
LDO Type	Analog with LCS	Analog	Analog	Digital
Input Voltage = V_{IN}	1.00V - 0.60V	1.2V	1.15V	1.1V
Output Voltage = V_{OUT}	0.90V - 0.45V	1.0V	1.0V	0.9V
Additional Capacitor for Stability	None	1,000nF (external)	0.14nF (on-die)	23.5nF (N/A)
Maximum Current Load = I_{MAX}	200mA (V_{IN}=0.9V, V_{OUT}=0.81V)	800mA (V_{IN}=1.2V, V_{OUT}=1.0V)	10mA (V_{IN}=1.15V, V_{OUT}=1.0V)	200mA (V_{IN}=1.1V, V_{OUT}=0.9V)
Quiescent Current = I_Q	53μA	25μA	50μA	110μA
Load Step = ΔI_L / t_{RISE}	84mA / 351ps	800mA / 500,000ps	10mA / 200ps	180mA / 4,000,000ps
Voltage Droop = ΔV_{OUT}	75mV	20mV	43mV	120mV
Settling Time	76ns	N/A	100ns	40,000ns
FOM: Minimum Dropout Voltage	55mV – 100mV	200mV	150mV	200mV

Fig. 14. Comparison with state-of-the-art LDOs.