Non-isolated 48V-to-1V Heterogeneous Integrated Voltage Converters for High Performance Computing in Data Centers
(Invited paper)

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***Abstract*—This paper discusses and compares various topologies of non-isolated 48/1V heterogeneous integrated voltage converters that are potential solutions for future power conversion in data centers. Recent topologies can be divided into three categories: buck and modified buck topologies, switched-capacitor based hybrid topologies, and merged two-stage hybrid topologies. Features, design trade-offs, and outlooks of each topology are discussed.**

Keywords—DC-DC converter, hybrid converter, high voltage converter, 48V-to-1V power conversion

I. Introduction

Over the last 20 years, two-stage power conversion consisting of one 48/12V converter and one 12/1V Point of Load (PoL) converter has been widely used for power delivery in data centers [1] (Fig.1.(a)). However, with the massive increase of power consumption in data centers [2], two-stage solutions are not desirable due to high conduction loss on 12V power bus and large system volume [3]. Compared to 12/1V PoL converters, System in Package (SiP) single-stage 48/1V PoL converters reduce the power bus conduction loss by 16x and increase the overall power density (Fig.1.(b)). Therefore, 48/1V PoL converters have become a promising design choice. However, two key challenges emerge in high voltage converters: (1) a portion of the losses scales with the input voltage (V_{IN}); (2) the ultra-short on-time of high-side (HS) switches limits the operation frequency, which further prevents us from shrinking the system volume (Fig.2). To overcome these issues, conventional 48/1V converters use transformers to bring down the voltage and operate at low frequency to maintain a low switching loss as well as enough on-time control headroom [4]. However, it requires large passives which is not suitable for a desired SiP solution.

In recent years, new non-isolated heterogeneous integrated topologies have been explored. These topologies can be divided into three basic categories: buck and modified buck topologies [5-14]; switched capacitor (SC) based hybrid topologies [15-21]; and merged two-stage hybrid topologies [22,23]. The key factor in these topologies is the utilization of flying capacitors to lower the switching voltage (V_{SW}). Lower V_{SW} results in the following benefits: 1) lower switching loss; 2) extended on-time; 3) lower current ripple; and 4) utilization of better performance switches. The benefits above enable both high efficiency and high integration density. This paper offers a review of these topologies which are potential candidates for SiP 48/1V PoL converters. Since data-center applications demand high power efficiency, for the rest of the paper we will focus primarily on techniques that can improve converter efficiency.

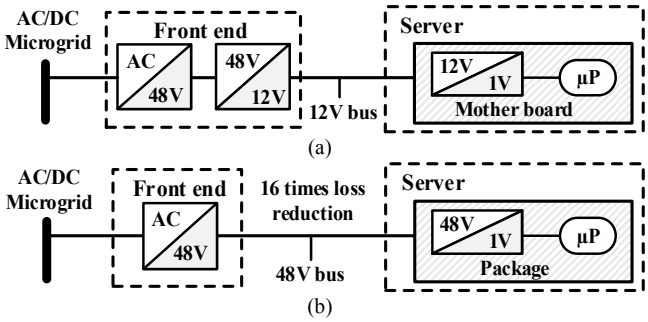


Fig. 1. Current two-stage power conversion (a) and future single-stage power conversion (b) in data centers.

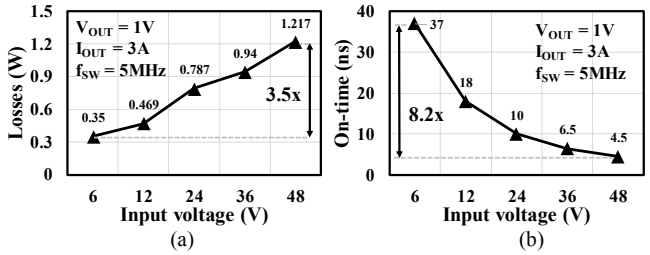


Fig.2. Total losses (a) and on-time of high-side switches (b) scale with V_{IN}. (simulated results of two-phase buck converter)

II. A Survey of Non-isolated High Voltage Converters

A. Buck and Modified Buck Topologies

Synchronous buck converter (Fig.3 (top left)) has been the most popular topology of voltage converters because: 1) the low number of passives enables dense integration, 2) single transistor paths for reduced conduction loss. Deadtime control is essential for this topology: proper deadtime is required for low-side zero voltage switching (ZVS) while non-optimized deadtime increases losses [5]. Deadtime is largely dependent on load current, and adaptive deadtime control techniques have been proposed in [5-9]. HS ZVS can be implemented to improve efficiency, but it requires large current ripple as load current increases [6]. Adaptive zero voltage transition presented in [10] reduces half of the current ripple and can be optimized with load current. Synchronous buck topologies can be improved by incorporating GaN switches at the cost of monolithic integration. However, this topology is limited by its high V_{SW}. Therefore, margins for further improvement are slim.

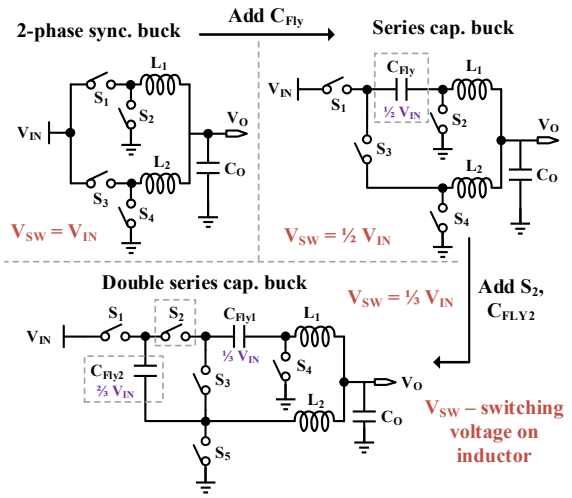


Fig. 3. The buck topology and its modifications: sync. buck (top left), series capacitor buck (top right), and double series capacitor buck (bottom).

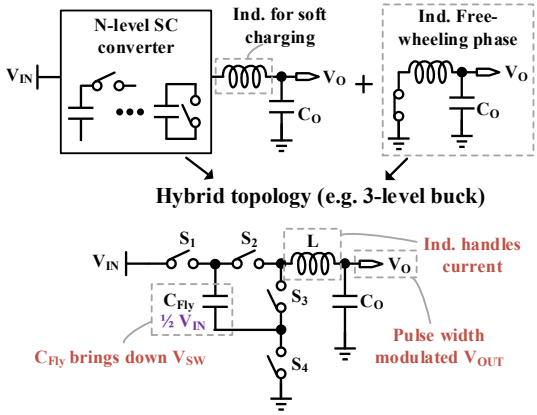


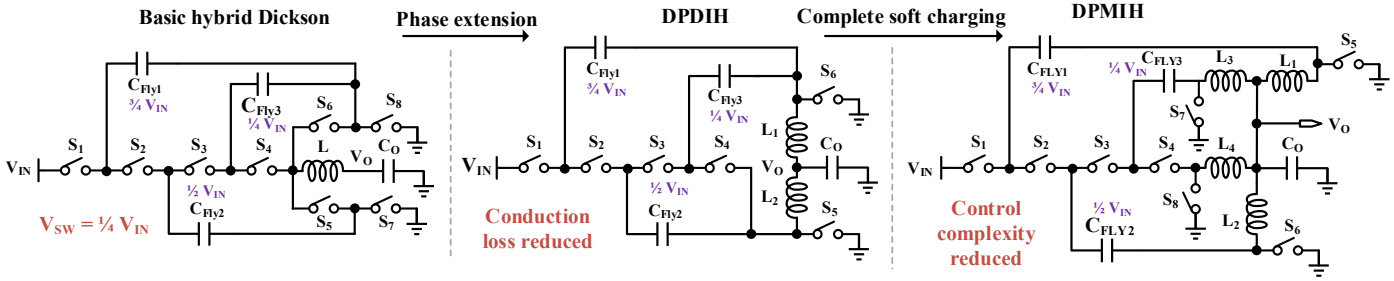
Fig. 4. The evolution of hybrid topologies (top) and the 3-level buck converter (bottom).

Based on synchronous buck converter, series capacitor buck converter adds one flying capacitor to bring down V_{SW} by half (Fig.3 (top right)). Therefore, it has higher efficiency and 2x extended on-time. Moreover, automatic inductor current balancing can be achieved by the flying capacitor. Interested readers are pointed to [11] for further discussions. A master-slave direct 48/1V series capacitor buck converter is presented by [12]. In this architecture, the lower phase is controlled by current mode adaptive on-off time controller while the upper phase is regulated by the lower phase. This avoids the overlap of S_1, S_3 during transient response and eliminates the current sensing mismatch. A peak efficiency of 85.2% at 100KHz has been reported [12]. To further lower the V_{SW}, a double series capacitor converter is presented in [13] (Fig.3 (bottom)). One additional flying capacitor and switch are added enabling one third of V_{IN} at the switching node. However, asymmetric load current distribution appears across L_1 and L_2 in this topology which in turn, increases the conduction loss. In the same lines, a four-phase series capacitor topology is presented in [14]. Series capacitor converters show significant advantages over a fully synchronous buck converter by lowering half V_{SW}. Although they are widely used for 12/1V PoL converters, the reduction of V_{SW} is not enough for 48V V_{IN}.

B. Swtiched-capacitor Based Hybrid Topologies

As discussed above, efficiently lowering the V_{SW} is a key enabler for developing more efficient converter topologies. SC converters have been successful in down conversion with high efficiencies at high input voltage. However, conventional SC converters have two challenges: 1) hard charging, and 2) discrete conversion ratios. Soft charging of SC converters can be achieved by adding inductors to it [15]. Based on that, hybrid topologies add another freewheeling phase of inductors to efficiently utilize the passives (Fig.4). Therefore, SC based hybrid converters can achieve high efficiency by using capacitors to lower the high V_{IN} and inductors to handle the high current.

Based on a 2-to-1 SC converter, three-level buck converter shows high efficiency in low power applications because all switches only see half of V_{IN} [16] (Fig.4 (bottom)). A similar topology can be extended to an N-level flying capacitor multilevel (FCML) converter [17]. Proper control methods are required to balance the voltages on flying capacitors. However, FCML converters have high conduction losses (multi-switches in series) that limit the output current. Among various SC structures, Dickson converter has become a popular choice because: 1) efficient utilization of switches [18], and 2) intrinsic phase duality enabling multi-phase operation. In [19], a 6-level dual-phase dual-inductor hybrid (DPDIH) converter is presented (Fig.5 (middle)). Two inductors achieve two phase interleaved operation which reduces conduction loss, and it uses fewer switches than Dickson converter. However, it needs split-phase control and a capacitor sizing strategy to achieve complete soft charging [18]. DPDIH topology is further enhanced by a dual phase multi inductor hybrid (DPMIH) topology in [20] (Fig.5 (right)). In this work, each flying capacitor is connected to an inductor to achieve complete soft charging and inherent voltage balancing without any additional control. It supports up to 100A and achieves over 90% efficiency. Higher level Dickson converters can be further extended to more phases to support higher current [21].



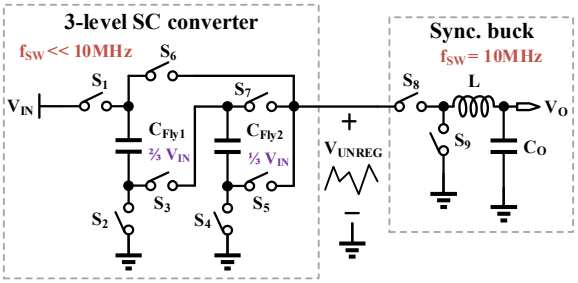


Fig. 6. Merged two-stage topology with unregulated intermediate voltage.

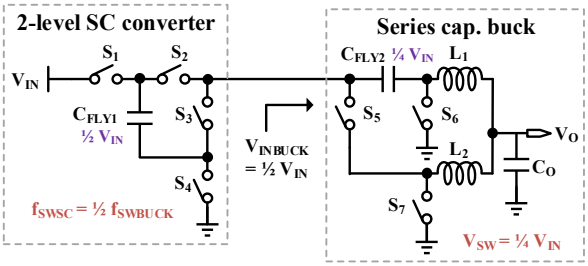


Fig. 7. Merged two-stage topology with series capacitor buck converter as buck stage.

By efficiently utilizing passives, SC based hybrid topologies show promising results. It achieves high efficiency (over 90%) and supports high load current. However, the large number of capacitors and switches increases the system volume and switching losses. Current works are all discrete and operate at low frequency (<500KHz). Transient response and high frequency control remain to be explored. Compared to buck topologies, SC based hybrid topologies are more desirable and have been a subject of intense research recently.

C. Merged Two-stage Hybrid Topologies

From above discussion, SC converters can bring down the voltage efficiently while buck converter is good at regulating the output. Therefore, a converter that makes two stages both working on desired conditions becomes an attractive solution. It is proposed in [22] where the buck converter can serve as a current load between capacitors to achieve soft charging. Therefore, by merging two stages, the SC converter can efficiently bring down V_{SW} and the buck converter can efficiently regulate the output.

In [22], a buck converter is merged into a 3-level SC converter (Fig.6). The SC stage operates at lower frequency to reduce switching losses while the buck stage operates at a high frequency for tight regulation. Therefore, the intermediate voltage is no longer restricted to a small voltage ripple, and the energy stored on capacitors can be more effectively utilized. To overcome variations on V_{IN} of the buck stage, feed-forward control techniques are used to provide high control bandwidth. Moreover, series buck converter also can be used in the buck stage. A tri-state double step down (DSD) converter is proposed in [23] (Fig.7). In this design, a 2-level SC converter serves as the first stage, and the series capacitor buck converter at the second stage further brings down the voltage. This topology achieves 4x lower V_{SW} with only 2 capacitors. As a result, the voltage ripple at the intermediate voltage needs to be controlled.

In summary, as another kind of hybrid topology, the merged two-stage topology shows high utilization of both capacitors and inductors, thus achieves high efficiency as well as fast response. Moreover, the SC stage sees a lower average current than the output load, so silicon devices can be used for denser integration.

III. State-of-The-Art and Simulation Results

Table. I summarizes the state-of-the-art of different high voltage converters. Synchronous buck converter shows high frequency and efficiency at low conversion ratio, but they drop dramatically as conversion ratio increases. Current state-of-the-art hybrid topologies achieve high efficiency, but they have large areas and operate at low frequency. To explore efficiencies of different topologies with GaN switches, SPICE simulations are performed. For fair comparison, ideal pulse width modulator (PWM) and bootstrap circuits are used. The total inductor budget is 400nH, and output capacitor is 500nF. Driver stages use silicon devices from the 180nm BCD process. All converters are operating at 5MHz. The efficiency plot is shown in Fig.8. Due to fixed GaN FETs size, the peak efficiency appears at 5A. ZVS is implemented for buck topologies to improve light load efficiency. Since proper control technique can be used to improve dynamic range, we are focusing on peak efficiency that certain topology can achieve. SC based hybrid topology and merged two-stage topology show 11.6% and 9.8% efficiency improvement by efficiently lowering V_{SW}, respectively. Although apples-to-apples comparisons are difficult, we can summarize the key features and trade-offs in these high voltage PoL converters.

TABLE. I. BENCHMARKING TABLE

	Buck and Modified Buck			SC Based Hybrid			Merged Two-stage Hybrid	
Topology	Sync. buck [5-10]	Series cap. [12]	Double series cap. [13]	Three level [16]	DPDIH [19]	DPMIH [20]	SC+sync. buck [22]	Tri-state DSD [23]
Integration	Hetero. Integ.	Hetero. Integ	Discrete	Hetero. Integ	Discrete	Discrete	Integrated	Integrated
Type of switches	GaN/Si	GaN	GaN	GaN	GaN	GaN	Si	Si
Conversion ratio	4-20	48	48	10	48	48	6.8	24
Peak efficiency (%)	60-90	85.4	91.5	83	93	91	77.5	82
Output current (A)	0.5-4	1.5	30	0.5	10	100	1	3
Power density (W/in^3)	/	/	/	/	225	440	/	/
Frequency (Hz)	2M-40M	2M	500K	2M	300K	167K	10M	1M
On-time (ns)	1.25-75	21	125	100	420	500	45	167
# of switches	2-4	4	5	4	8	8	9	7
Value of inductors (H)	0.5u-1.5u	1.8u	0.9u	1.5u	3u	4u	/	1.1u
Value of capacitors (F)	10u-20u	22u	100u	4.7u	6.8u	/	/	10u
Step-response (s)	20u	8.4u	10u	/	/	/	/	/
Figure of Merit (FoM)*	800-10000	4608	1152	2000	691	384	/	576

*FoM is calculated by: (f_{SW}·V_{IN}·V_{IN})/V_{OUT} (MHz·V) from ISSCC 2017 Forum 1. Higher is better.

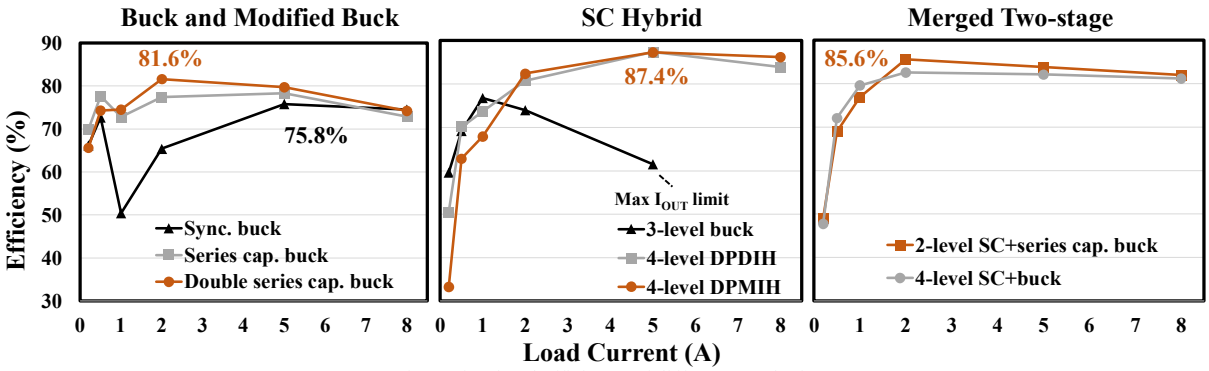


Fig.8. Simulated efficiency of different topologies.

IV. Conclusion

Buck and modified buck topologies are well developed but further improvement is limited. As a new topology, hybrid topology shows its potential of high conversion ratio and efficiency. However, integration and high frequency operation of hybrid topology need to be explored. Finally, merged two-stage hybrid topology shows its flexibility among efficiency, integration, and transient response. In conclusion, bring down V_{SW} efficiently is the key of developing new topologies. A 48/1V converter needs to combine good topology, high-performance switches, and good control schemes to achieve high efficiency, small volume, and fast response.

References

[1] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-Stage 48 V-12 V/6 V-1.8 V Voltage Regulator Module With Dynamic Bus Voltage Control for Light-Load Efficiency Improvement," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5628–5636, Jul. 2017.

[2] S. Oliver, "From 48 V direct to intel VR12. 0: Saving 'big data' $500, 000 per data center, per year," pp. 1–6, Jul. 2012. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/wp_VR12.pdf

[3] M. Ye, P. Xu, B. Yang and F. C. Lee, "Investigation of Topology Candidates for 48V VRM," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf. Expo.*, 2002, pp. 699–705.

[4] X. Zhang, B. Nguyen, A. Ferencz, T. Takken, R. Senger and P. Coteus, "A 12- or 48-V Input, 0.9-V Output Active-Clamp Forward Converter Power Block for Servers and Datacenters," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1721–1731, Feb. 2020.

[5] J. Wittmann, A. Barner, T. Rosahl, and B. Wicht, "An 18 V Input 10 MHz Buck Converter With 125 ps Mixed-Signal Dead Time Control," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1705–1715, Jul. 2016.

[6] A. Barner, J. Wittmann, T. Rosahl1 and B. Wicht, "10 MHz, 48-to-5V Synchronous Converter with Dead Time Enabled 125 ps Resolution Zero-Voltage Switching," in *Proc. IEEE Annu. Appl. Power Electron. Conf. Expo.*, 2016, pp. 106–110.

[7] X. Ke, J. Sankman, M. K. Song, P. Forghani, and D. B. Ma, "A 3-to-40V 10-to-30MHz Automotive-Use GaN Driver with Active BST Balancing and V_{SW} Dual-Edge Dead-Time Modulation Achieving 8.3% Efficiency Improvement and 3.4ns Constant Propagation Delay," *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2016, pp. 302–303.

[8] E. Aklimi, D. Piedra, K. Tien, T. Palacios and K. L. Shepard, "Hybrid CMOS/GaN 40-MHz Maximum 20-V Input DC–DC Multiphase Buck Converter," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1618–1627, Jun. 2017.

[9] X. Ke, and D. B. Ma, "A 3-to-40V V_{IN} 10-to-50MHz 12W isolated GaN driver with self-excited t_{dead} minimizer achieving 0.2ns/0.3ns t_{dead}, 7.9% minimum duty ratio and 50V/ns CMTI," *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2018, pp. 386–387.

[10] Q. Cheng, L. Cong, and H. Lee, "A 48-to-80V Input 2MHz Adaptive ZVT-Assisted GaN-Based Bus Converter Achieving 14% Light-Load Efficiency Improvement," *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2020, pp. 196–197.

[11] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a Buck Converter and a Series Capacitor Buck Converter for High-Frequency, High-Conversion-Ratio Voltage Regulators," *IEEE Trans. Power Electron*, vol. 31, no. 10, pp. 7006–7015, Oct. 2016.

[12] D. Yan, X. Ke, and D. B. Ma, "Direct 48-/1-V GaN-Based DC–DC Power Converter With Double Step-Down Architecture and Master–Slave AO^2T Control," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 988–998, Apr. 2020.

[13] O. Kirshenboim, and M. M. Peretz, "High-Efficiency Nonisolated Converter With Very High Step-Down Conversion Ratio," *IEEE Trans. Power Electron*, vol. 32, no. 5, pp. 3683–3690, May. 2017.

[14] Y. Jang, Milan M. Jovanović, and Y. Panov, "Multi-Phase Buck Converters with Extended Duty Cycle," *Proc. IEEE 21st Annu. Appl. Power Electron. Conf. Expo.*, 2006, pp. 38–44.

[15] Y. Lei, and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," *IEEE Trans. Power Electron*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.

[16] J. Xue, and H. Lee, "A 2MHz 12-to-100V 90%-Efficiency Self-Balancing ZVS Three-Level DC-DC Regulator with Constant-Frequency AOT V^2 Control and 5ns ZVS Turn-On Delay," *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2016, pp. 226–227.

[17] J. S. Rentmeister and J. T. Stauth, "A 48V:2V Flying Capacitor Multilevel Converter Using Current-Limit Control for Flying Capacitor Balance," in *Proc. Annu. Appl. Power Electron. Conf. Expo.*, 2017, pp. 367–372.

[18] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," *IEEE Trans. Power Electron*, vol. 31, no. 01, pp. 770–782, Jan. 2016.

[19] G. Seo, R. Das, and H. Le, "95%-Efficient 48V-to-1V/10A VRM Hybrid Converter Using Interleaved Dual Inductors," in *Proc. IEEE Energy Conversion Congress and Expo. (ECCE)*, 2018, pp. 3825–3830.

[20] R. Das, and H. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," in *Proc. Annu. Appl. Power Electron. Conf. Expo.*, 2019, pp. 1997–2001.

[21] R. Das, G. Seo, D. Maksimovic, and H. Le, "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," in *Proc. Annu. Appl. Power Electron. Conf. Expo.*, 2019, pp. 25–29.

[22] R. Pilawa-Podgurski, and D. J. Perreault, "Merged Two-Stage Power Converter With Soft Charging Switched-Capacitor Stage in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.

[23] K. Wei, Y. Ramadass, and D. B. Ma, "A Direct 12V/24V-to-1V 3W 91.2%-Efficiency Tri-State DSD Power Converter with Online V_{CF} Rebalancing and In-Situ Precharge Rate Regulation," *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, 2020, pp. 190–191.