# Characterization of PVT Variation & Aging Induced Hold Time Margins of Flip-Flop Arrays at NTV in 22nm Tri-Gate CMOS

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***Abstract*— With increasing process variation in scaled technology nodes along with voltage and temperature variations and aging degradations, critical timing circuits are impacted which leads to potential loss of performance and yield. In this paper we study the impact of process induced variations on frequency independent min-delay failures in flip-flops in 22nm tri-gate CMOS and demonstrate through novel test-structures the overall impact of within-die and die-to-die hold time fluctuations across a wide range of process skews, temperatures, voltages and aging conditions. This will guide robust silicon-calibrated statistical design methodologies and process targets for min-delay failure mitigation, especially at near-threshold voltage (NTV). Further we demonstrate local clock driver boosting as a potential scheme for yield improvement at NTV, with only 10-20% boost and minimal overheads.**

## I. Introduction

The impact of process induced variations on failure of memory cells in SRAM arrays is well understood. Tail bits in memory arrays are protected by redundancy and ECC. Next to SRAM, flip-flops (Fig. 1a) by virtue of the inherent contention in the circuit topology present significant design challenges, particularly at NTV. The fact that flip-flops are protected by neither redundancy nor ECC, exacerbates the problem. In particular frequency-independent min-delay failures cause loss of otherwise good-dies or lead to increased logic-$V_{MIN}$ in complex system-on-chip (SoC) designs in scaled CMOS process [1]. Hence, understanding the impact of variations on such min-delay failures is important, but the difficulty of measuring min-delays in process or product characterization

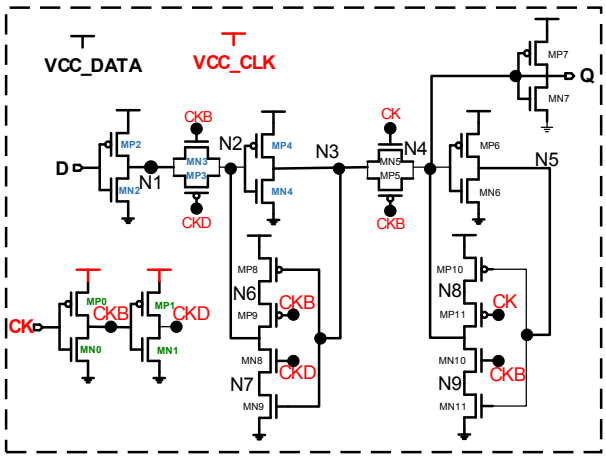


Fig. 1: (a) Schematic of Flip-Flop. Variation in minimum sized transistors MN0, MN1, MP0, and MP1 affects the hold-time and transistors MN2, MN3, MN4, MP2, MP3, and MP4 affects the setup-time. CK is supplied by secondary rail (VCC_CLK) compared to data-path which is supplied by primary rail (VCC_DATA)

continues to be a challenge. In this paper, we present a novel test-structure for high-volume characterization of flip-flops and demonstrate the critical impact of variations and process corners on timing margins in flip-flops.

Min-delay failures can happen due to (1) flip-flop hold time fluctuations, (2) local clock skew degradations and (3) min-

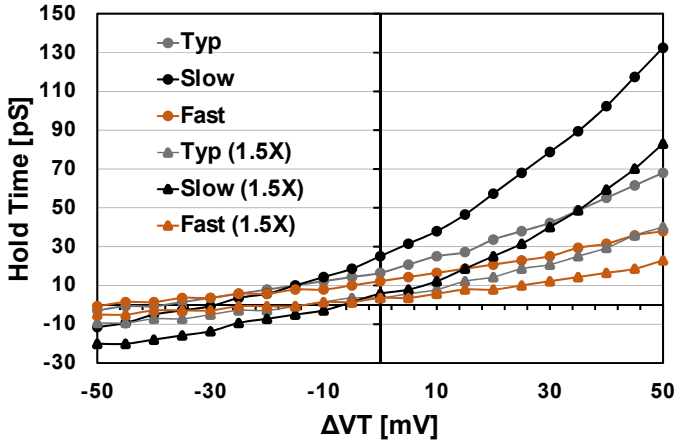


Fig. 1: (b) Hold time as a function of variation in threshold voltage ($V_T$) in transistors in MN0, MN1, MP0 and MP1 across typical (typ), slow and fast process skews at 0.45V, 70degC. Note that sizing (1.5X) of above transistors improves hold-time (simulation)

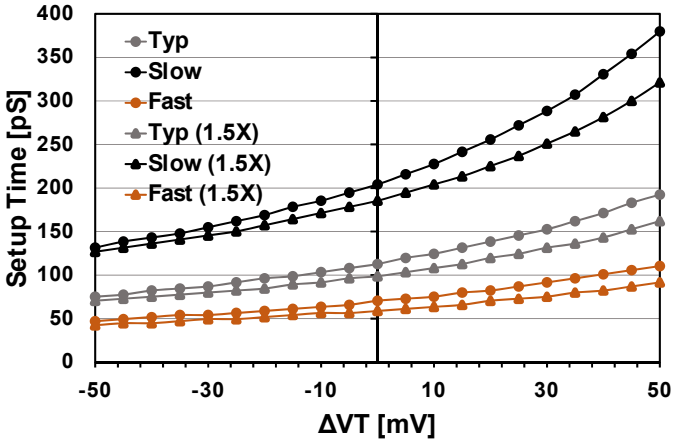


Fig. 1: (c) Setup time as a function of variation in threshold voltage ($V_T$) in transistors in MN2, MN3, MN4, MP2, MP3 and MP4 across typical (typ), slow and fast process skews at 0.45V, 70degC. Note that sizing (1.5X) of above transistors improves setup-time (simulation)

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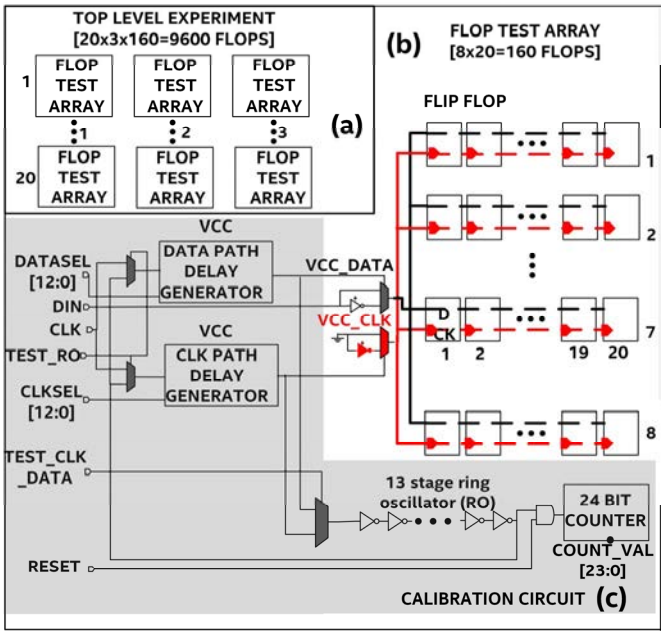



Fig. 2: (a) Test chip block diagram, (b) flip-flop test array, (c) calibration circuit with ring oscillator (RO) and counter

path delay changes, induced by process-voltage-temperature (PVT) variation and aging. While max delay timing failures, limited by flip-flop clock-to-Q & set-up times, clock skew as well as critical path delays, can be mitigated by operating at lower frequency, min-delay functional failures are frequency-independent, thus resulting in functional yield loss that cannot be recovered by operating at lower frequency. Therefore, robust statistical min-delay failure analysis and mitigation techniques, calibrated to high volume silicon measurements, are necessary, especially for near-threshold voltage (NTV) designs [2] since variation and aging impacts become exponentially worse at low voltages. As an illustrative example, Fig.1 (b,c) illustrates the impact of $V_T$ shift on hold, and setup times of flip-flops, respectively. We note that the hold time of flip-flops, which is nominally negative can increase manifold in the slow corners leading to min-delay failures. In this paper, we measure within-die and die-to-die hold time fluctuations in flip-flop arrays implemented in a test chip in 22nm tri-gate CMOS [3] across a wide range of temperatures and voltages, including NTV. Aging impacts on hold time distributions are measured and analyzed. Statistical min-delay failure rates based on the measured data are utilized to guide robust design methodologies at NTV. A local clock-boosting technique to mitigate min-delay failures at NTV with minimal overhead is evaluated via test chip measurements.

## II. Flip-Flop Arrays Test Chip for Hold Time Measurements

The test chip (Figs. 2, 3 & 4) has 20x3 identical flip-flop test array blocks, for a total 9600 flip-flops per die. Each test array contains (1) 8x20 flip-flops, (2) programmable delay generators for both data and clock signals, and (3) a circuit for post-silicon calibration of the delay generators. The calibration is done by using the delayed pulses to enable a 13-stage ring oscillator (RO) and counter. The delay generators are used to independently adjust the timings of data and clock to each flip-flop in the array. A 13-bit digital code, loaded via serial scan, selects the number of inverters in the data and clock path to set the required delay. Binary-weighted tri-state inverters are used in the final two stages of the delay generator to enable finer granularity of delay settings. Measurements demonstrate better than 10ps delay resolution across a wide tuning range (Fig. 3).

Hold time of the flip-flop is defined as the minimum delay required between the rising clock edge that captures data in the slave latch and the next transition of input data, such that the current data is captured correctly. It is governed by the delay mismatch between two local paths (Fig. 1) – (1) input data path to the storage node of the master latch, and (2) clock path that shuts off the master latch. Hence, hold time fluctuations are caused by changes in this delay mismatch due to PVT variations and aging, and are expected to become worse at low voltages. In order to accurately measure hold time fluctuations, we need to change the relative timings of data and clock in a precise manner over a wide range while checking that the correct data is captured [4]. Boosting the voltage of the clock (Fig. 1) to drive selected critical nodes of the flip-flop to higher voltage, can reduce the delay mismatches in the data and clock paths, and thus help mitigate min-delay failures at NTV with minimal power and design complexity overheads.

## III. Hold Time Fluctuation Measurements

Hold time measurements are performed for all 9600 flip-flops on each of several dies, chosen from wafers with typical, slow, and fast process skews. Hold time distribution measurements for a single die show that at lower voltages, mean of the hold time distribution (μ_HOLD) improves but

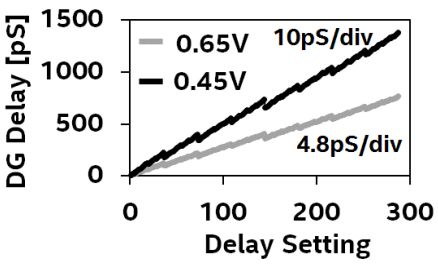
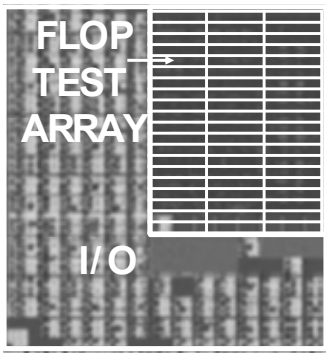



Fig. 3: Delay generator (DG) calibration for 0.45V (larger range) and 0.65V (larger precision)




| | |
|---|---|
| Technology | 22nm, 9-metal layer tri-gate high-K/MG CMOS |
| Area: core + test | 0.83 x 0.9 mm2 |
| Core transistor count | 8.1M |
| Package | FCBGA13 951 |

Fig. 4: Test chip die photo and characteristics table

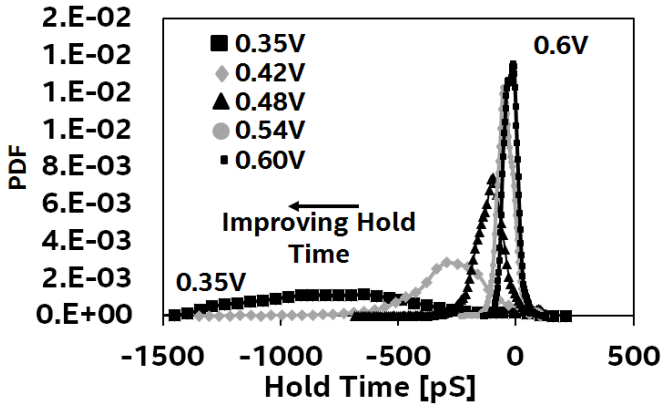



Fig. 5: Probability Density Function (PDF) of hold time with $V_{CC}$ (0.35V to 0.6V) shows that μ_HOLD shifts to the left for low voltages

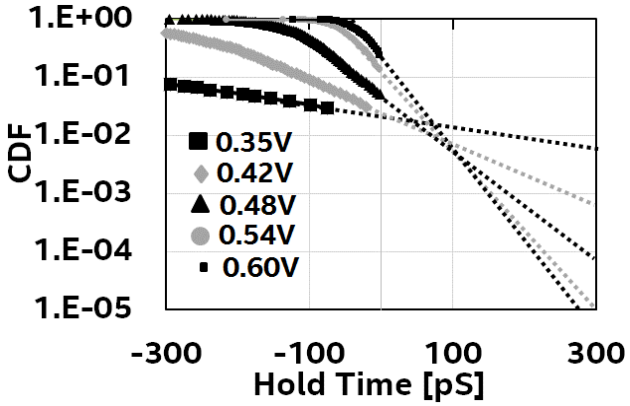



Fig. 6: Cumulative Distribution Function (CDF) of hold time vs. $V_{CC}$ shows that σ_HOLD increases for low voltages

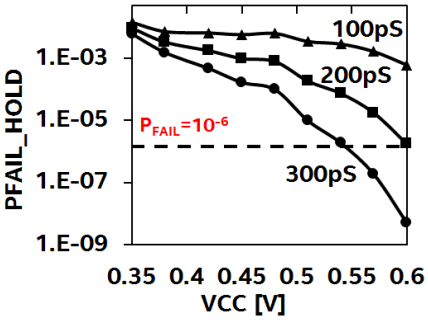



Fig. 7: Probability of min-delay failure (PFAIL_HOLD) vs. $V_{CC}$ for three different data hold times shows that probability of min-delay failure increases at low voltage

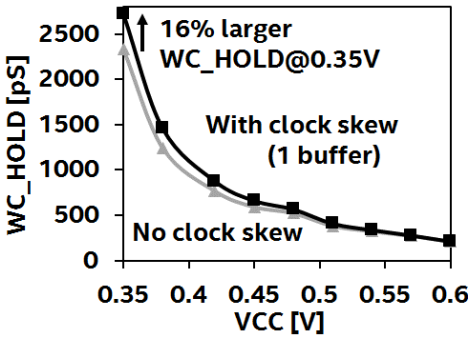



Fig. 8: Worst-case data hold requirement (WC_HOLD) increases for lower voltages with further increase contributed by clock skew

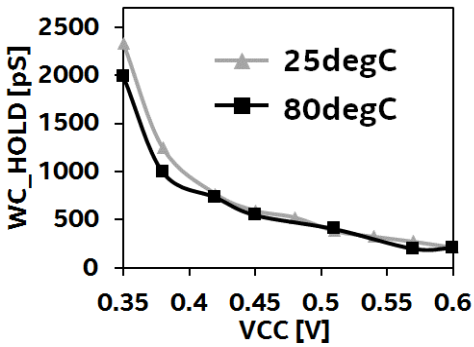



Fig. 9: WC_HOLD at 25ºC and 80ºC shows that low temperature is the hold margin limiter

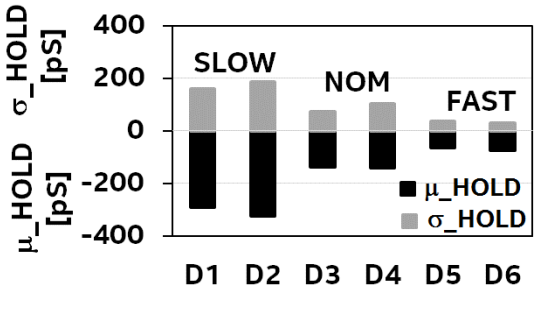



Fig. 10: Die to die variation from 6 dies (2 slow [D1,D2], 2 typical [D3,D4] and 2 fast [D5,D6]) showing variation in μ_HOLD (negative) and σ_HOLD (positive)

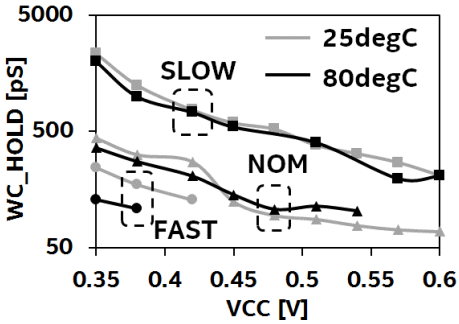



Fig. 11: WC_HOLD vs $V_{CC}$ across skew (slow, typical, fast) and temperature (25ºC and 80ºC)

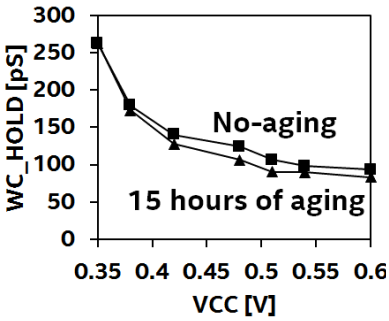



Fig. 12: Aging effect on WC_HOLD showing minimal impact

standard deviation (σ_HOLD) becomes larger (Figs. 5 & 6). Since the worst-case hold time at the tail of the distribution dictates min-delay failure of the entire design, the probability of failure worsens at lower voltages (Fig. 7), as σ degrades, even though the mean improves. For a target maximum failure rate of 1e-6, the minimum data hold requirement increases from 200ps at 0.6V to 300ps at 0.55V. Higher clock skews, expected at lower voltages, also degrade the worst-case data hold requirements (Fig. 8). Measurements show a weak temperature dependence of hold time fluctuations across a

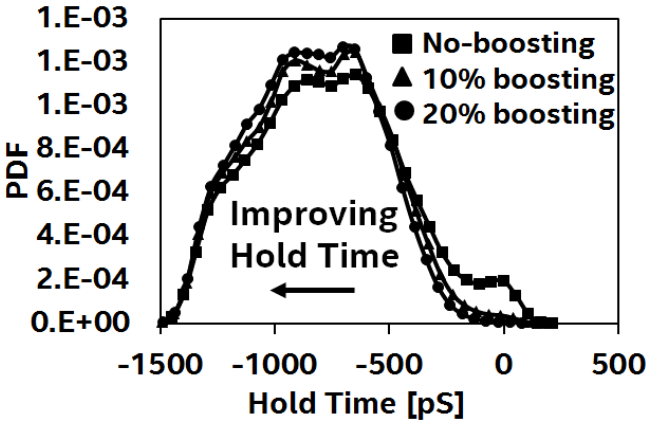



Fig. 13: PDF impact of clock boosting at 0.35V. μ_HOLD shifts to the left and σ_HOLD decreases with boosting

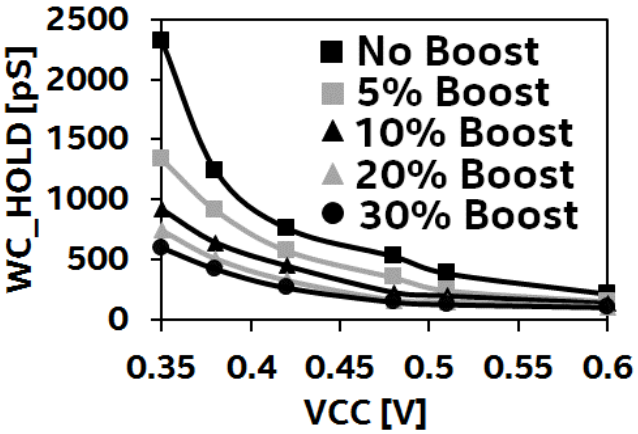



Fig. 14: Clock boosting impact on WC_HOLD

wide voltage range (Fig. 9), with data hold requirements being worse at low temperature, especially at low voltages.

Hold time distributions for different dies across different process skews (Fig. 10) reveal that σ degrades for slower processes where delays are more sensitive to variations, while the mean improves. Overall data hold requirements are the most stringent at the PVT corner of slow process, low voltage and low temperature (Fig. 11). These PVT variation effects need to be comprehended properly in a robust NTV design methodology. While workload and data dependent differences in NBTI/PBTI aging of different transistors in the clock and data paths can degrade delay mismatches, leading to worse hold times and clock skews, test chip measurements show that uniform aging of all transistors has minimal impact on the worst case data hold requirements (Fig. 12).

Design methodologies for min-delay failure mitigation require buffer insertion in short paths and additional clock timing adjustments. The associated performance, power and area overheads may be too high, especially for NTV designs. Measurements show that the local clock driver boosting scheme can significantly improve the worst-case data hold requirements, especially at low voltages, with only 10-20% voltage boost and minimal power impact (Figs. 13-15). This power overhead can be further reduced by potential elimination of some min-delay buffers in short paths. While clock boosting incurs some design overhead, it can be activated selectively (post-Si tuning) only for dies prone to min-delay failures at NTV.

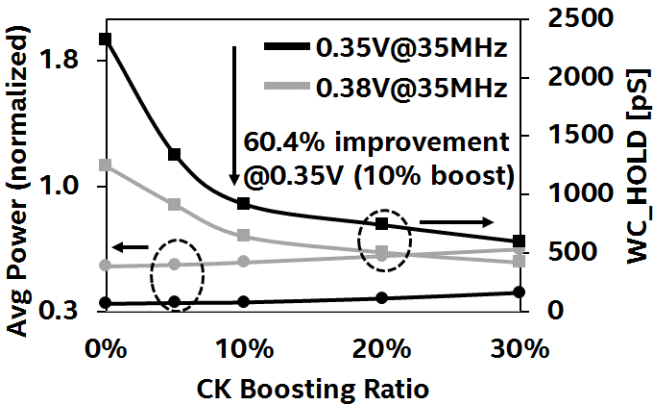



Fig. 15: Power impact of clock boosting

## IV. CONCLUSIONS

In this paper we present comprehensive measurements and methodologies for characterization of failure modes in flip-flops with an emphasis on frequency-independent min-delay failures that can lead to loss of functional yield. We demonstrate the impact of PVT and aging on timing margins through direct measurements on flip-flop characteristics. We also show that local clock-boosting can be a post-silicon NTV technique to mitigate the effects of variation on these margins.


### ACKNOWLEDGMENT

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