# A 65nm 376nA 0.4V Linear Classifier Using Time-Based Matrix-Multiplying ADC with Non-Linearity Aware Training

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***Abstract*—A 6-bit time-based folding matrix multiplication technique for support vector machine (SVM) classification is proposed. A voltage controlled oscillator (VCO) based analog-to-digital converter (ADC) performs in-situ matrix multiplications (MM) along with analog to digital conversion. It also offers a low supply voltage of operation (down to 0.4V) and an input range of 0.8V, drawing a total of 376nA of current. We propose a technique to extend the input range of the VCO based ADC using a folding technique. The classifier is trained considering the non-linearity of the VCO, which results in 5X lower power at iso-accuracy. An accuracy of 93% is achieved with adaboost at the digital back-end with linear SVM as the weak classifier.**

***Index Terms*—time based ADC, dot product, classifier**

## I. Introduction

Embedded sensing applications require machine learning algorithms to perform in-sensor classification [1] [2] to avoid transmission bandwidth and latency to the cloud. Low power and low supply are crucial for sensing and inference. Embedded inference using neural networks, matched filters are gaining importance [1] [3]. There has been extensive work on ADC based in-sensor classifiers reported in [4] [3] [2]. All of the published results so far, demonstrate low-precision computation in voltage domain along with data-conversion. However, the minimum supply required [4] [3] is in the range of 1-1.2V. A lower supply voltage is preferred, if we need to operate the sensors using energy harvesting sources. Also, a low supply voltage is compatible with the traditional digital back-end and is scaling friendly. Due to the scalability and energy-efficiency, VCO based ADC's [5] [6] are gaining more attention. Fig. 1 (a) shows the traditional embedded sensor/classifier interface. In a traditional sensor interface, the ADC operates at a higher supply [4] and digital back end operates at low supply (0.4 - 0.6V). The traditional interface requires two different supply voltages, hence reducing power efficiency. Fig. 1 (b) shows the proposed embedded sensor/classifier interface. We use Adaboost with SVM as the weak classifier. We perform matrix multiplication in time domain and accumulation in digital domain. The accumulated value is compared to a bias value to obtain the results of the weak classifier. Then we perform majority voting and adaboost on the weak classifiers to obtain the final decision.

VCO based ADC consist of Voltage to Frequency (V to F) converter and Frequency to Digital Converter (FDC). V to F converter is achieved using a Voltage Controlled Oscillator (VCO). The FDC is a counter operating at the VCO frequency. However the VCO range is limited and the INL of such a compact ADC is poor. To calibrate the non-linearity digital post processing is typically used and the raw INL of 15-20 LSB reduces to less than a few LSBs. In this paper, we propose a technique to extend the input range and reduce the

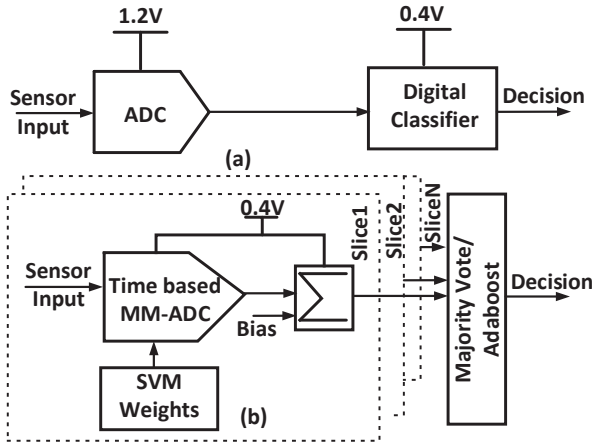



Fig. 1: (a) Traditional sensor/classifier interface (b) Proposed sensor/classifier interface

ADC non-linearity using a folding architecture. The classifier is trained in a manner that accounts for the resultant non-linearity of the ADC and no back-end digital calibration is required. This approach reduces the system power by a factor of more than 5X compared to an ADC with low INL. In the proposed architecture (Fig. 1 (b)) the sensor front-end operates fully at the digital supply.

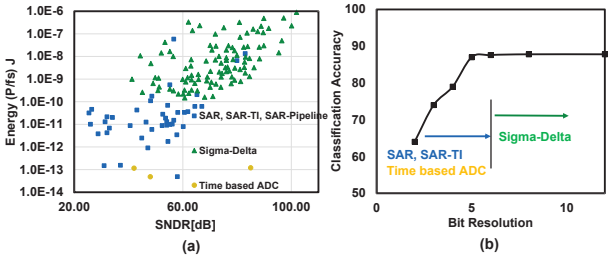



Fig. 2: Choice of ADC for in-situ matrix multiplication

Fig. 2 (a) shows the Energy vs ENOB of the state of the art ADC's. We observe that for low resolution to medium resolution successive approximation (SAR), SAR-TI (time interleaved) and VCO based ADC's have low energy/conversion. Fig. 2 (b) shows the classification accuracy of the MNIST database vs bit width. We can observe that 5-6 bits of datapath are sufficient to achieve the same accuracy as 12 bits. This makes SAR, time based ADC's most suited for embedded classification. Time based ADC's are mostly digital. Porting from one technology to another is easier and they are friendly to both voltage and technology scaling. We propose a time based mixed signal matrix multiplying ADC where : (1) the Digital to time converter produces a pulse proportional to the digital code and (2) the pulse is used to gate the VCO

which produces a frequency proportional to the input voltage (Vin) (3) the counter produces a digital code proportional to the frequency (4) the digital code is compared to a bias value using a compactor to obtain the final decision. We have also analyzed the effect of INL on the classification accuracy of handwritten images from the MNIST database. Section II briefly describes the mathematical background of Adaboost based Support Vector Machine (SVM) as a weak classifier. Section III describes circuit implementation details. Section IV describes experimental results and Section V concludes the paper.

## II. Adaboost with SVM as the weak classifier

SVM is a linear classifier that performs classification based on the hyper-plane or a set of hyper-planes. Support vectors represent data points close to the hyper-plane [7]. The MNIST database has 60,000 training data and 10,000 testing data. The samples are represented by $(X_{i1}, ....X_{iK})$ where K=60,000. Each image can be represented by a sequence of samples as: $(x_{i1}, ....x_{iN})$ where N=784. For M number of weak classifiers, the labels are represented by: $y_1, ...., y_M$. For SVM and the Adaboost classifier, we use:

$$y_t = sgn(w * X_i - b) \quad (1)$$

$$y_f = max(\alpha_1 * y_1 + \alpha_2 * y_2 + ..... + \alpha_M * y_M) \quad (2)$$

Here the sgn operation indicates the sign of the operand, w is the array of support vectors, b is the bias value, $\alpha_i = 1/M$ (where, M=28) and $y_f$ is the final classified label. The hardware implementation of the proposed technique is shown in the Fig. 1 (b). The sensor input is directly fed to the time-based MM-ADC. It is a true mixed-signal matrix multiplier, where the sensor input is an analog signal and the weights are digital values.

## III. Hardware Implementation

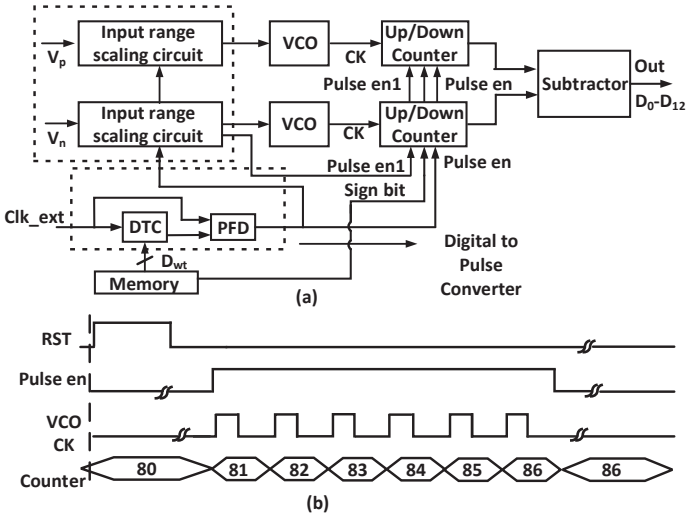



Fig. 3: (a) Proposed pseudo-differential matrix multiplying time-based ADC (b) The corresponding timing diagram

Fig. 3(a) shows the full schematic of the MM-TADC. The frequency of the VCO is directly proportional to the input voltage in the linear range of the VCO. The frequency of the VCO is:

$$F_t = K_{VCO} * V_{in} \quad (3)$$

where, $K_{VCO}$ is the linearity co-efficient of the VCO and $V_{in} = V_p - V_n$ is the differential voltage. From the digital weight stored in the on-chip memory, we convert each digital value into a pulse using a digital-to-time converter (DTC) and a phase-frequency detector (PFD). The DTC receives an external clock reference. The DTC output and the reference clock are fed to the PFD. The PFD produces pulses whose widths are proportional to the digital codes ($D_{wt}$). The DTC along with the PFD forms a digital-to-pulse converter (DPC). The pulse width of the PFD is:

$$P_t = K_{DTC} * D_{wt} \quad (4)$$

The counter gets its clock from the VCO and the enable signal from the PFD output. Since the VCO input is gated with the DPC output, the counter value represents the gated VCO clock. The counter output is:

$$Out1 = K_{VCO} * Vin * K_{DTC} * D_{wt} \quad (5)$$

Eq. 5 shows that the counter output is proportional to the input voltage and the weights ($D_{wt}$). The sign-bit is directly fed to the counter. Since the counter is implemented as an up-down counter, we can naturally add or subtract the input multiplied by the magnitude of the weight, depending on the sign of the weight. The counter inherently is an accumulator. It is initially reset to 80 (hex). This is a mixed signal multiplier in the time-domain where the digital weights are multiplied with the absolute difference value of the analog sensor input.

**VCO design and input range extension circuits:** Fig. 4 shows the proposed VCO and the counter architecture. We convert the input voltage to a current using a V to I converter. The V to I converter acts as a current source to the VCO. Two phases of the VCO are used to the feed two counters. $Counter_1$ gets its enable directly from the PFD output (*Pulse-en*). $Counter_2$ gets its enable from the gated PFD output (*Pulse-en1*). Fig. 5 shows the proposed input range extension circuit. The VCO has a linear range of 250 to 300mV. We propose a technique to extend the range of the VCO. When the input is more than 600mV, we first scale down the input by $2\times$ and perform analog-to-digital conversion. This preserves the linear operating range of the VCO. Finally, the output is scaled up by $2\times$ to obtain the correct digital code. The proposed circuit uses a clocked comparator whose output is high if the input voltage is above 600mV; otherwise it stays at 0. The VCO receives the input voltage or a zero value from the multiplexer, depending on the *Pulse en* signal from the DPC. Output scaling is achieved as: (a) If the input is less than 600mV, one counter is used to count the VCO frequency (*Pulse-en* always enabled, *Pulse-en1* disabled). (b) Otherwise, two counters are used to count the VCO frequency (*Pulse-en1* is now enabled).

**Digital-to-Pulse converter:** The Digital-to-pulse converter (DPC) consists of a DTC followed by a PFD. Fig. 6 (b) shows the proposed DTC. It consists of a chain of four delay cells. Each delay cell is a cascade of two inverter cells (Fig. 6 (a)), where one inverter has a programmable capacitance as the load. An unit capacitance, $C_0$ of 10fF is implemented. The DTC receives an external clock. The output of the DTC is represented by CLKD. The delayed clock and the original clock are fed

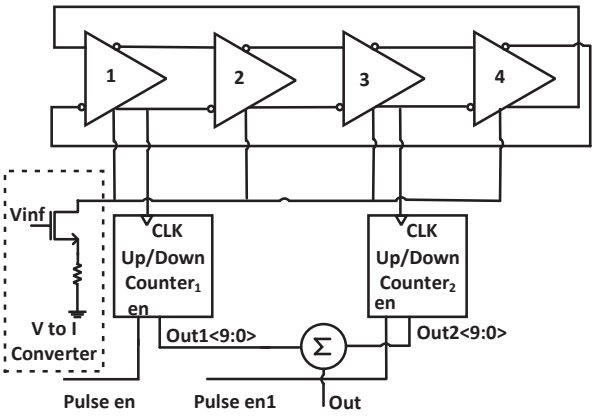



Fig. 4: A single ended VCO along with the output counter

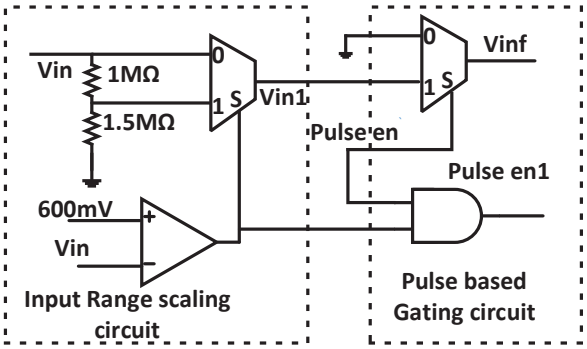



Fig. 5: Input dependent scaling of the output code achieves input range extension

to a PFD. The PFD produces a pulse which is proportional to the delay between CLK and CLKD (Fig. 6 (c)). The test-chip is implemented in 65nm CMOS. We have implemented a bit-slice of the design and input for characterization is serially streamed in for system level analysis. The die photo and the chip characteristics are shown in Fig. 7.

## IV. Experimental Results

Fig. 8 (a) shows the traditional training procedure for classification of the MNIST database. The VCO based ADCs have low-power but poor INL performance. Here we show that the training can be aware of such non-ideality. Fig. 8 (b) shows the proposed training procedure for the MNIST classification. The proposed technique comprehends the non-linearity (INL) error included in the matrix multiplication. This error-aware model is used for training and testing (Fig. 8 (c)) the MNIST images. This error-aware technique helps to improve the accuracy of the classification. Fig. 9 (a) shows the measured single-ended VCO transfer characteristics. The single ended VCO has a linear range of 250mV. Fig. 9 (b) shows the VCO transfer characteristics with the range extension technique. The proposed extended-range differential-VCO has an input range of 800mV.

Fig. 10 (a) shows the DNL of the proposed MM-TADC. The DNL is less than 1.5LSB. Fig. 10 (b) shows the INL of the proposed MM-TADC. The INL is less than 7LSB. Fig. 11 (b) shows the classification accuracy with and without the

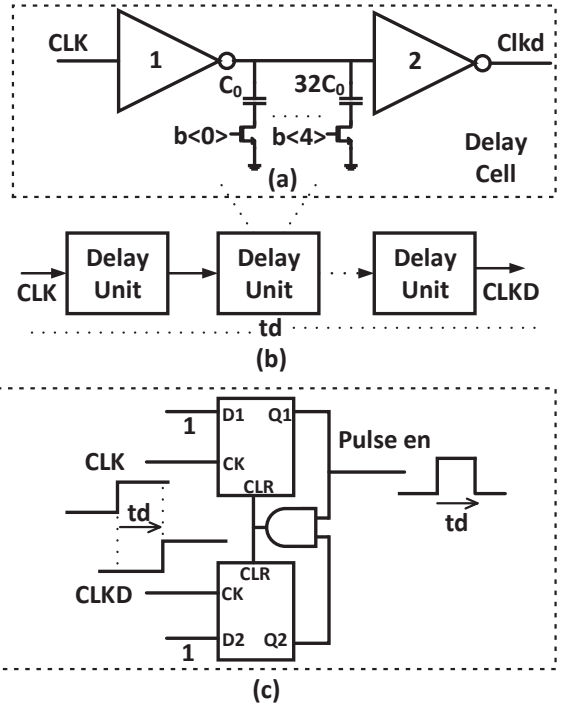
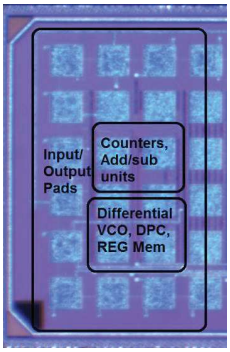



Fig. 6: Digital to pulse converter (DPC) for pulse generation




| Process | GF 65nm CMOS 8M |
|---|---|
| Active Area | 0.03mm$^2$ |
| VCO Area | 0.0042mm$^2$ |
| Packaging | LCC |
| No. of Pads | 32 |

Fig. 7: Die shot and chip characteristics

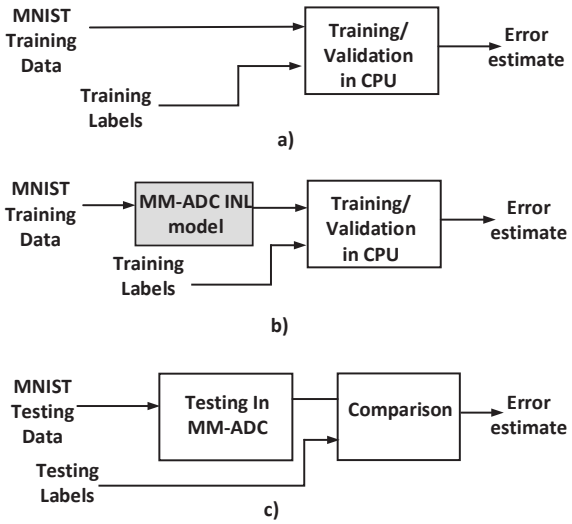



Fig. 8: (a) Traditional training procedure (b) Proposed INL aware training and (c) Testing for accuracy of inference

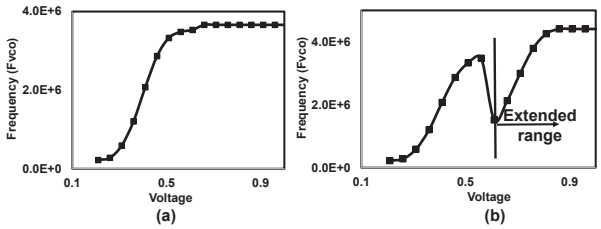



Fig. 9: Measured: (a) Single ended VCO transfer characteristic (b) Folded VCO transfer characteristic with high input range

INL error-aware training. We can observe that without error-aware training, the classification error goes up with increasing INL. However, with INL error-aware training, the classification error remains within a $\pm$2-3% margin. The ADC energy per step scales as $2^{2*ENOB}$. Here, ENOB of 5.3 can achieve the same accuracy as an 8 bits with a large INL. With the proposed circuit we achieve more than 5X reduction in power using the TD ADC. Fig. 11 (a) shows the digital code vs the differential input voltage for the proposed circuit. We can observe that after 600mV, the range gets extended. This is achieved by the the proposed folding architecture before the VCO. Fig. 12 (a) and (b) show the captured VCO output and the DPC output with a pulse width of 400ns.

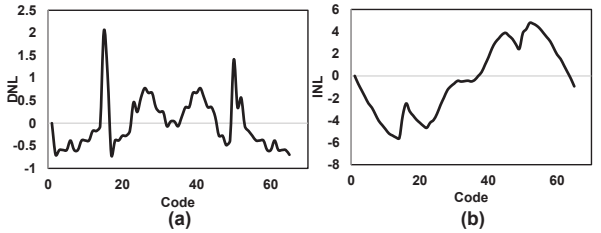



Fig. 10: (a) Measured DNL of the proposed front-end (b) Measured INL of the proposed front-end

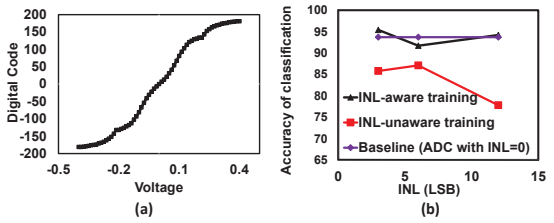



Fig. 11: (a) Digital code vs differential input voltage (b) Classification accuracy for a baseline design and TD ADC based design with and without error aware training

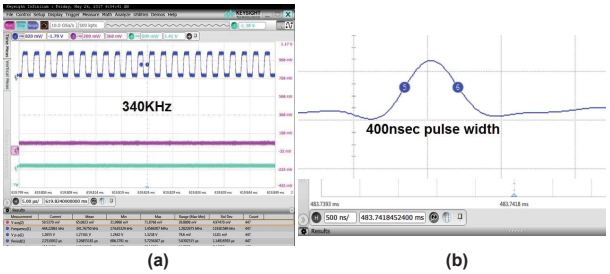



Fig. 12: (a) Scope capture of the VCO frequency at 360mV (b) Zoomed-in scope-capture of the DPC output

| Component | Power |
|---|---|
| VCO | 360nA |
| Counter | 40nA |
| DPC | 80nA |
| Adder/Sub-tractor | 16nA |
| Total | 376nA |

TABLE I: Power drawn by various components

Table I shows the power drawn by various blocks of the proposed MM TADC. For a 700ns pulse width of the DPC, energy/MAC is 1.47pJ. For $28*28$ image size with 60 support vectors the estimated total energy is 313nJ. For Adaboost with 26 weak classifiers, the energy/classification is 8.1$\mu$J. Table II shows the comparison with previously reported results [4] [8] [3]. [4] [8] perform matrix multiplication in the voltage domain. The amplifier used in [8] requires a 1-1.2V supply. The measured energy of our work is comparable to reported results and it uses a digitally scalable architecture enabled by time-based processing.

| | ISSCC 2015 [4] | ISSCC 2016 [3] | ISSCC 2017 [8] | ASSCC 2016[1] | **This work** |
|---|---|---|---|---|---|
| System | Object/ECG detection | Object detection | Spatial Filtering | Image Classification | **Image Classification** |
| Technology | 130nm | 40nm | 65nm | 28nm | **65nm** |
| A/D Rate<br>ENOB<br>D/A Rate | 20kS/s<br>7Bits<br>N/A | 39MS/s<br>5-7bits<br>1GS/s | NA<br>14bits<br>1.5MHz | 2.4MHz<br>8 bits | **500kHz**<br>**5.4 bits**<br>**-** |
| Multiplication domain | Voltage mode | Voltage mode | Voltage mode | Voltage mode | **Time based** |
| Analog/Digital Supply | 1.2V | 1.1V | 1V | 1V | **0.4V** |
| Input range | 0.6V | 0.5V | 1V | 1V | **0.8V** |
| Power(µW/MHz) | 66.3 | 0.228 | 260 | 3 | **0.46** |
| Energy (pJ/MAC) | 16 | 0.12 | 2 | 3.2** | **1.47** |
| Classification accuracy | 87% | - | 89% | NA | **93%** |

**Table II. Comparison with table reported works** **Off-chip Accumulator

## V. Conclusion

This paper presents a time-based matrix multiplying technique. At 0.4V, the energy per classification for the SVM is 313nJ/frame. The proposed training technique which is aware of the INL of the ADC and achieves high classification accuracy.

## VI. Acknowledgements

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