A 90.4% Peak Efficiency 48V/1V Three-Level Hybrid Dickson Converter with Gradient Descent Run-time Optimizer and GaN/Si Hybrid Conversion

Minxiang Gong\textsuperscript{1}, Xin Zhang\textsuperscript{2}, Arijit Raychowdhury\textsuperscript{1}
\textsuperscript{1}Georgia Institute of Technology, \textsuperscript{2}IBM T. J. Watson Research Center

Abstract

This work presents a 48V/1V DC-DC Point-of-Load (POL) converter for efficient high voltage conversion in data centers. The converter includes (1) a three-level hybrid Dickson topology with GaN/Si hybrid conversion achieving efficient flying capacitor (C\textsubscript{F}) utilization. (2) A gradient descent run-time optimizer finding optimal switching frequency (f\textsubscript{SW}) and number of fingers turned on (N\textsubscript{F}) during converter’s operation. (3) A 10bit hybrid ADC for current sensing. The test chip is fabricated in 0.18\mu m BCD process and shows a 90.4% peak efficiency at 48V/1V conversion with a 240 A/inch\textsuperscript{2} current density.

Introduction and Motivation

Data centers are moving to the 48V power bus from conventional 12V. Therefore, direct 48V-to-1V point of load (POL) converters become popular. Recently, hybrid topologies [1]-[5] gain interest, which overcome high voltage stress and small duty ratio in the half bridge topology. However, first, prior works adopt N-1 C\textsubscript{F} to reduce max voltage on the switching node (V\textsubscript{SW}) N times, which increases component count and hurls the power density. Second, recent works only focus on the peak efficiency and ignore the operation range of load current (I\textsubscript{L}). This work proposes a three-level hybrid Dickson converter achieving efficient utilization of both power switches and C\textsubscript{F} with a run-time gradient descent optimizer for efficiency enhancement across a wide range of I\textsubscript{L}.

Three-Level Hybrid Dickson Topology

Recent work [2] proposes a tri-state double step-down topology achieving efficient C\textsubscript{F} utilization shown in Fig. 1. However, the max switching node voltage (V/4V\textsubscript{IN}) is not well-suited for 48V input, and a flying capacitor voltage (V\textsubscript{CF}) rebalancing technique is required. Inspired by [2], this work proposes a three-level hybrid Dickson topology (Fig. 1). By replacing the DSD topology with a five-level hybrid Dickson topology, the proposed topology has following features: (1) it reduces max V\textsubscript{SW} 10x and extends the duty ratio 10x with only five C\textsubscript{F} and 11 switches—a 54% and 21% reduction compared to [5]. (2) it has inherent V\textsubscript{CF} balancing which eliminates additional controls. C\textsubscript{F2}-C\textsubscript{F5} are balanced by inductors as described in [1],[2],[3],[4], C\textsubscript{F1} is balanced by C\textsubscript{F2}-C\textsubscript{F4} as shown by equations in Fig. 1. (3) To avoid C\textsubscript{F} hard charging in Dickson structure, an additional inductor L\textsubscript{1} is used to split C\textsubscript{F5} out from L\textsubscript{1} [6] for soft charging. The L\textsubscript{3} enables three phase operation which reduces output voltage (V\textsubscript{O}) ripple and support higher I\textsubscript{O}. Fig. 2 shows our analysis on efficiency versus frequency and gate drive loss, necessitating the run-time optimizer. First, the max efficiency occurs at different f\textsubscript{SW}. Second, when I\textsubscript{O} is low, the conduction loss (P\textsubscript{C}) is less than 12% of the total loss. Turning on all fingers of Si switches wastes large amount of drive power (10s of mW) and has limited P\textsubscript{C} reduction. Therefore, a run-time optimizer of f\textsubscript{SW} and N\textsubscript{F} is proposed.

System Architecture and Circuit Implementation

Fig. 3 shows the proposed converter system architecture, and the colored area indicates the die. The converter uses two off-chip GaN switches (S\textsubscript{1}, S\textsubscript{2}), nine on-chip Si LDMOS (S\textsubscript{3}-S\textsubscript{11}), forming a hybrid conversion [5]. Drive signals are generated from a 12bit digital PWM with a resolution of 156ps. S\textsubscript{3}-S\textsubscript{6} and S\textsubscript{8}-S\textsubscript{9} require high voltage level switches to accomplish high voltage gate driving. To have a precise power loss estimation, a 10bit hybrid ADC with a differential amplifier is proposed for sensing L\textsubscript{1}’s average current (I\textsubscript{L1}) when S\textsubscript{1} is turned on. The 10bit current information along with the 12bit on-time (t\textsubscript{ON}) are sent to a gradient descent run-time optimizer. The optimizer calculates the power loss at each step and compares it with the optimal f\textsubscript{SW} and N\textsubscript{F}. The f\textsubscript{SW} is controlled by a frequency divider capable for 4bit frequency tuning (0.52-4.4MHz). The 9x3bit N\textsubscript{F} of S\textsubscript{3}-S\textsubscript{11} are sent to finger scalable gate drivers for driving Si switches. The output voltage is quantized by a 6bit SAR ADC and a digital PID controller is responsible for V\textsubscript{O} regulation. The circuit schematic of 10bit hybrid ADC and block diagram of the gradient descent run-time optimizer are shown in Fig. 4. The V\textsubscript{I} and V\textsubscript{0} indicating I\textsubscript{L1} are first converted by a 5bit SAR ADC. Then, the residual voltages on capacitors of the SAR ADC are directly sent to tail transistors of two voltage-to-time converters (VTC). Since the difference of residual voltages are small (~62.5mV), the VTC shows good linearity within such small input range. The difference between residual voltages is converted by a 5bit time-to-digital converter (TDC). Compared to conventional pipeline ADC, the proposed design eliminates intermediate amplifiers by reusing voltages on capacitors, which reduces area/power overhead. The 10bit I\textsubscript{L1} is sent to a power loss calculator to estimate the power loss (P\textsubscript{LOSS}). The equation of P\textsubscript{LOSS} is shown in Fig. 4. Besides I\textsubscript{L1}, I\textsubscript{ON} also provides information of input power (P\textsubscript{IN}), which overcomes noise in the current sensing circuit. To optimize both f\textsubscript{SW} and N\textsubscript{F}, an iterative gradient descent method is used. The f\textsubscript{SW} optimizer performs gradient descent starting from the lowest f\textsubscript{SW} and stops at each step waiting for N\textsubscript{F} optimizer to find the optimal N\textsubscript{F}. Starting from the highest N\textsubscript{F} that all fingers are turned on, the N\textsubscript{F} is subtracted each time until its gradient becomes positive. Then, N\textsubscript{F} and P\textsubscript{LOSS} are sent to f\textsubscript{SW} optimizer for remaining process. At each step of f\textsubscript{SW} or N\textsubscript{F}, the hybrid ADC starts conversion after PID controller is stabilized to ensure accurate I\textsubscript{L1} sensing. Thus, the run-time optimizer finds the global minimum for both f\textsubscript{SW} and N\textsubscript{F} without interoperating converter’s operation. Conventional level shifters face challenges of speed and reliability in high conditions. The proposed high-speed digital-assisted level shifter is shown in Fig. 5. It uses diode clamping for fast transition and current mirrors for symmetric pull-up/pull-down time. However, first, during the transition, I\textsubscript{X} and I\textsubscript{Y} copied from I\textsubscript{X} and I\textsubscript{Y} by current mirrors charge V\textsubscript{F} and V\textsubscript{X} to high. Second, in steady state, small currents I\textsubscript{X} and I\textsubscript{Y} discharge V\textsubscript{F} and V\textsubscript{X} gradually. To avoid output flipping, a digital logic is used to lock the output. Compared to conventional cascaded level shifter, it shows high speed (~1ns) with a smaller area (195x65\mu m\textsuperscript{2}).

Measurement Results

The test chip is fabricated in 0.18\mu m BCD process with an area of 4.3mm\textsupersquare (Fig.6). Fig. 7 shows measured switching node waveform. The switching node voltages shift between 0V-4.8V, validating the proposed topology. In the large timescale, switching node voltages are stable indicating voltages on all flying capacitors are balanced. Measured efficiency is shown in Fig. 8. This work achieves 90.4% and 87.2% peak efficiency at 48V-1V and 48V-0.7V, respectively. The small figure in Fig. 8 shows efficiency improvement with proposed run-time optimizer. Fig. 9 shows P\textsubscript{LOSS} and f\textsubscript{SW} at different I\textsubscript{L}. At low I\textsubscript{L}, switches are soft switched (with fixed dead-time) so f\textsubscript{SW} is increased to reduce excessive ripple current (I\textsubscript{ripple}) on inductors. As I\textsubscript{L} increases, N\textsubscript{F} becomes larger for reduced P\textsubscript{C} while f\textsubscript{SW} is reduced for lower switching losses (P\textsubscript{SW}). Measured transient response is shown in Fig. 10. A 120mV voltage droop and 20\mu s response time is measured at a load step of 1A/\mu s. Fig. 11 shows measured current sensor accuracy with proposed hybrid ADC. The ideal resolution is 2mA, and the average error is within 9. Table I shows the comparison with state-of-the-art.

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References

 fig. 1. Proposed three-level hybrid Dickson topology and features.

Fig. 2. Motivation for the run-time optimization of switching frequency and number of fingers.

Fig. 3. Converter system architecture with on-chip Si device, off-chip GaN, digital regulation loop and run-time gradient descent optimizer.

Fig. 4. Diagram of 10-bit hybrid ADC and run-time optimization of fSW and Nf with iterative gradient descent.

Fig. 5. High-speed digital-assisted level shifter.

Fig. 6. Die shot and board.

Fig. 7. Measured switching waveform.

Fig. 8. Measured efficiency.

Fig. 9. Optimization results.

Fig. 10. Transient response.

Table 1. Comparison of state-of-the-art.