A 90.4% Peak Efficiency 48V/1V Three-Level Hybrid Dickson Converter with Gradient Descent Run-Time Optimizer and GaN/Si Hybrid Conversion

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Abstract

This work presents a 48V/1V DC-DC Point-of-Load (POL) converter for efficient high voltage conversion in data centers. The converter includes (1) a three-level hybrid Dickson topology with GaN/Si hybrid conversion achieving efficient flying capacitor (C_F) utilization. (2) A gradient descent run-time optimizer finding optimal switching frequency (f_{SW}) and number of fingers turned on (N_F) during converter's operation. (3) A 10bit hybrid ADC for current sensing. The test chip is fabricated in 0.18μm BCD process and shows a 90.4% peak efficiency at 48V-1V conversion with a 240 A/inch^3 current density.

Introduction and Motivation

Data centers are moving to the 48V power bus from conventional 12V. Therefore, direct 48V-to-1V point of load (POL) converters become popular. Recently, hybrid topologies [1]-[5] gain interest, which overcome high voltage stress and small duty ratio in the half bridge topology. However, first, prior works adopt N-1 C_F to reduce max voltage on the switching node (V_{SW}) N times, which increases component count and hursts the power density. Second, recent works only focus on the peak efficiency and ignore the operation range of load current (I_O). This work proposes a three-level hybrid Dickson converter achieving efficient utilization of both power switches and C_F with a run-time gradient descent optimizer for efficiency enhancement across a wide range of I_O.

Three-Level Hybrid Dickson Topology

Recent work [2] proposes a tri-state double step-down topology achieving efficient C_F utilization shown in Fig. 1. However, the max switching node voltage (¼V_{IN}) is not well-suited for 48V input, and a flying capacitor voltage (V_{CF}) rebalancing technique is required. Inspired by [2], this work proposes a three-level hybrid Dickson topology (Fig. 1). By replacing the DSD topology with a five-level hybrid Dickson topology, the proposed topology has following features: (1) it reduces max V_{SW} 10x and extends the duty ratio 10x with only five C_F and 11 switches – a 54% and 21% reduction compared to [5]. (2) it has inherent V_{CF} balancing which eliminates additional controls. C_{F2}-C_{F5} are balanced by inductors as described in [1],[2] and [4]. C_{F1} is balanced by C_{F2}-C_{F4} as shown by equations in Fig. 1. (3) To avoid C_F hard charging in Dickson structure, an additional inductor L_3 is used to split C_{F5} out from L_1 [6] for soft charging. The L_3 enables three phase operation which reduces output voltage (V_O) ripple and support higher I_O. Fig. 2 shows our analysis on efficiency versus frequency and gate drive loss, necessitating the run-time optimizer. First, the max efficiency occurs at different f_{SW}. Second, when I_O is low, the conduction loss (P_C) is less than 12% of the total loss. Turning on all fingers of Si switches wastes large amount of drive power (10s of mW) and has limited P_C reduction. Therefore, a run-time optimizer of f_{SW} and N_F is proposed.

System Architecture and Circuit Implementation

Fig. 3 shows the proposed converter system architecture, and the colored area indicates the die. The converter uses two off-chip GaN switches (S_1, S_2), nine on-chip Si LDMOS (S_3-S_{11}), forming a hybrid conversion [5]. Drive signals are generated from a 12bit digital PWM with a resolution of 156ps. S_1-S_3, and S_5-S_8 require high voltage level shifters to accomplish high voltage gate driving. To have a precise power loss estimation, a 10bit hybrid ADC with a differential amplifier is proposed for sensing L_1's average current (I_{L1}) when S_1 is turned on. The 10bit current information along with the 12bit on-time (t_{ON}) are sent to a gradient descent run-time optimizer. The optimizer calculates the power loss at each step and compares them to find the optimal f_{SW} and N_F. The f_{SW} is controlled by a frequency divider capable for 4bit frequency tuning (0.52-4.4MHz). The 9x3bit N_F of S_3-S_{11} are sent to finger scalable gate drivers for driving Si switches. The output voltage is quantized by a 6bit SAR ADC and a digital PID controller is responsible for V_O regulation. The circuit schematic of 10bit hybrid ADC and block diagram of the gradient descent run-time optimizer are shown in Fig. 4. The V_L and V_O indicating I_{L1} are first converted by a 5bit SAR ADC. Then, the residual voltages on capacitors of the SAR ADC are directly sent to tail transistors of two voltage-to-time converters (VTC). Since the difference of residual voltages are small (<62.5mV), the VTC shows good linearity within such small input range. The difference between residual voltages is converted by a 5bit time-to-digital converter (TDC). Compared to conventional pipeline ADC, the proposed design eliminates intermediate amplifiers by reusing voltages on capacitors, which reduces area/power overhead. The 10bit I_{L1} is sent to a power loss calculator to estimate the power loss (P_{LOSS}). The equation of P_{LOSS} is shown in Fig. 4. Besides I_{L1}, t_{ON} also provides information of input power (P_{IN}), which overcomes noise in the current sensing circuit. To optimize both f_{SW} and N_F, an iterative gradient descent method is used. The f_{SW} optimizer performs gradient descent starting from the lowest f_{SW} and stops at each step waiting for N_F optimizer to find the optimal N_F. Starting from the highest N_F that all fingers are turned on, the N_F is subtracted each time until its gradient becomes positive. Then, N_F, and P_{LOSS} are sent to f_{SW} optimizer for remaining process. At each step of f_{SW} or N_F, the hybrid ADC starts conversion after PID controller is stabilized to ensure accurate I_{L1} sensing. Thus, the run-time optimizer finds the global minimum for both f_{SW} and N_F without interoperating converter's operation. Conventional level shifters face challenges of speed and reliability in high conditions. The proposed high-speed digital-assisted level shifter is shown in Fig. 5. It uses diode clamping for fast transition and current mirrors for symmetric pull-up/pull-down time. However, first, during the transition, $I_{X\text{-}C}$ and $I_{Y\text{-}C}$ copied from I_X and I_Y by current mirrors charge V_P and V_N to high. Second, in steady state, small currents $I_{X\text{-}S}$ and $I_{Y\text{-}S}$ discharge V_P and V_N gradually. To avoid output flipping, a digital logic is used to lock the output. Compared to conventional cascoded level shifter, it shows high speed (~1ns) with a smaller area (195x65μm^2).

Measurement Results

The test chip is fabricated in 0.18μm BCD process with an area of 4x3mm^2 (Fig.6). Fig. 7 shows measured switching node waveform. The switching node voltages trip between 0V-4.8V, validating the proposed topology. In the large timescale, switching node voltages are stable indicating voltages on all flying capacitors are balanced. Measured efficiency is shown in Fig. 8. This work achieves 90.4% and 87.2% peak efficiency at 48V-1V and 48V-0.7V, respectively. The small figure in Fig. 8 shows efficiency improvement with proposed run-time optimizer. Fig. 9 shows N_F and f_{SW} at different I_O. At low I_O, switches are soft switched (with fixed dead-time) so f_{SW} is increased to reduce excessive ripple current (I_{ripple}) on inductors. As I_O increases, N_F becomes larger for reduced P_C while f_{SW} is reduced for lower switching losses (P_{SW}). Measured transient response is shown in Fig. 10. A 120mV voltage droop and 20μs response time is measured at a load step of 1A/μs. Fig. 11 shows measured current sensor accuracy with proposed hybrid ADC. The ideal resolution is 2mA, and the average error is within 9. Table I shows the comparison with state-of-the-art.

Acknowledgement

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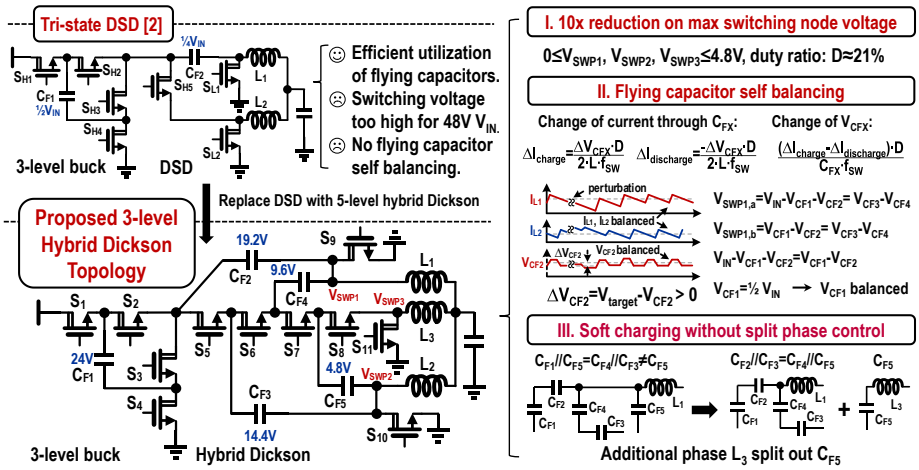

Fig. 1. Proposed three-level hybrid Dickson topology and features.

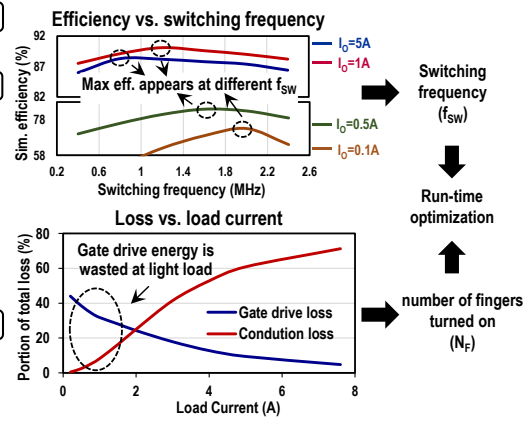

Fig. 2. Motivation for the run-time optimization of switching frequency and number of fingers.

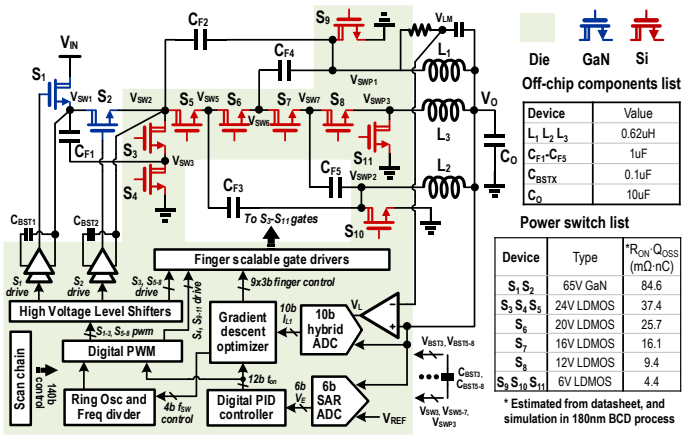

Fig. 3. Converter system architecture with on-chip Si device, off-chip GaN, digital regulation loop and run-time gradient descent optimizer.

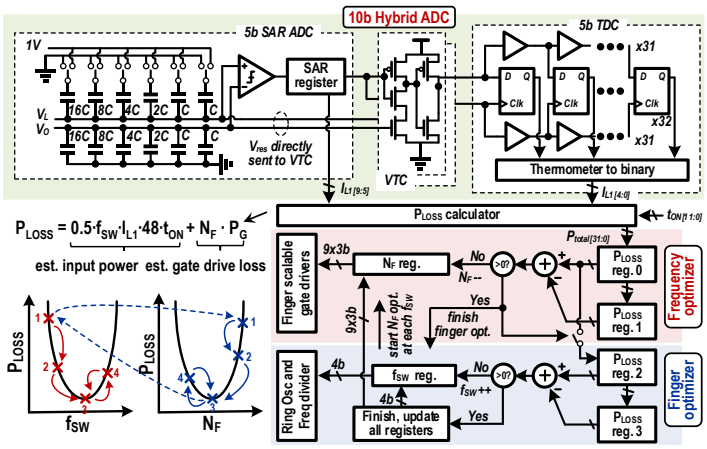

Fig. 4. Diagram of 10bit hybrid ADC and run-time optimization of f_{SW} and N_F with iterative gradient descent.

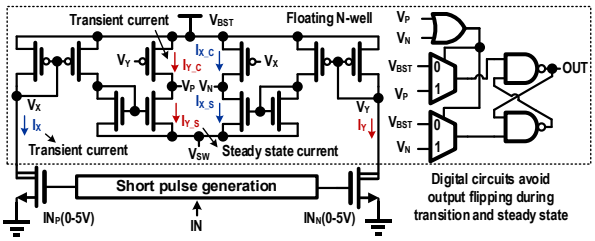

Fig. 5. High-speed digital-assisted level shifter.

Fig. 6. Die shot and board.

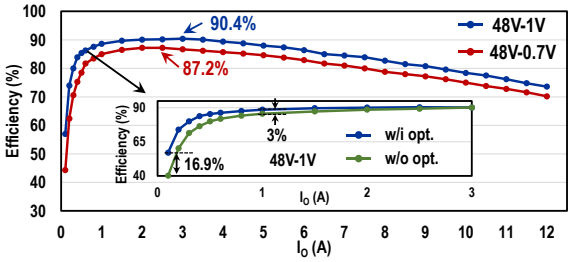

Fig. 8. Measured efficiency.

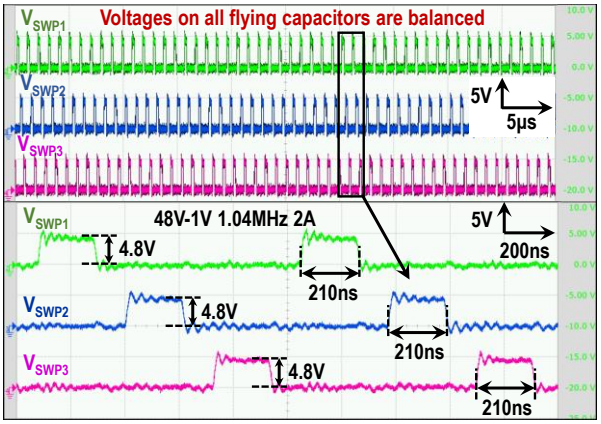

Fig. 7. Measured switching waveform.

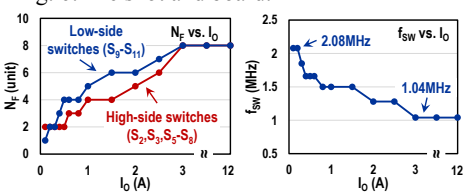

Fig. 9. Optimization results.

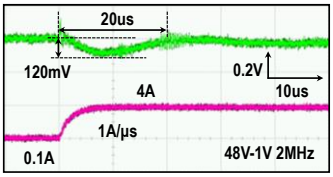

Fig. 10. Transient response.

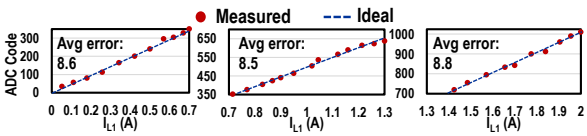

Fig. 11. Current sensing results.

	APEC 2019 [1]	ISSCC 2020 [2]	ISSCC 2020 [3]	JSSC 2020 [4]	ISSCC 2021 [5]	This work
Technology	Discrete	180nm BCD	180nm BCD	180nm BCD	180nm BCD	180nm BCD
Topology	Dual-phase Multi-inductor hybrid	Tri-state Double Step Down	3-level+ current doubler	Double Step Down	12-level series-capacitor	3-level hybrid Dickson
Input Voltage	48V	12V/24V	48-60V	48V	36-60V	48V
Output Voltage	1-5V	1V	0.5-1V	1V	0.5-1V	0.7-1V
Max Load Current	100A	3A	60A	1.5A	8A	12A
Power Switches	GaN	On-chip Si	Ext. Si	GaN	On-chip Si & GAN	On-chip Si & GAN
Inductor	4x1uH	2x0.56uH	2x0.33uH+transformer	2x0.9uH	/	3x0.62uH
#. of Flying Capacitor	3	2	1	1	11	5
Voltage Reduction	4x	4x	16x	2x	12x	10x
#. of External Switch	8	0	6	4	1	2
Peak Efficiency	90.9%@48-1V, 333kHz	88.3%@24-1V, 100kHz	92.8%@48-1V, 333kHz	85.4%@48-1V, 100kHz	90.2%@48-1V, 2.5MHz	90.4%@48-1V, 1MHz
On-chip Optimization	No	No	No	No	No	Yes
Current Density	440 A/inch^3	/	/	/	196/ *998 A/inch^3	#240/ **992A/inch^3

*current density for component area only. #without C_O and C_{BST}.

Table. I. Comparison with state-of-the-art.