Cong (Callie) Hao

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RESEARCH AREA

- **High-performance reconfigurable computing**: FPGA, embedded system, IoT and edge computing
- **Machine learning and system**: hardware acceleration, ML algorithm/system co-design, autonomous driving
- **Electronic design automation (EDA)**: high-level synthesis (HLS), physical synthesis, network-on-chip

EDUCATION

Ph.D.	Electrical Engineering	Waseda University, Japan	2014 - 2017
M.S.	Electrical Engineering	Waseda University, Japan	2010 - 2012
M.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2011 - 2014
B.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2007 - 2011

PROFESSIONAL APPOINTMENTS

2022.01 - present	Assistant Professor	School of Electrical and Computer Engineering Georgia Institute of Technology, USA
2020.09 - 2021.12	Faculty Fellow **transitional position due to Visa delay*	School of Electrical and Computer Engineering Georgia Institute of Technology, USA
2017.12 - 2020.09	Postdoctoral Researcher	School of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, USA

HONORS

2022	Appointed to Sutterfield Family Early Career Professorship, Georgia Tech
2021	Best Paper Award, ACM Great Lakes Symposium on VLSI (GLSVLSI)
2020	Third place winner, IEEE Design Automation Conference (DAC) System Design Contest
2019	First place winner (FPGA track, 1/58), IEEE DAC System Design Contest First place winner (GPU track, 1/52), IEEE DAC System Design Contest
2019	Best Poster Award, ICML Workshop
2018	Student Innovation Award, IEEE HPEC Graph Challenge
2018	Third place winner (FPGA track, 3/62), IEEE DAC System Design Contest
2018	Distinguished Project Award, Boeing Global Technology
2016	Best Student Paper, IEEE International New Circuits and Systems Conference
2015	Best Student Paper, IEEE International Conference on ASIC
2015	Student travel grant (250 US$), International Workshop on Logic and Synthesis
2015	Young Student Fellow Award, IEEE Design Automation Conference (1K US$ grant)
2015	Excellent Paper Award, ISIPS, Graduate School of IPS, Japan
2013	Best Student Paper, IEEE International Conference on ASIC
2013	Google Anita Borg Memorial Scholarship (1.5K US$)
2013	IEICE VLD Excellent Student Award, Asia and South Pacific Design Automation Conference
2012	Best Paper Nomination, International Symposium on VLSI Design, Automation and Test

RESEARCH FUNDING

DARPA "Ultra-Light Video Intelligence by Data-Circuit-Model Tri-Design: In-Pixel Filtering, In-Memory Focusing, and In-Loop Optimization", *Artificial Intelligence Exploration (AIE)*
PI: Shimeng Yu. Co-PI: Callie Hao, Shiyu Chang, Atlas Wang, Sijia Liu
Year: 2021-2022. Total = $1,000,000. My share = $200,000.

PUBLICATIONS

- **Journals**

[1] **Cong Hao**, Jordan Dotzel, Jinjun Xiong, Luca Benini, Zhiru Zhang, and Deming Chen, "Enabling Design Methodologies and Future Trends forEdge AI: Specialization and Co-design", *IEEE Design & Test, 2021*

[2] Cheng Gong, Ye Lu, Tao Li, **Cong Hao**, Deming Chen, and Yao Chen, "VecQ: High Accuracy DNN Model Compression with Vectorized Weight Quantization", *IEEE Transactions of Computers*, 2020

[3] Jianwei Zheng, Chao Lu, **Cong Hao**, Deming Chen, and Donghui Guo, "Improving the Generalization Ability of Deep Neural Networks for Cross-Domain Visual Recognition", *IEEE Transactions on Cognitive and Developmental Systems*, 2020

[4] Zhao Yi, **Cong Hao**, and Takeshi Yoshimura. "Thermal and Wirelength Optimization With TSV Assignment for 3D-IC", *IEEE Transactions on Electron Devices*, 2019

[5] Ma Jiayi, **Cong Hao**, and Kundong Wang. "Decomposing and Cluster Refinement Design Method for Application-Specific Network-on-Chips.", *Journal of Shanghai Jiao Tong University (Science)*, 2018

[6] **Cong Hao**, Takeshi Yoshimura. "An Efficient Multi-Level Algorithm for 3D-IC TSV Assignment", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, March 2017

[7] **Cong Hao**, Nan Wang, and Takeshi Yoshimura. "A Unified Scheduling Approach for Power and Resource Optimization with Multiple V-dd or/and V-th in High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2017.

[8] **Cong Hao**, Jianmo Ni, Nan Wang, and Takeshi Yoshimura. "Interconnection Allocation between Functional Units and Registers in High-Level Synthesis", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[9] Wang Nan, Wei Zhong, **Cong Hao**, Song Chen, Takeshi Yoshimura, and Yu Zhu. "Leakage-power-aware scheduling with dual-threshold voltage design.", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[10] Nan Wang, Song Chen, **Cong Hao**, Haoran Zhang, and Takeshi Yoshimura. "Leakage Power Aware Scheduling in High-Level Synthesis.", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, 2014

- **Conferences**

[11] Nan Wu, Hang Yang, Yuan Xie, Pan Li, **Cong Hao**, "High-Level Synthesis Performance Prediction using GNNs: Benchmarking, Modeling, and Advancing", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2022.

[12] Xinyi Zhang, **Cong Hao**, Peipei Zhou, Alex Jones, Jingtong Hu, "H2H: Heterogeneous Model to Heterogeneous System Mapping with Computation and Communication Awareness", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2022.

[13] Hanchen Ye, **Cong Hao**, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, Deming Chen, "ScaleHLS: A New Scalable High-Level Synthesis Framework on Multi-Level Intermediate Representation", IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022

[14] Yuhong Li, **Cong Hao**, Pan Li, Jinjun Xiong, Deming Chen, "Generic Neural Architecture Search via Regression", International Conference on Neural Information Processing Systems (NeurIPS), 2021, Spotlight

[15] Xinheng Liu, Yao Chen, **Cong Hao**, Ashutosh Dhar, Deming Chen, "WinoCNN: Kernel Sharing Winograd Systolic Array for Efficient Convolutional Neural Network Acceleration on FPGAs", IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2021

[16] Yao Chen, Cole Hawkins, Kaiqi Zhang, Zheng Zhang, **Cong Hao**, "3U-EdgeAI: Ultra-Low Memory Training, Ultra-Low Bitwidth Quantization, and Ultra-Low Latency Acceleration", ACM Great Lakes Symposium on VLSI (GLSVLSI), 2021, Invited

[17] Nan Wu, Yuan Xie, **Cong Hao**, "IronMan: GNN-assisted Design Space Exploration in High-Level Synthesis via Reinforcement Learning", ACM Great Lakes Symposium on VLSI (GLSVLSI), 2021, Best Paper Award

[18] **Cong Hao**, Deming Chen, "Software/Hardware Co-design for Multi-modal Multi-task Learning in Autonomous System", IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2021, Invited

[19] Lixiang Li, Yao Chen, Zacharie Zirnheld, Pan Li, and **Cong Hao**, "MeLoPPR: Software/Hardware Co-design for Memory-efficient Low-latency Personalized PageRank", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2021.

[20] Dongning Ma, Rahul Thapa, Xingjian Wang, **Cong Hao** and Xun Jiao, "Workload-Aware Approximate Computing Configuration". IEEE/ACM Design, Automation & Test in Europe Conference (DATE), 2021.

[21] Yuhong Li*, **Cong Hao***, Xiaofan Zhang, Chen Yao, Jinjun Xiong, Wen-mei Hwu and Deming Chen, "EDD: Efficient Differentiable DNN Architecture and Implementation Co-search for Embedded AI Solutions", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2020.

[22] Xiaofan Zhang, Haoming Lu, **Cong Hao**, Jiachen Li, Bowen Cheng, Yuhong Li, Kyle Rupnow, Jinjun Xiong, Thomas Huang, Honghui Shi, Wen-mei Hwu, Deming Chen, "SkyNet: a Hardware-Efficient Method for Object Detection and Tracking on Embedded Systems", The Conference on Machine Learning and Systems (SysML), 2020.

[23] Pengfei Xu, Xiaofan Zhang, **Cong Hao**, Yang Zhao, Zetong Guan, Yongan Zhang, Yue Wang, Deming Chen and Yingyan Lin, "AutoDNNchip: An Automated DNN Chip Generator through Compilation, Optimization, and Exploration", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2020.

[24] **Cong Hao**, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, Junli Gu and Deming Chen, "NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019.

[25] **Cong Hao**, Xiaofan Zhang, Yuhong Li, Sitao Huang, Jinjun Xiong, Kyle Rupnow, Wen-Mei Hwu, and Deming Chen, "FPGA/DNN Co-Design: An Efficient Design Methodology for IoT Intelligence on the Edge", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2019.

[26] **Cong Hao**, Atif Sarwari, Bryan Wu, Zhijie Jin, Junli Gu, and Deming Chen, "FPGA-based Secondary System for Autonomous Driving Cars", Proceedings of IEEE International Workshop on Signal Processing Systems, 2019.

[27] Yao Chen, Kai Zhang, Cheng Gong, **Cong Hao**, Xiaofan Zhang, Tao Li, and Deming Chen, "TDLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA", Proceedings of IEEE Computer Society Annual Symposium on VLSI, 2019.

[28] Cheng Gong, Ye Lu, **Cong Hao**, Xiaofan Zhang, Tao Li, Deming Chen, and Yao Chen, "μL2Q: An Ultra-Low Loss Quantization Method for DNN Compression", Proceedings of International Joint Conference on Neural Networks (IJCNN), 2019.

[29] Xiaofan Zhang, **Cong Hao**, Yuhong Li, Yao Chen, Jinjun Xiong, Wen-Mei Hwu and Deming Chen, "A Bi-Directional Co-Design Approach to Enable Deep Learning on IoT Devices," Joint Workshop on On-Device Machine Learning & Compact Deep Neural Network Representations, ICML Workshop, 2019, Best Poster Award

[30] Yao Chen, Jiong He, Xiaofan Zhang, **Cong Hao**, and Deming Chen, "Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2019.

[31] **Cong Hao**, Deming Chen, "Deep Neural Network Model and FPGA Accelerator Co-design: Opportunities and Challenges", Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018.

[32] Sitao Huang, Mohamed El-Hadedy, **Cong Hao**, Qin Li, Vikram S Mailthody, Ketan Date, Jinjun Xiong, Deming Chen, Rakesh Nagi, Wen-mei Hwu, "Triangle Counting and Truss Decomposition using FPGA", IEEE High Performance extreme Computing Conference (HPEC), 2018

[33] Yi Zhao, **Cong Hao**, Takeshi Yoshimura, "TSV Assignment of Thermal and Wirelength Optimization for 3D-IC Routing", In 28th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2018

[34] **Cong Hao**, and Takeshi Yoshimura. "Application of on-line machine learning in optimization algorithms: A case study for local search." Computer Science and Electronic Engineering (CEEC), IEEE, 2017

[35] Yangyizhou Wang, **Cong Hao**, and Takeshi Yoshimura. "A Particle Swarm Optimization and Branch and Bound Based Algorithm for Economical Smart Home Scheduling" In 20th IEEE MWSCAS, 2017

[36] Yuxin Qian, **Cong Hao**, and Takeshi Yoshimura. "3D-IC signal TSV assignment for thermal and wirelength optimization" In 27th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2017

[37] Jiayi Ma, **Cong Hao**, Takeshi Yoshimura. "Power-efficient Partitioning and Cluster Generation Design for Application-Specific Network-on-Chip" In 13th IEEE ISOCC, 2016

[38] Hui Zhu, **Cong Hao**, Takeshi Yoshimura. "Thermal-Aware Floorplanning for NoC-Sprinting" In 59th IEEE MWSCAS, 2016

[39] **Cong Hao**, Takeshi Yoshimura. "Economical Smart Home Scheduling for Single and Multiple Users" In 59th IEEE MWSCAS, 2016

[40] **Cong Hao**, Nan Ding, Takeshi Yoshimura. "An Efficient Algorithm for 3D-IC TSV Assignment". In 14th IEEE NEWCAS, 2016, Best Student Paper

[41] **Cong Hao**, Takeshi Yoshimura. "EACH: An Energy-Efficient High-Level Synthesis Framework for Approximate Computing" In 2nd IEEE WAPCO, 2016

[42] Jian-Mo Ni, Qian Ai, **Cong Hao**, Takeshi Yoshimura, Nan Wang. "Primal-Dual Method based Simultaneous Functional Unit and Register Binding." In 10th ASICON, 2015

[43] **Cong Hao**, Nan Wang, Jian-Mo Ni, Takeshi Yoshimura. "An Efficient Tabu Search Methodology for Port Assignment Problem in High-Level Synthesis." In 24th IWLS, 2015

[44] **Cong Hao**, Jian-Mo Ni, Hui-Tong Wang, Takeshi Yoshimura. "Simultaneous Scheduling and Binding For Resource Usage and Interconnect Complexity Reduction in High-Level Synthesis." In 11th IEEE ASICON, 2015, Best Student Paper

[45] **Cong Hao**, Song Chen, Takeshi Yoshimura. "Network simplex method based Multiple Voltage Scheduling in Power-efficient High-level synthesis." In 18th IEEE ASP-DAC, 2013, IEICE VLD Excellent Student Award

[46] **Cong Hao**, Nan Wang, Song Chen, Takeshi Yoshimura, Min-You Wu. "Interconnection allocation between functional units and registers in High-Level Synthesis." In 10th IEEE ASICON, 2013, Best Student Paper

[47] Wang Nan, **Cong Hao**, Nan Liu, Haoran Zhang, Takeshi Yoshimura. "Timing and resource constrained leakage power aware scheduling in high-level synthesis." In 10th IEEE ASICON, 2013,

[48] **Cong Hao**, Haoran Zhang, Song Chen, Takeshi Yoshimura, Min-You Wu. "Port assignment for multiplexer and interconnection optimization." In 5th IEEE ASQED, 2013

[49] Haoran Zhang, **Cong Hao**, Nan Wang, Song Chen, Takeshi Yoshimura. "Power and resource aware scheduling with multiple voltages." In 10th IEEE ASICON, 2013, Best Student Paper

[50] **Cong Hao**, Song Chen, Takeshi Yoshimura. "Port assignment for interconnect reduction in high-level synthesis." In 19th IEEE VLSI-DAT, 2012, Best Paper Nomination

INVITED TALKS

Feb. 2022	"GenGNN: a Generic FPGA Acceleration Framework for Graph Neural Networks" *Georgia Tech CRNCH Summit, virtual*
Oct. 2021	"How Powerful are Graph Neural Networks and Reinforcement Learning in EDA: a Case Study in High-Level Synthesis" *Stevens Institute of Technology ECE Seminar, virtual*
Sep. 2021	"How Powerful are Graph Neural Networks and Reinforcement Learning in EDA: a Case Study in High-Level Synthesis" *Rutgers EFficient AI (REFAI) Seminar, virtual*
Jun. 2021	"Software/Hardware Co-Design for Multimodal Multi-Task Learning in Autonomous Systems" *IEEE AICAS 2021, special session, virtual*
Jun. 2021	"3U-EdgeAI: Ultra-Low Memory Training, Ultra-Low Bit-width Quantization, and Ultra-Low Latency Acceleration" *ACM GLSVLSI 2021, special session, virtual*
Nov. 2019	"NAIS: neural architecture and implementation co-search" *IEEE/ACM ICCAD 2019, special session, Denver, CO*

TEACHING EXPERIENCE

Spring 2022	Georgia Tech, ECE8893 (Parallel Programming for FPGAs) Graduate-level class of 43 students
Fall 2021	Georgia Tech, ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture) Graduate-level class of 70 students
Fall 2019	University of Illinois at Urbana-Champain, ECE 498 (IoT and Cognitive Computing) Guest Lecturer

Spring 2018 University of Illinois at Urbana-Champain, ECE 527 (System-on-Chip Design)
Guest Lecturer

PROFESSIONAL SERVICES

- **Associate Editor**

2020-present Neural Processing Letters (Springer)

- **Conference Organization**

2021 Publicity chair of 30th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2022)
2021 Co-chair of 58th IEEE/ACM Design Automation Conference System Design Competition (DAC-SDC), 2022
2021 Co-chair of ACM Student Research Competition at ICCAD (SRC@ICCAD21), 2021

- **Technical Program Committee**

2022 TinyML'22, FCCM'22
2021 DAC'22, DAC'21, DATE'21, ICCD'21
2020 DATE'20, ICCD'20, SRC@ICCAD'20, CENICS'20
2019 CENICS'19

- **Session Chair**

2021 ICCV'21 Workshop (Low-power Computer Vision)
2021 GLSVLSI'21 (New Trends in Hardware Security, Towards Energy-efficient Machine Learning)
2020 ICCD'20 (Novel Architectures)
2020 DATE'20 (Hardware-aware Training)

- **Journal Review**

IEEE Journal on Selected Areas in Communications
Engineering Optimization
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
IEEE Design & Test (D&T)
Multidimensional Systems & Signal Process (MULT)
ACM Transactions on Design Automation of Electronic Systems (TODAES)
IEEE Internet of Things Journal
ACM Journal on Emerging Technologies in Computing Systems (JETC)
IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
ACM Transactions on Embedded Computing Systems (TECS)
IEEE Transactions on Computers (TC)