Poulami Das

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Education

Georgia Institute of Technology, GA, USA — Aug 2017 - Present
Ph.D. Candidate, Electrical and Computer Engineering — GPA - 4.0/4.0
Recipient of Microsoft Research PhD Fellowship
Advisor: Moinuddin Qureshi
Research Area: Software and Architecture for Reliable Quantum Computing

The University of Texas at Austin, TX, USA — Aug 2014 - May 2016
M.S. in Electrical and Computer Engineering — GPA - 3.82/4.0

National Institute of Technology, Durgapur, India — Jul 2008 - May 2012
B.Tech. in Electronics and Communication Engineering — GPA - 9.53/10.0
Institute Gold Medal for Highest Distinction

PhD Dissertation Research

Title: Software and Architecture for Reliable Quantum Computing
Summary: Quantum computers promise to accelerate many important classes of applications. However, qubit devices are noisy and cause computational errors during the execution of quantum programs. *My research bridges the gap between quantum applications and noisy devices using software and architecture solutions.* Quantum computers can be made fault-tolerant by using quantum error correction (QEC). However, QEC codes are too resource-intensive to be practical in the near-term. Instead, these systems run program in the presence of errors. My research focuses on designing compiler optimizations and software post-processing techniques to *mitigate the impact of hardware errors* on near-term quantum applications. In the long run, the objective is to build Fault-Tolerant Quantum Computers that can power a wider class of application. My research focuses on leveraging micro-architectural and system-level solutions to enable *error correction* on these systems.

Awards and Honors

- Selected as a Rising Star in EECS, UT Austin, 2022.
- Invited to the 7^{th} Workshop on the Future of Computing Architectures (FOCA), IBM Research, 2022.
- Invited to the 9^{th} Heidelberg Laureate Forum, 2022.
- Best Research Award, Ph.D. Forum, Design Automation Conference 2022.
- Colonel Oscar P. Cleaver Award for the Most Outstanding PhD Dissertation Proposal, Georgia Tech, 2022.
- Microsoft Research PhD Fellowship, 2020-2022.
- Distinguished Alumnus of Ashok Hall Group of Schools, Kolkata, 2020.
- Best Paper Award for "A Case for Superconducting Accelerators" at Computing Frontiers, 2019.
- Institute Gold Medal for Highest Distinction in B. Tech, NIT Durgapur, 2012.
- Institute Gold Medal for Overall Scholastic Excellence in B. Tech, NIT Durgapur, 2012.

Publications

1. ISCA'23 — Suhas Vittal, **Poulami Das**, and Moinuddin Qureshi,
Astrea: Accurate Quantum Error-Decoding via Practical Minimum-Weight Perfect-Matching,
International Symposium on Computer Architecture (**ISCA**) 2023.

2. HPCA'23 — **Poulami Das**, Yunong Shi, and Eric Kessler,
The Imitation Game: Leveraging CopyCats for Robust Native Gate Selection in NISQ Programs,
International Symposium on High-Performance Computer Architecture (**HPCA**) 2023.

3. ASPLOS'23 — Ramin Ayanzadeh, Narges Alavisamani, **Poulami Das**, and Moinuddin Qureshi,
FrozenQubits: Boosting Fidelity of QAOA by Skipping Hotspot Nodes,
International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2023.

4. QCE'22 — Ramin Ayanzadeh, **Poulami Das**, Swamit Tannu, and Moinuddin Qureshi,
EQUAL: Improving Fidelity of Quantum Annealers by Injecting Controlled Perturbations,
International Conference on Quantum Computing and Engineering (**QCE**), 2022.

5. ASPLOS'22 — **Poulami Das**, Aditya Locharla, and Cody Jones,
LILLIPUT: A Lightweight Low-Latency Lookup-Table Decoder for Near-term Quantum Error Correction,
International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2022.

6. ASPLOS'22 — Swamit Tannu, **Poulami Das**, Ramin Ayanzadeh, and Moinuddin Qureshi,
HAMMER: Boosting Fidelity of Noisy Quantum Circuits by Exploiting Hamming Behavior of Erroneous Outcomes,
International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2022.

7. HPCA'22 — **Poulami Das**, Christopher A. Pattison, Srilatha Manne, Douglas M. Carmean, Krysta M. Svore, Moinuddin Qureshi, and Nicolas Delfosse,
AFS:Accurate, Fast, and Scalable Error-Decoding for Fault-Tolerant Quantum Computers,
International Symposium on High-Performance Computer Architecture (**HPCA**), 2022.

8. MICRO'21 — **Poulami Das**, Swamit Tannu, and Moinuddin Qureshi,
JigSaw: Boosting Fidelity of NISQ Programs via Measurement Subsetting,
International Symposium on Microarchitecture (**MICRO**), 2021.

9. MICRO'21 — **Poulami Das***, Swamit Tannu*, Siddharth Dangwal, and Moinuddin Qureshi,
ADAPT: Mitigating Idling Errors in Qubits via Adaptive Dynamical Decoupling,
International Symposium on Microarchitecture (**MICRO**), 2021. [*Equal Contributions]

10. MICRO'19 — **Poulami Das**, Swamit S. Tannu, Prashant J. Nair, and Moinuddin Qureshi,
A Case for Multi-programming Quantum Computers,
International Symposium on Microarchitecture (**MICRO**), 2019.

11. CF'19 — Swamit S. Tannu, **Poulami Das**, Michael L. Lewis, Robert Krick, Douglas M. Carmean, and Moinuddin K. Qureshi,
A Case for Superconducting Accelerators,
International Conference on Computing Frontiers (**CF**), 2019.
Best Paper Award

Research Internships and Full-Time Experience

- **Amazon Braket Science (Quantum Research)** — Seattle, USA
  Applied Science (Research) Intern, Advisor: Yunong Shi, Eric Kessler — May 2022 - Jul 2022
  - *Braket Compiler Tool-chain*: Shaped the vision of AWS Braket's quantum software stack for near-term quantum computers by establishing a systematic view of noise-aware compilation workflow and software error-mitigation.
  - *Noise-aware instruction selection (accepted at **HPCA'23**)*: Designed *ANGEL*, which is a noise-adaptive compiler for efficient selection of native gates supported by a quantum hardware while translating high-level instructions of quantum programs to improve application fidelity.

- **Google Quantum AI Research** — California, USA
  Research Intern, Advisor: Cody Jones — May 2021 - July 2021
  - *Look-Up Table Decoders for Near-term Quantum Error Correction (published at **ASPLOS'22**)*: Designed *LILLIPUT*, which is a reconfigurable, lightweight, low latency, and accurate lookup table decoder for practical adoption to study small surface codes in the near-term. Also, proposed memory compression techniques to reduce the storage overheads of the design such that it can fit on off-the-shelf FPGAs.

- **Microsoft Research** — Redmond, USA
  Research Intern, Advisors: Srilatha Manne, Doug Carmean, Nicolas Delfosse — May 2019 - July 2019
  - *Hardware-Efficient Scalable Decoding (published at **HPCA'22**)*: Designed the micro-architecture of the *AFS* decoder, which uses a fully-pipelined Union-Find algorithm to improve error decoding latency compared to prior software implementations. Also, proposed an optimized hardware-efficient system architecture to scale to large systems. Furthermore, analyzed low-cost data compression schemes to reduce the bandwidth required for data transmission between the quantum substrate and decoders.

- **Microsoft Research** — Redmond, USA
  Research Intern, Advisor: Doug Carmean — May 2018 - July 2018
  - *Noise Model of Transmon*: Developed an analytical tool to model the fidelities of a *transmon* qubit.
  - *Superconducting Logic Design (**Best Paper at CF'19**)*: Designed an accelerator to understand trade-offs in system level superconducting logic design. Also, developed a methodology to analyze superconducting designs using standard CMOS tools.

- **NXP Semiconductors (formerly Freescale)** — Austin, USA
  Design Engineer, Digital Network Group — May 2016 - Aug 2017
  Graduate Design Intern, Digital Network Group — May 2015 - Aug 2015
  - *IP and Network SOC Design*: Designed PCIe controller and energy-efficient Ethernet modules. Defined the architecture and designed the control and reset block to support the integration of different protocol configurations on the SerDes IP for a wide range of networking SoCs. Performed SOC integration, standard design checks (synthesis, logical equivalence, DFT checks, and clock domain crossing) and led the IP documentation for verification planning.

- **LSI Corporation (currently Broadcom)** — Bangalore, India
  IC Design Engineer I, Custom Solution Engineering Group — Aug 2012 - Aug 2014
  - *Low Power Verification*: Developed the environment to perform design checks and verify the low power features of PCIe subsystem, Ethernet subsystems, and Security subsystem for SSD controllers.

Patents

1. US Patent 11,410,070- Syndrome Data Compression for Quantum Computing Devices, *Granted, 2022.*
2. Pipelined Hardware Decoder for Quantum Computing Devices, *Submitted, 2019.*
3. Systems for Coupling Decoders to Quantum Registers, *Submitted, 2019.*
4. Geometry-based Compression for Quantum Computing Devices, *Submitted, 2019.*

Research Talks

- **Software and Architecture for Reliable Quantum Computing**
  University of California, San Diego (*Host*: Dean Tullsen) Apr 2023
  University of Illinois, Urbana Champaign (*Host*: Saugata Ghose) Apr 2023
  University of Texas, Austin (*Host*: Derek Chiou) Apr 2023
  Cornell University, Ithaca (*Host*: Christopher Batten) Mar 2023
  University of California, Los Angeles (*Host*: Tony Nowatzski) Mar 2023
  Carnegie Mellon University, Pittsburgh (*Host*: Franz Franchetti) Mar 2023
  Columbia University, New York (*Host*: John Wright)) Feb 2023
  University of Michigan, Ann Arbor (*Host*: Georgios Tzimpragos) Feb 2023
  EPFL, Lausanne (*Host*: Babak Falsafi) Feb 2023
  IBM Research, Yorktown Heights (*Host*: Ali Javadi-Abhari) Oct 2022
  [*Poster Presentation*] Rising Stars in EECS Workshop, UT Austin Oct 2022
  ETH, Zurich (*Host*: Onur Mutlu) Sep 2022
  TU, Munich (*Host*: Robert Wille) Sep 2022
  Georgia Tech Quantum Alliance Workshop, Atlanta May 2022

- **Architecture and System-Level Solutions for Real-Time Decoding in Fault-Tolerant Quantum Computers**
  [*Invited Talk*] APS March Meeting, Las Vegas Mar 2023

- **Low-cost Decoding Solutions for Near-Term Quantum Error Correction**
  Real Time Decoding Workshop, IEEE Quantum Week (QCE), Broomfield Sep 2022
  Google Quantum AI, California Jul 2021

- **The Imitation Game: Leveraging CopyCats for Robust Native Gate Selection**
  Amazon Braket Science, Seattle Aug 2022

- **Hardware and Circuit Synthesis for Reliable Quantum Computing**
  [*Poster Presentation*] DAC Ph.D. Forum, San Francisco Jul 2022

- **ForeSight: Reducing SWAPs in via Adaptive Multi-Candidate Evaluations**
  Amazon Braket, Seattle May 2022

- **A Scalable Decoder Micro-architecture for Fault-Tolerant Quantum Computing**
  Microsoft Research, Redmond Jul 2019

- **A Case for Superconducting Accelerators**
  Superconducting Digital Computing Architecture Research Workshop, New York Jun 2022
  ETH, Zurich (*Host*: Onur Mutlu) Apr 2019
  Microsoft Research, Redmond Jul 2018

Teaching Experience

- **Teaching Assistant** at Georgia Tech [*Upcoming*] Summer 2023
  Quantum Computing (CS 8803-O13)
- **Guest Lecturer** at Georgia Tech Fall 2022
  Quantum Computing (CS 8803-O13) [Lecture on Quantum Error Correction]
- **Co-Instructor** at Georgia Tech Spring 2022
  Introduction to Quantum Computing (CS 4803/ CS 8803)
- **Teaching Assistant** at Georgia Tech Fall 2017, Spring 2018, Fall 2018
  Advanced Computer Architecture (ECE 6100/ CS 6290)
- **Teaching Assistant** at UT Austin Spring 2015, Fall 2015, Spring 2016
  Digital Logic Design (ECE 316)

Research Mentoring Experience

- **Ramin Ayanzadeh** [Computing Innovation Postdoctoral Fellow at Georgia Tech] Fall 2020- Present
  Improving the fidelity of quantum annealers and gate-model quantum computers
  - HAMMER published at ASPLOS'22
  - EQUAL published at IEEE QCE'22
  - FrozenQubits accepted for publication at ASPLOS'23
- **Narges Alavisamani** [Ph.D. at Georgia Tech] Fall 2021- Present
  Designing high-fidelity quantum machine learning circuits using reinforcement learning
  - Early results presented in the CWIDCA Workshop at MICRO'2022.
- **Jiahao Wen** [M.S. at Georgia Tech] Fall 2021- Spr 2022
  Improving the measurement fidelity of superconducting qubits by using hybrid software discrimination
  - Successful defense of the MS Thesis
- **Suhas Vittal** [B.S. at Georgia Tech] Fall 2021- Present
  Software error-mitigation and architecture for quantum error correction.
  - **First runner-up at MICRO'2022 Student Research Competition for MIDAS**
- **Sahil Khan** [B.S. at Georgia Tech] Fall 2022- Present
  Improving the efficiency of surface code communication.

Academic Service

- **Artifact Evaluation Committee Member** MICRO-2022
- **External Review Committee Member** ISCA-2022
- **Student Mentor in Undergrad Architecture (uArch) Workshop** ISCA-2022
- **Life in Graduate School Panel Member** [*uArch Workshop*] ISCA-2021, ISCA-2022

References

(1) **Moinuddin Qureshi**
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(2) **Frederic T. Chong**
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