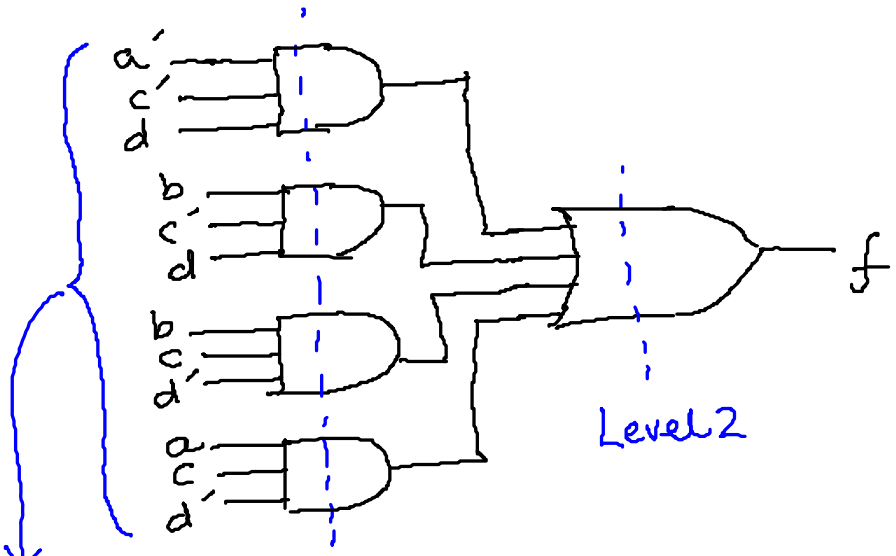
7.1 Multiple-Level Gate Circuits

Levels of gates: Maximum number of gates connected between a circuit input and the output

Two level: sum of products (SOP), product of sums (POS)

$$f = a'c'd + bc'd + bcd' + acd'$$



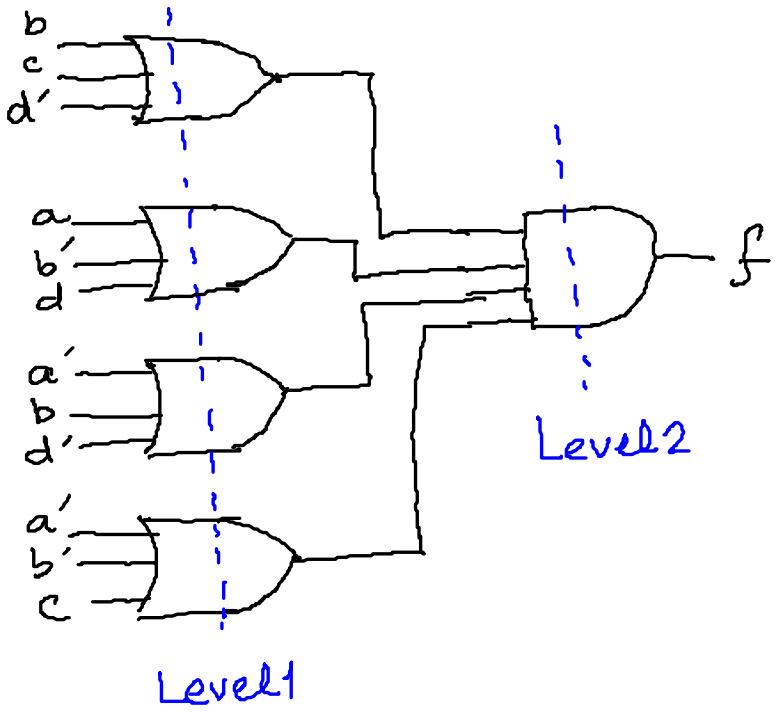
SOP

AND-OR

Two levels
Five gates
16 gate inputs

Coming from flipflops where both Q and Q' is available

$$f = (b + c + d')(a + b' + d)(a' + b + d')(a' + b' + c)$$



POS

OR-AND

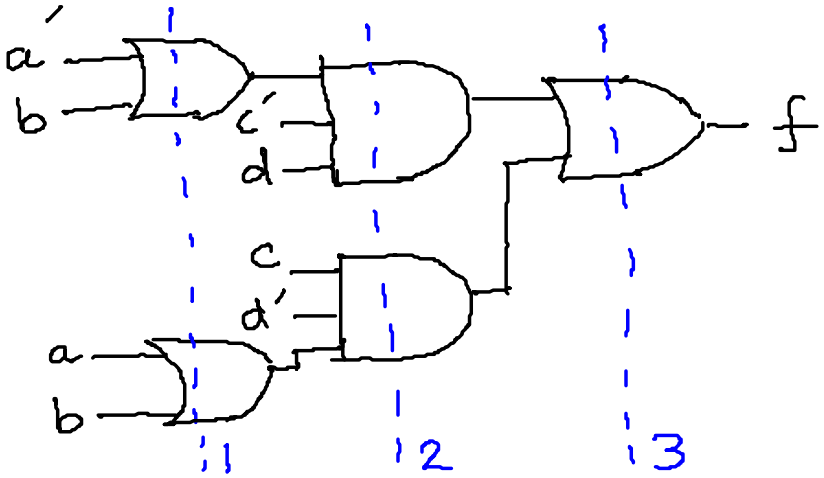
The number of levels in an AND-OR circuit can usually be increased by factoring the SOP expression from which it was derived.

$$f = a'c'd + bc'd + bcd' + acd'$$

factor

$$= c'd(a' + b) + cd'(a + b)$$

$c'd(a'+b)+cd'(a+b)$



Three levels

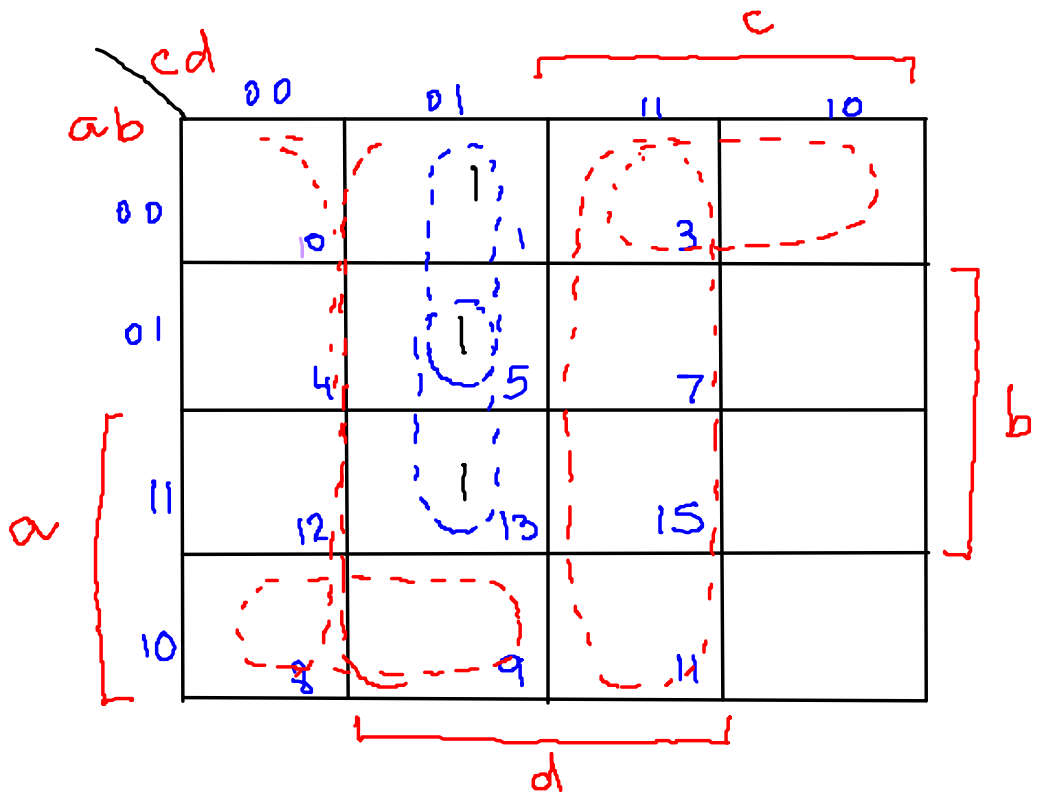
Five gates

12 gate inputs

Beat three level solution

Example:

$f(a,b,c,d)=\sum m(1,5,6,10,13,14)$

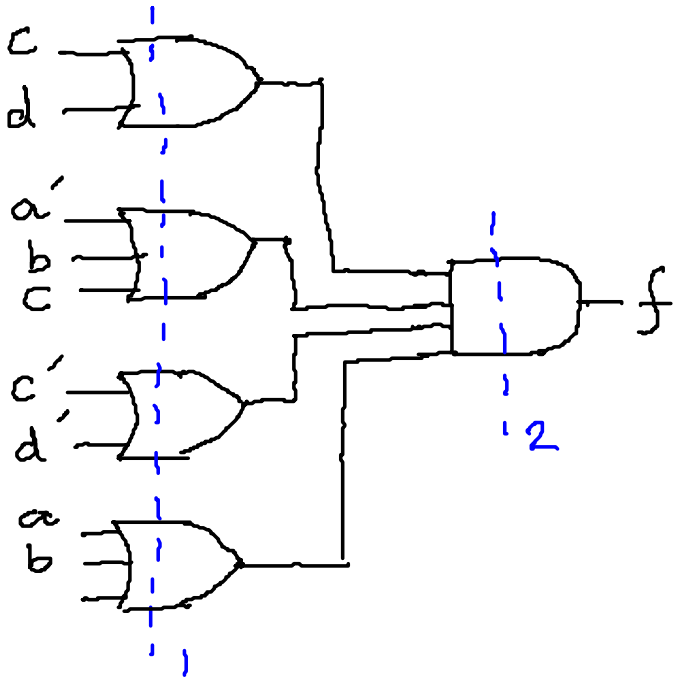


$a'c'd+bc'd+bcd'+acd'$

product of sums

$$f' = c'd' + ab'c' + cd + a'b'c$$

$$f = (c+d)(a'+b+c)(c'+d')(a+b+c')$$



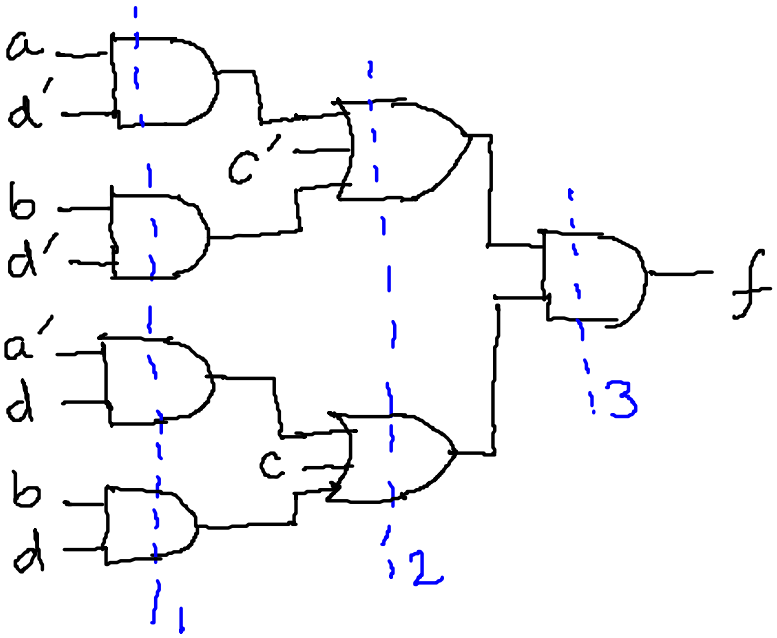
Two levels
Five gates
14 gate inputs
Best two level solution

The number of levels in an OR-AND circuit can usually be increased by multiplying out some of the terms in the POS expression from which it was derived

$$f = \underbrace{(c+d)(a'+b+c)}_{(c+d(a'+b))}\underbrace{(c'+d')(a+b+c')}_{(c'+d'(a+b))}$$

using $(x+y)(x+z) = x+yz$

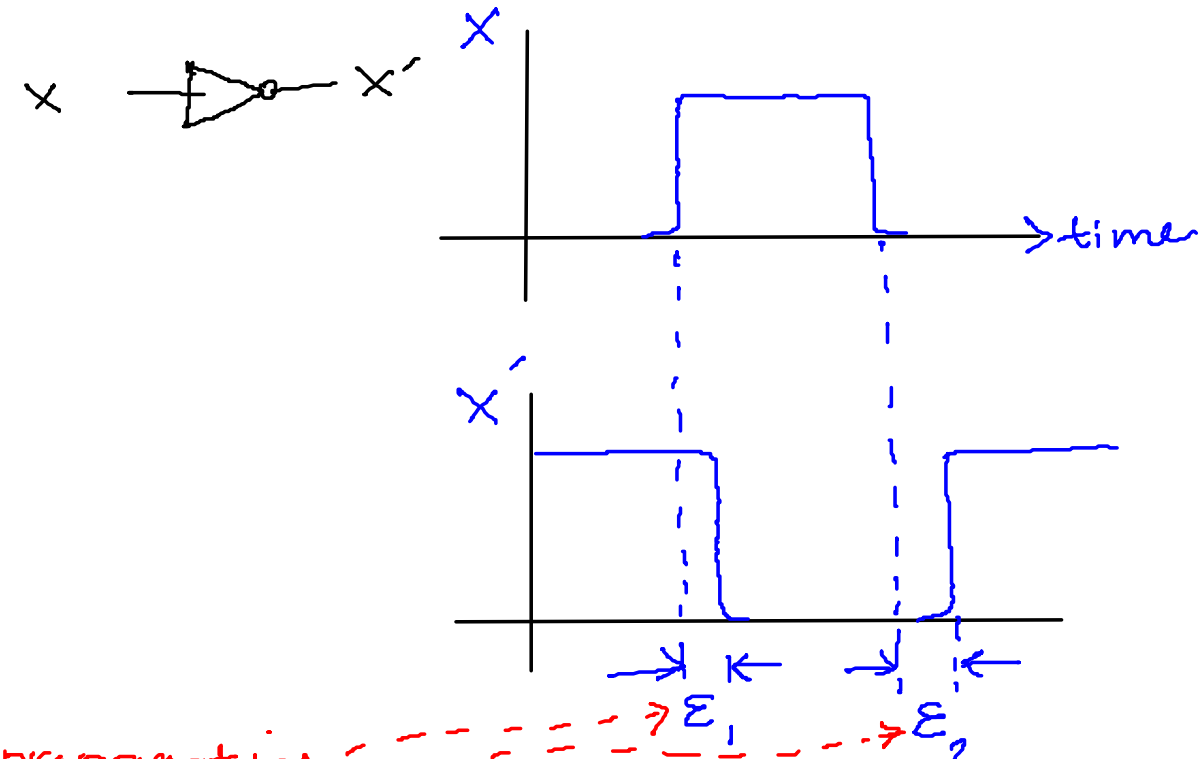
$$f = (c+d(a'+b))(c'+d'(a+b))$$
$$= (c+a'd+bd)(c'+ad'+bd')$$



Three levels
Seven gates
16 gate inputs

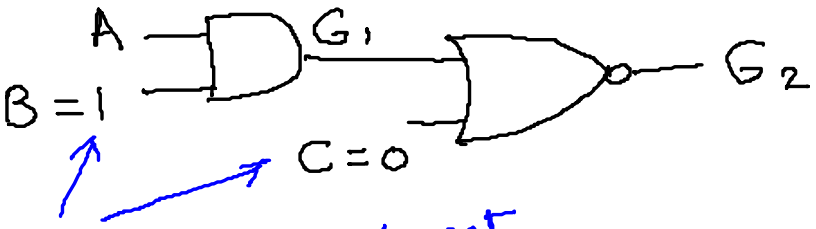
8.3 Gate Delays & Timing Diagrams

When the input to a logic gate is changed, the output will not change instantaneously.



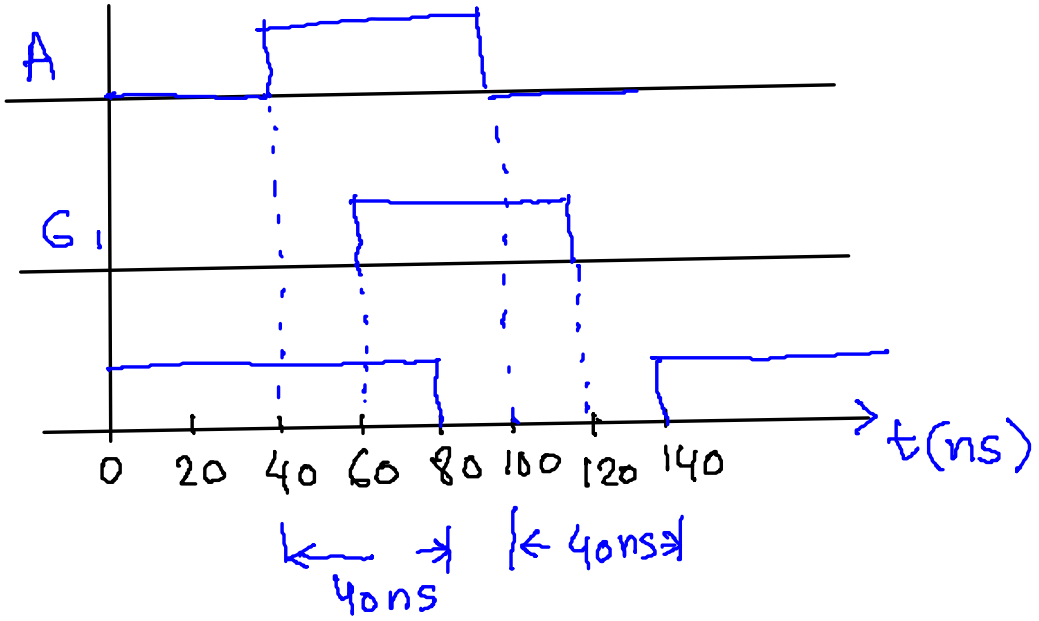
typical $\varepsilon \sim 10^{-9}$ s

Timing Diagrams

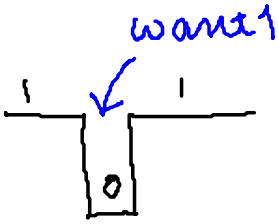


assume $\mathcal{E} = 20ns$

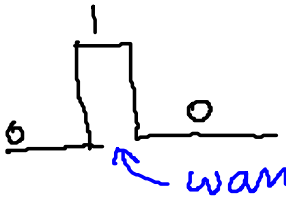
held at constant values



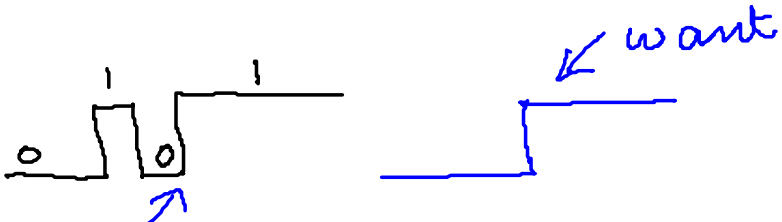
8.4 Hazards in Combinational circuits



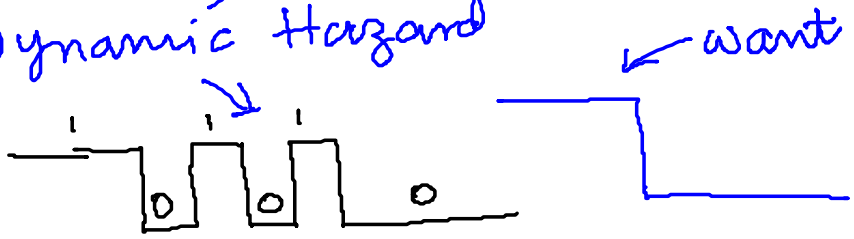
Static 1-hazard



static 0-hazard

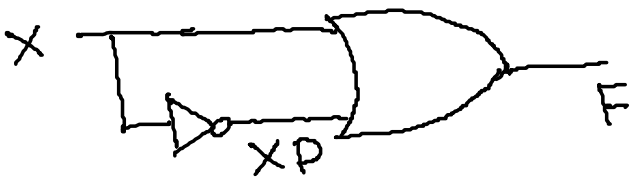


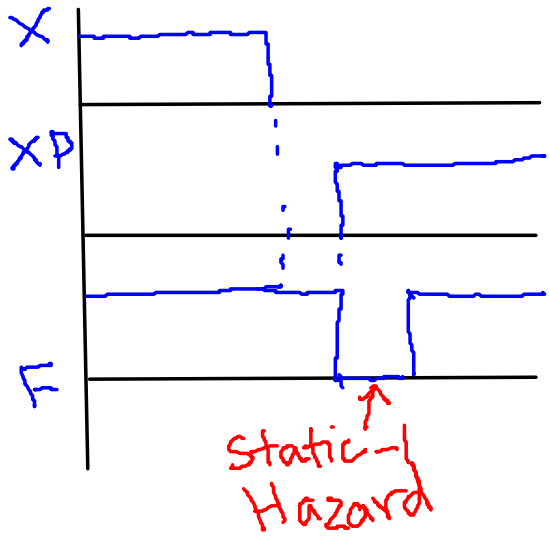
Dynamic Hazard

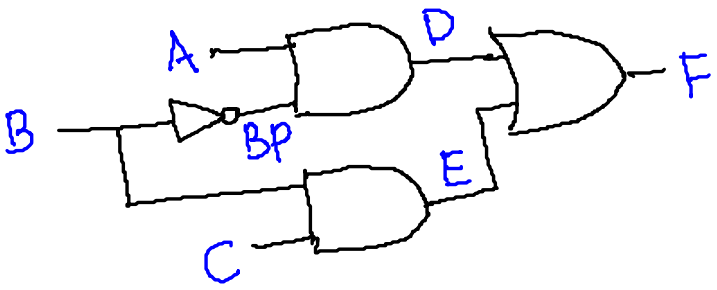


Static-1 Hazard

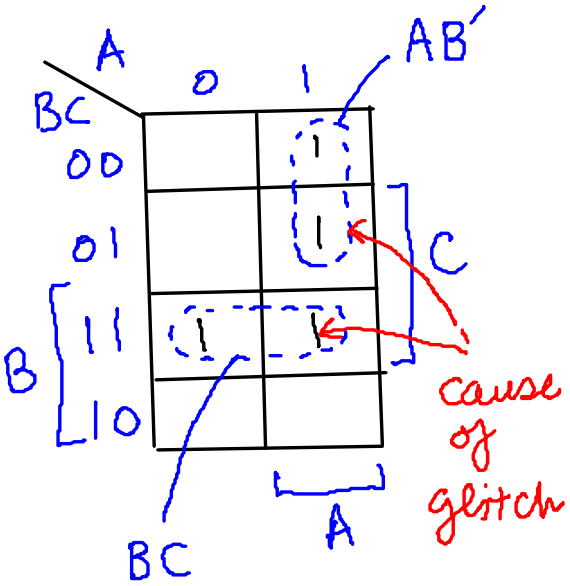
$X + X' = 1$







$F = AB' + BC$

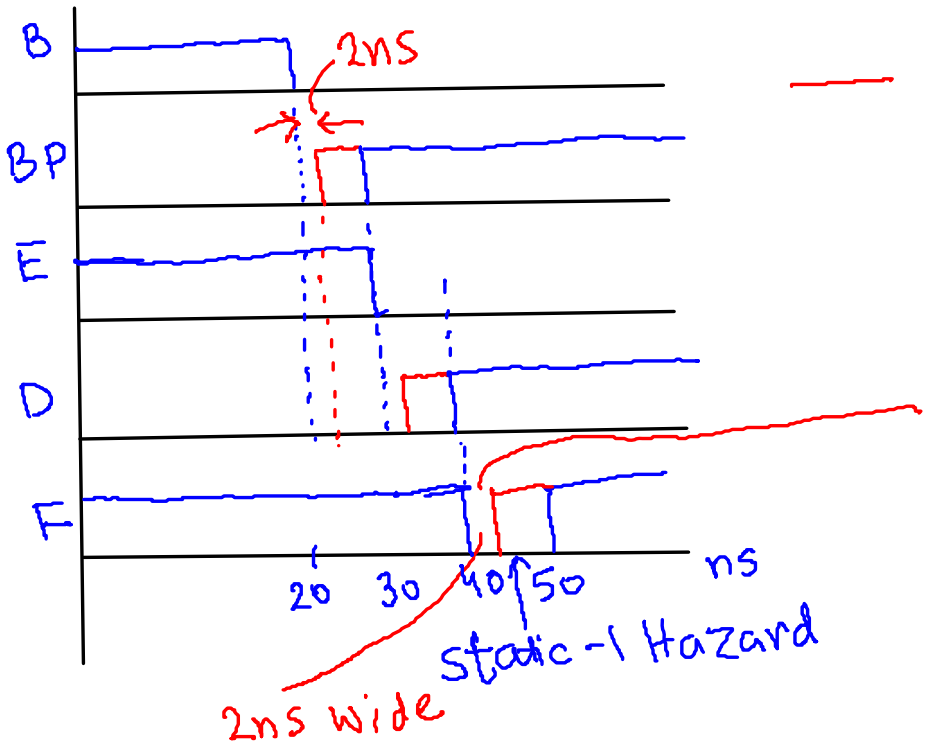


Fix A = 1 & C = 1

$F = B + B'$

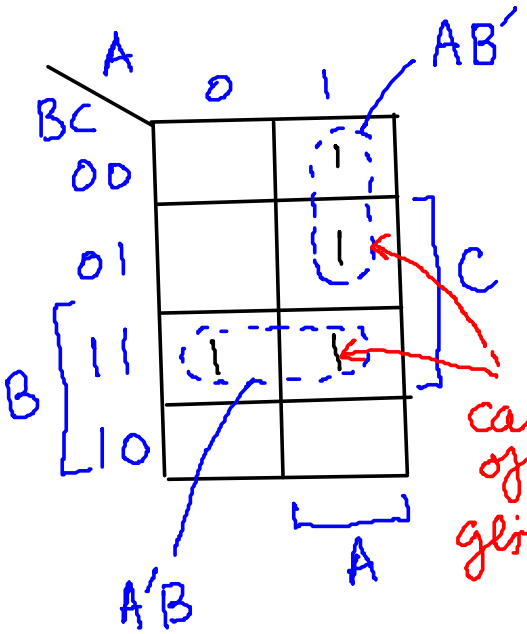
— gate delays 10ns

— not gate delay 2ms
others 10ns



this glitch might not show up if inertial delay ≥ 2ns

if inertial delay = 0 then gate is said to have ideal or transport delay



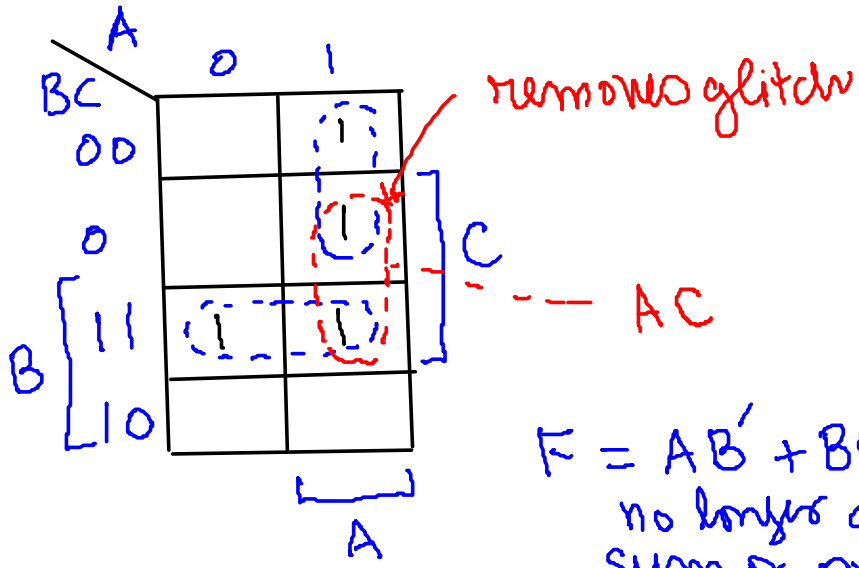
$ABC + AB'C$

$= AC(B+B')$

set $A=1, C=1$

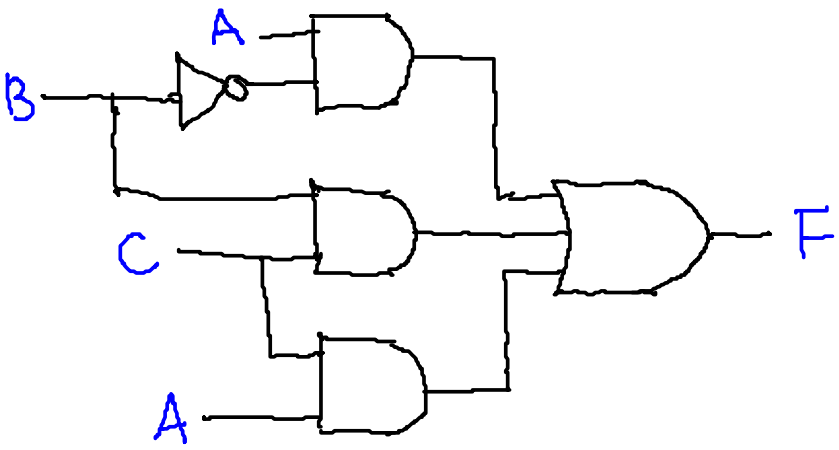
$= B+B'$

If any two adjacent 1's are not covered by the same rectangle, a 1-hazard exists



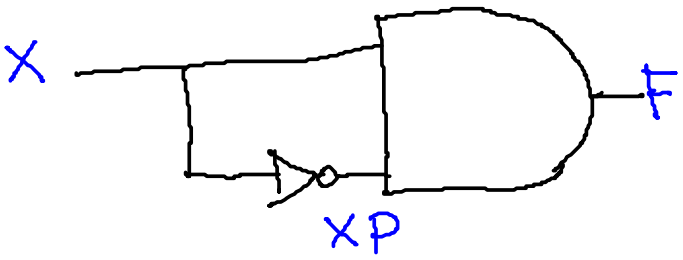
$F = AB' + BC + AC$

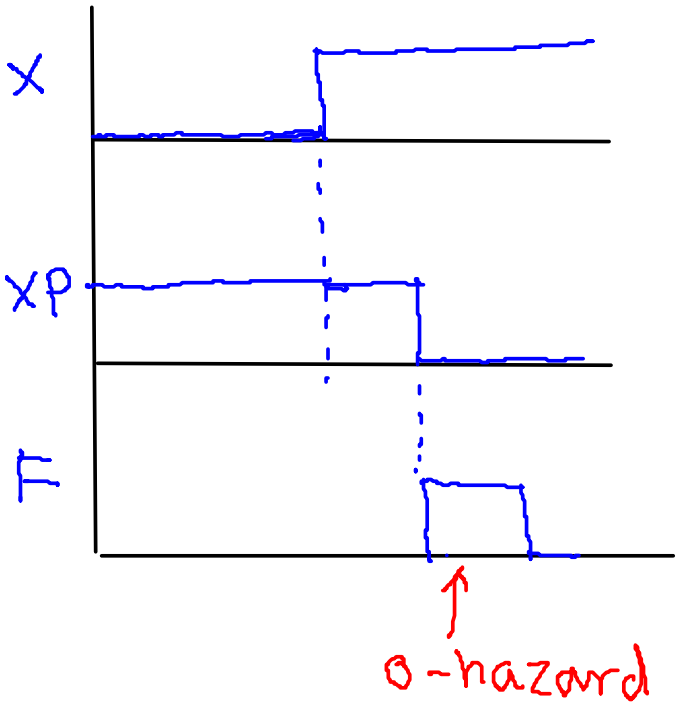
no longer a minimum sum of products



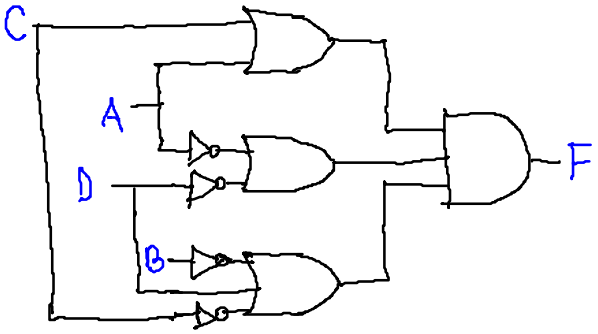
Zero hazards

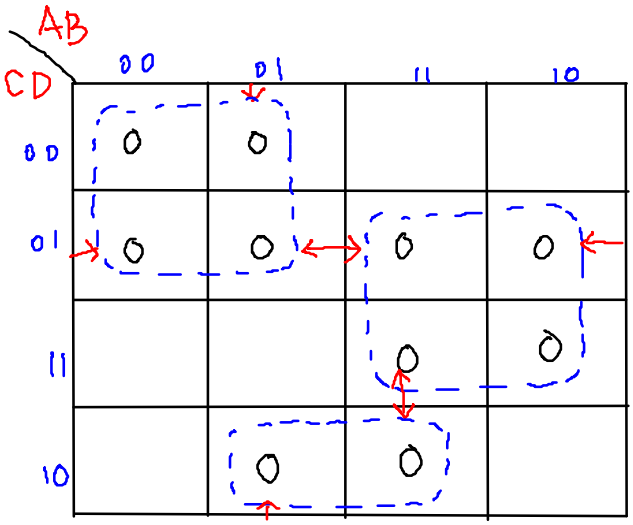
$XX' = 0$





$$F = (A + C)(A' + D')(B' + C' + D)$$



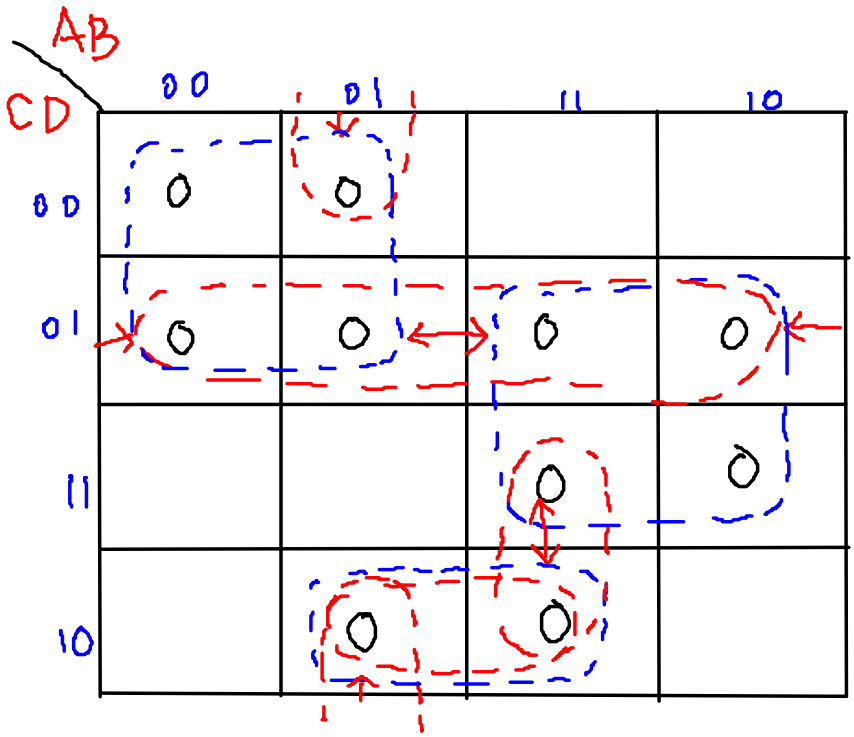


A = 0, B = 1, D = 0 & C hanges from 0 to 1

$F = (A + C)(A' + D')(B' + C' + D) = CC'$ ← glitch

See fig. (c) page 226

Eliminate glitch



$$F = (A + C)(A' + D')(B' + C' + D)(C + \bar{D})(A + B' + D)(A' + B' + C')$$