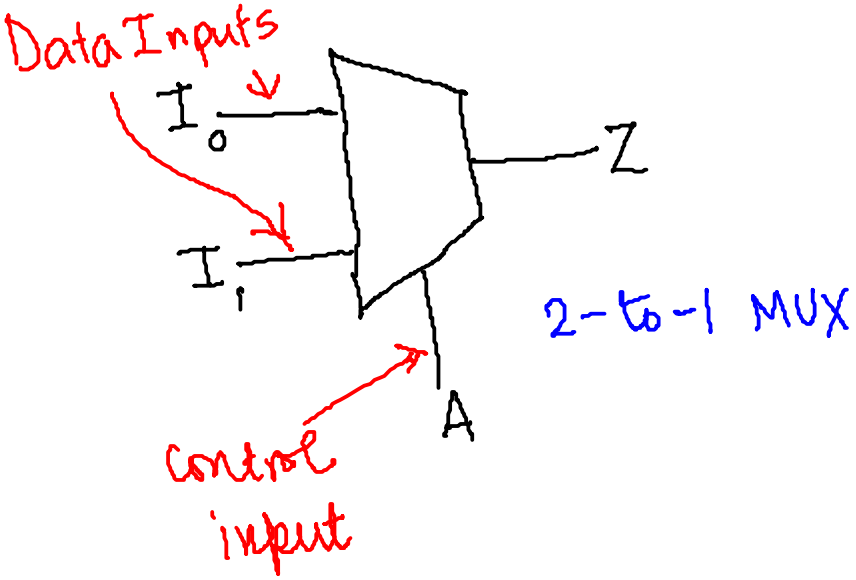
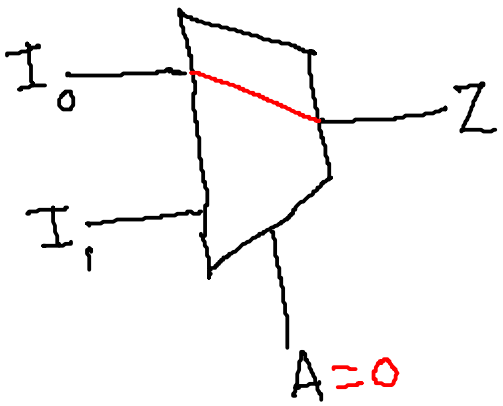
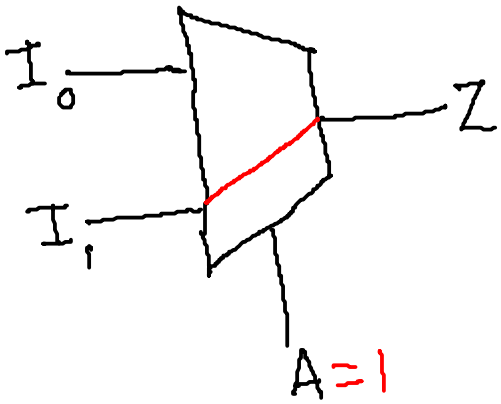
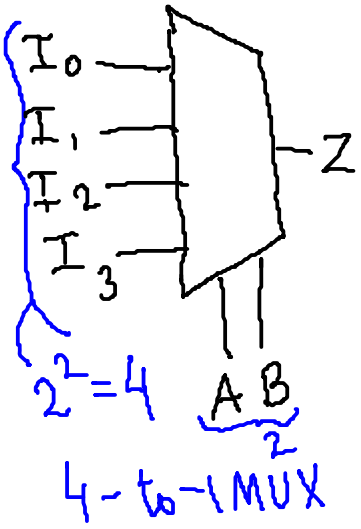
9.2 Multiplexers (MUX)

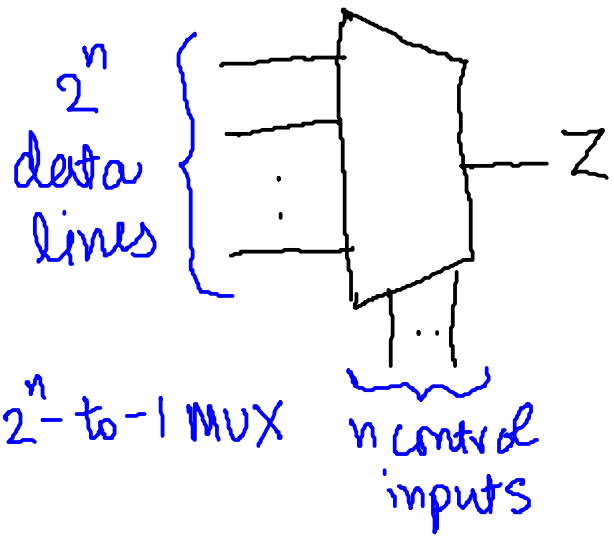


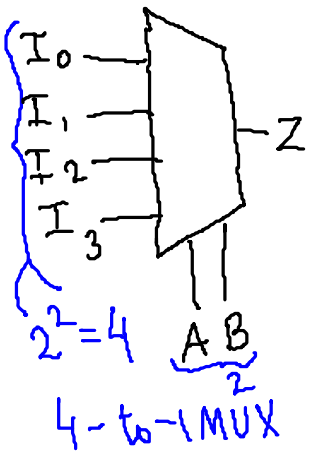




$$Z = A'I_0 + AI_1$$



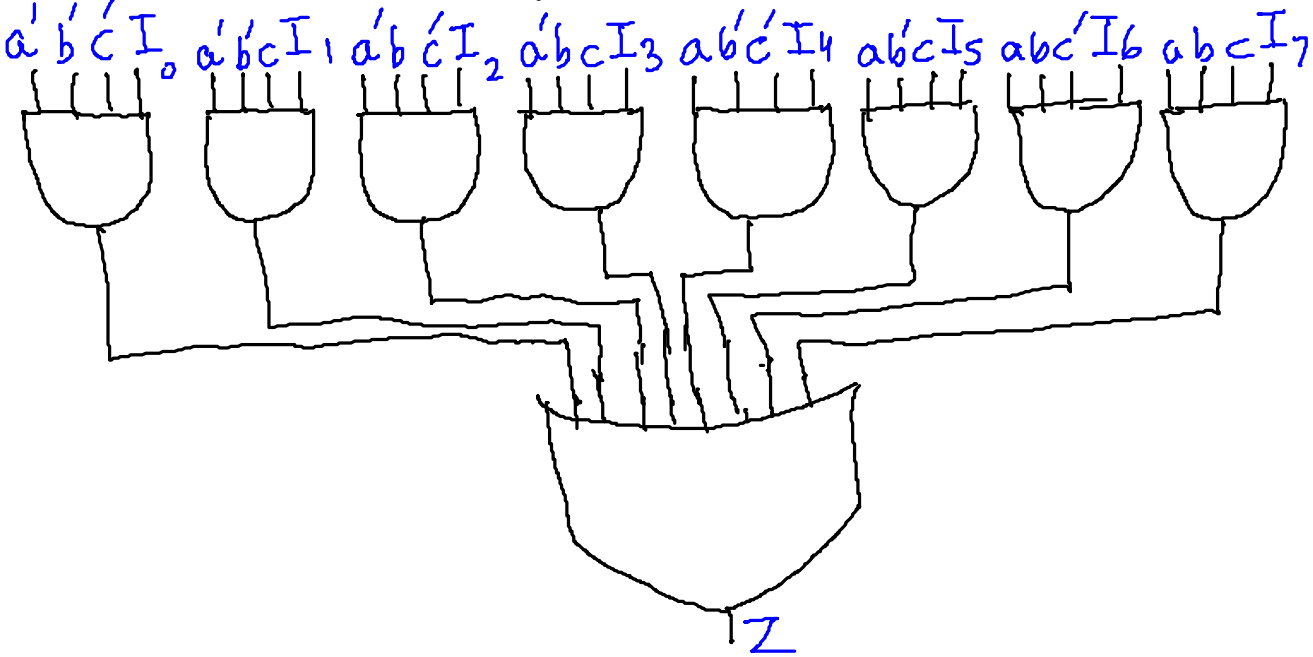


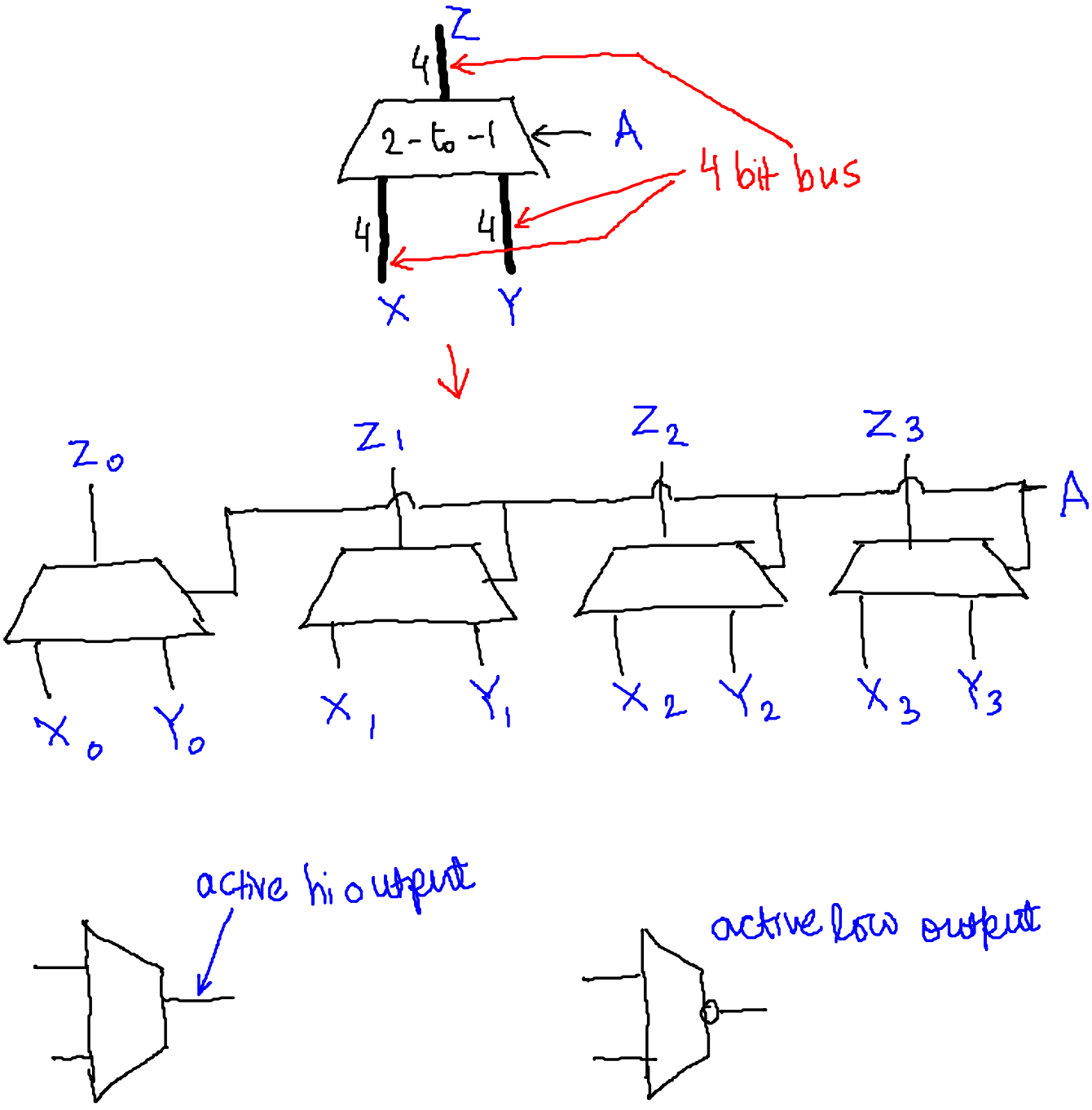


$$Z = \underbrace{A'B'}_{m_0} I_0 + \underbrace{A'B}_{m_1} I_1 + \underbrace{AB'}_{m_2} I_2 + \underbrace{AB}_{m_3} I_3$$

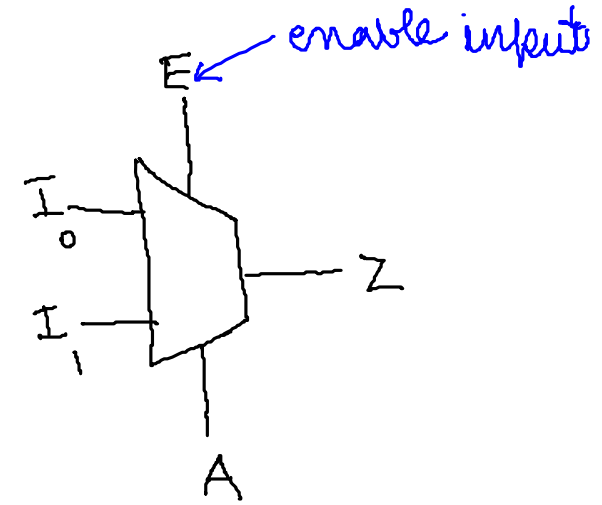
minterms

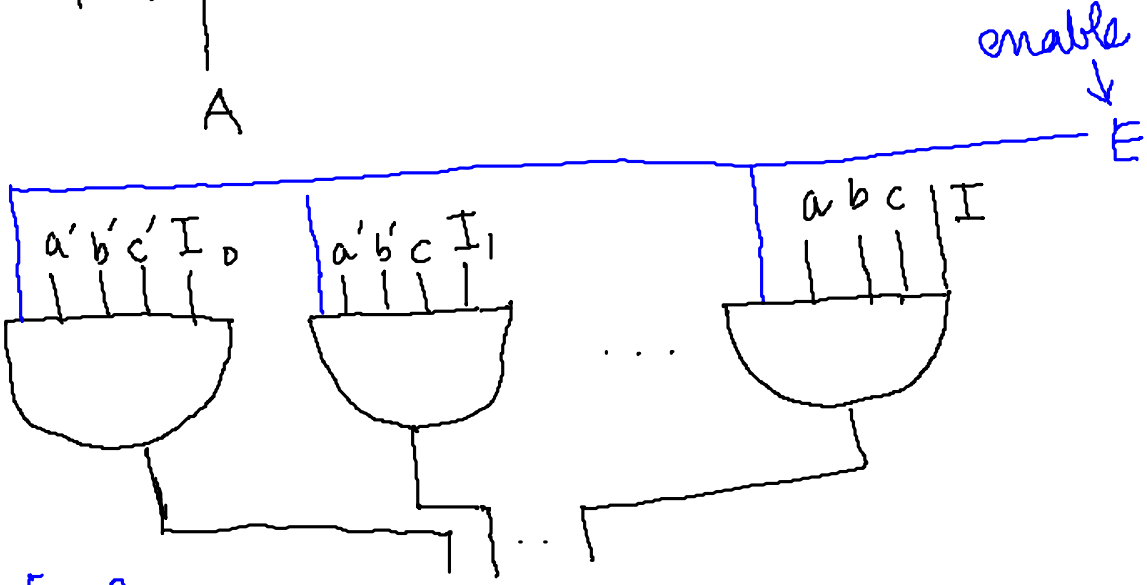
$$Z = \sum_{k=0}^{2^n-1} m_k I_k \qquad 2^n\text{-to-1 MUX}$$




Z
4
2-to-1
A
4 bit bus
4
4
X
Y
Z0
Z1
Z2
Z3
A
X0
Y0
X1
Y1
X2
Y2
X3
Y3

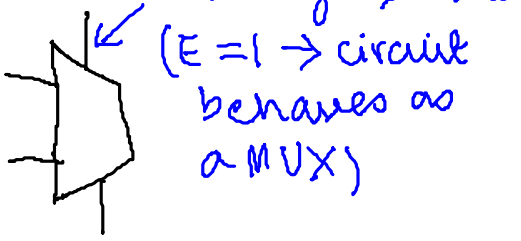
active hi output
active low output

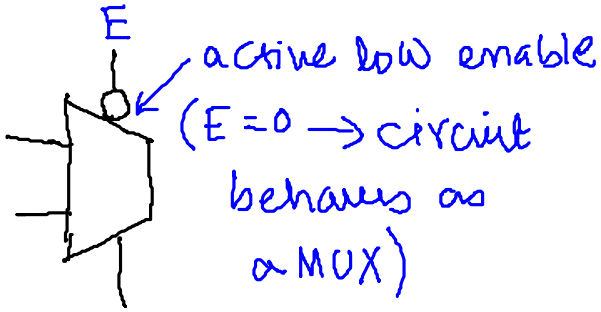




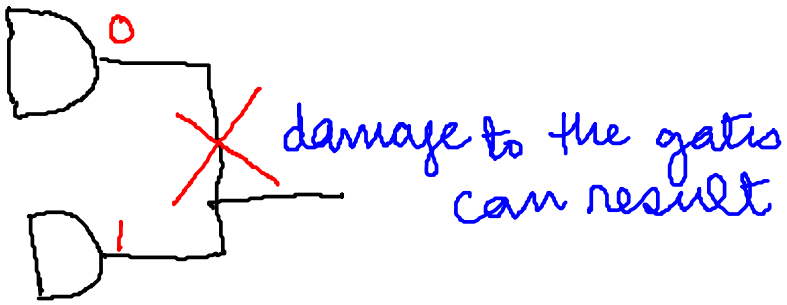
E = 0 Z = 0 independent of inputs (MUX disabled)

E = 1 MUX behaves normally (MUX enabled)

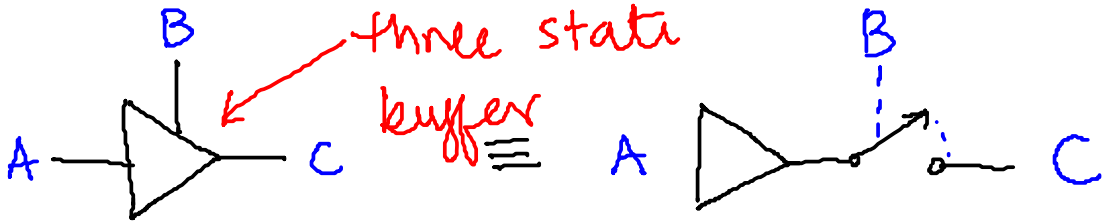




9.3 Three State Buffers



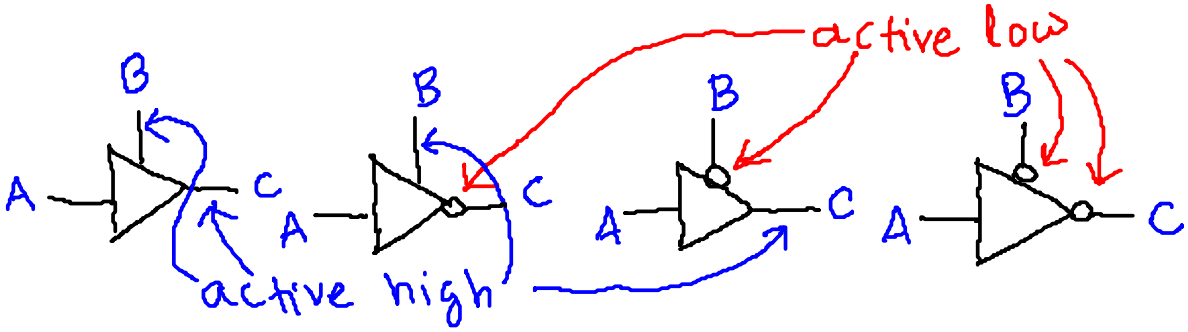
Three state logic



$B = 1 \Rightarrow C = A$

$B = 0 \Rightarrow C = hiz$ infiniteZ

$C \rightarrow \{0, 1, Z\}$



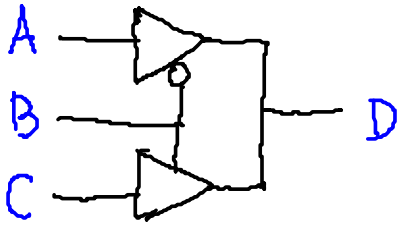
B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

B	A	C
0	0	Z
0	1	Z
1	0	1
1	1	0

B	A	C
0	0	
0	1	
1	0	
1	1	

B	A	C
0	0	1
1	1	0
Z	0	Z
Z	1	Z

Data selection



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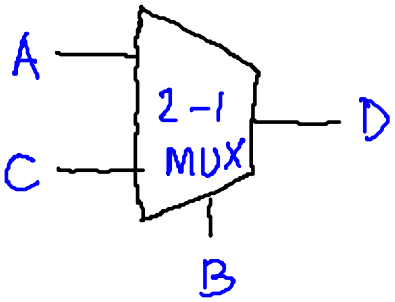
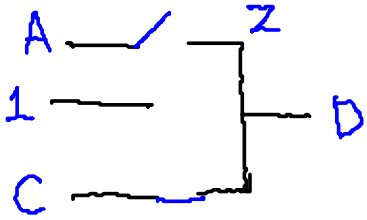
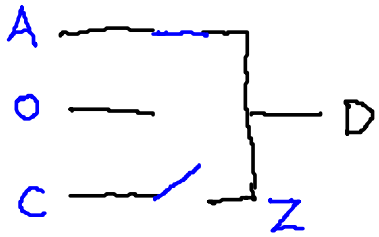
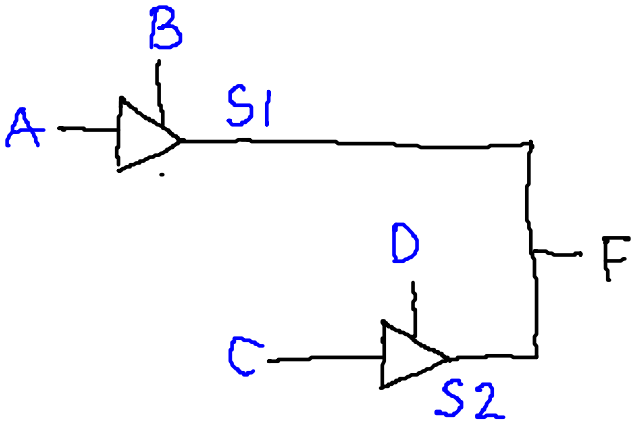
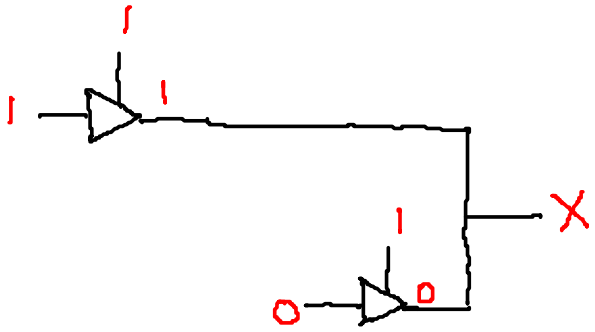




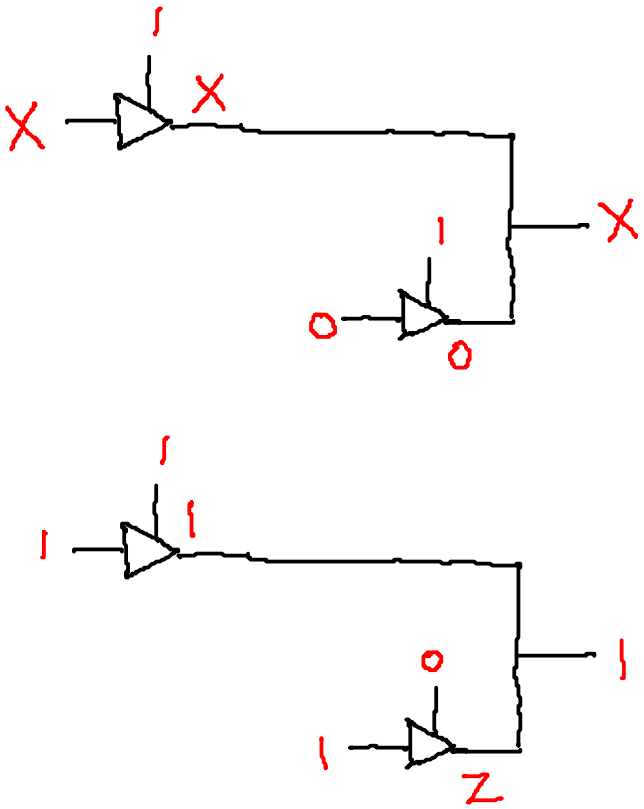




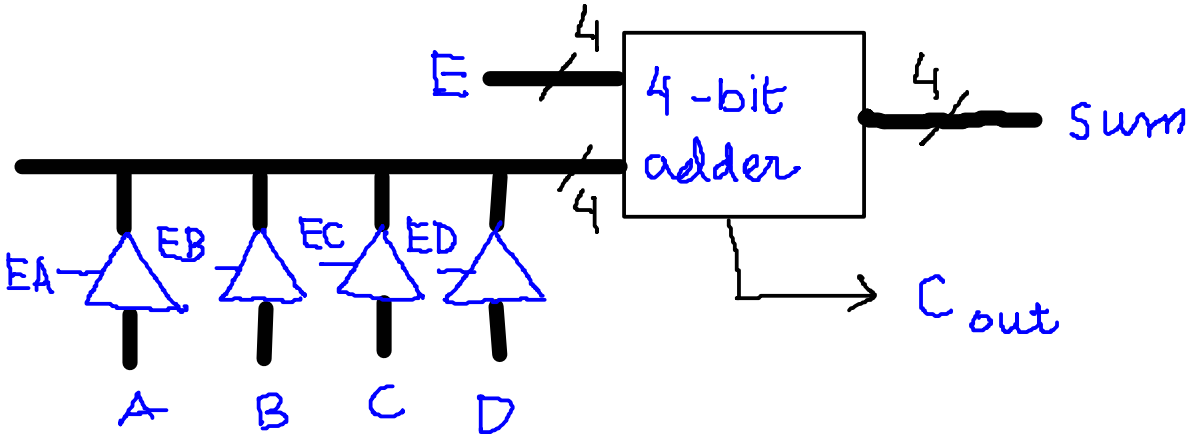
S2				
S1	X	0	1	Z
X	X	X	X	X
0	X	0	X	0
1	X	X	1	1
Z	X	0	1	Z



X (unknown)



4 Bit adder with 4 sources



Bidirectional pins