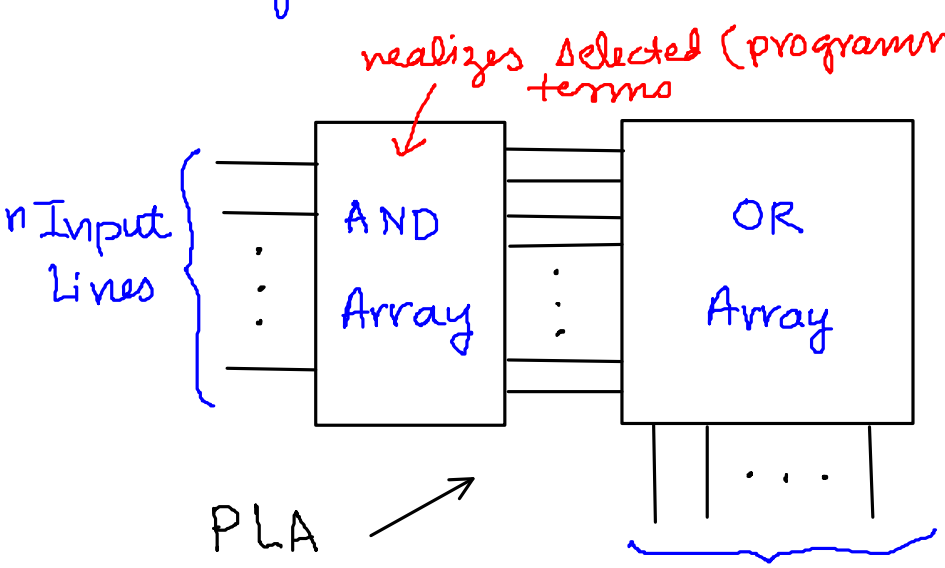
9.6 Programmable Logic Devices (PLD)

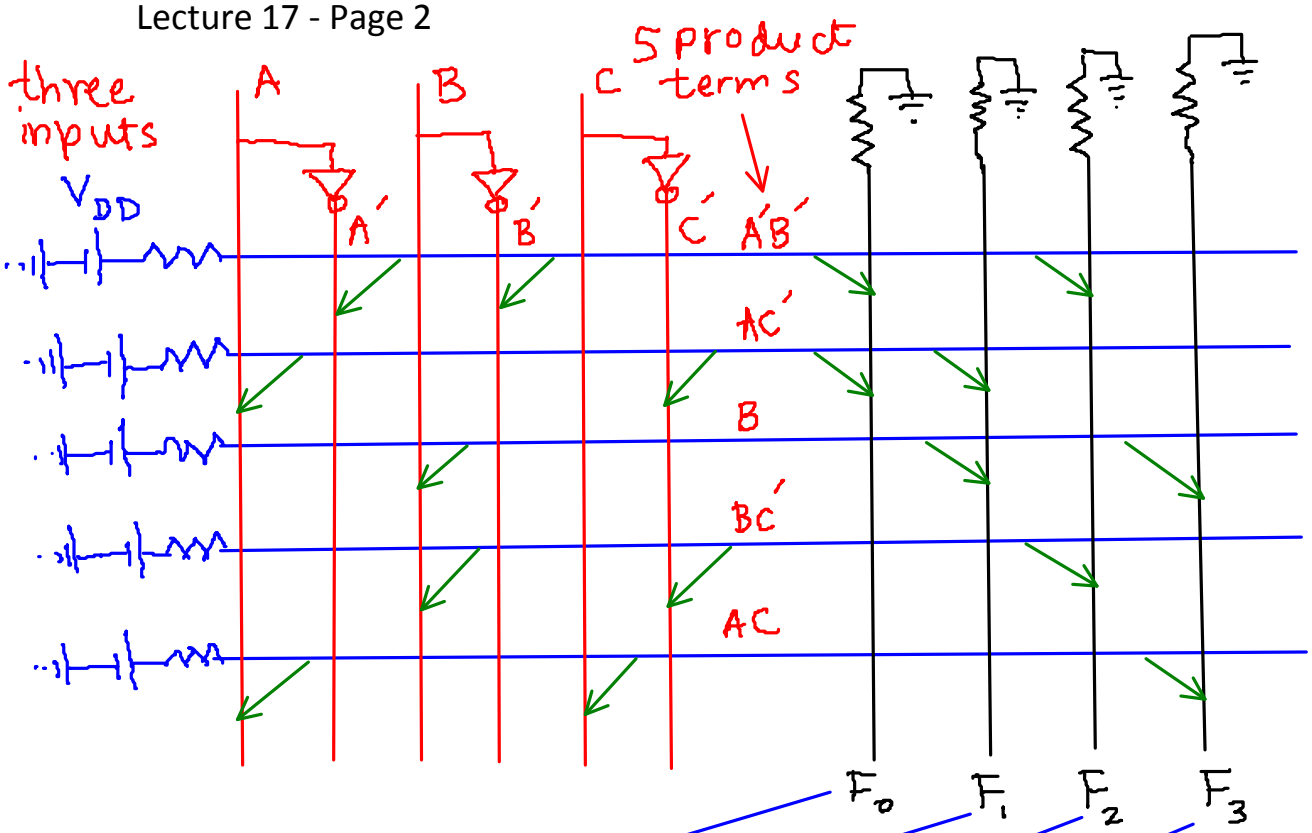
PLA (Programmable Logic Arrays)



Can realize m functions of n variables

same basic function as a ROM, but implements sum of product expressions (instead of sum of minterms)

ROM directly implements the truth table (sum of minterms)



$F_0 = A'B' + AC'$

$F_1= B + AC'$

$F_2 = A'B' + BC'$

$F_3 = AC + B$

4 outputs

PLA TABLE

variable complemented

variable not present

Product Term	Inputs A B C	F_0	F_1	F_2	F_3	
$A'B'$	0 0 –	1	0	1	0	$F_0 = A'B' + AC'$
AC'	1 – 0	1	1	0	0	$F_1 = AC' + B$
B	– 1 –	0	1	0	1	$F_2 = A'B' + BC'$
BC'	– 1 0	0	0	1	0	$F_3 = B + AC$
AC	1 – 1	0	0	0	1	

Variable not complemented

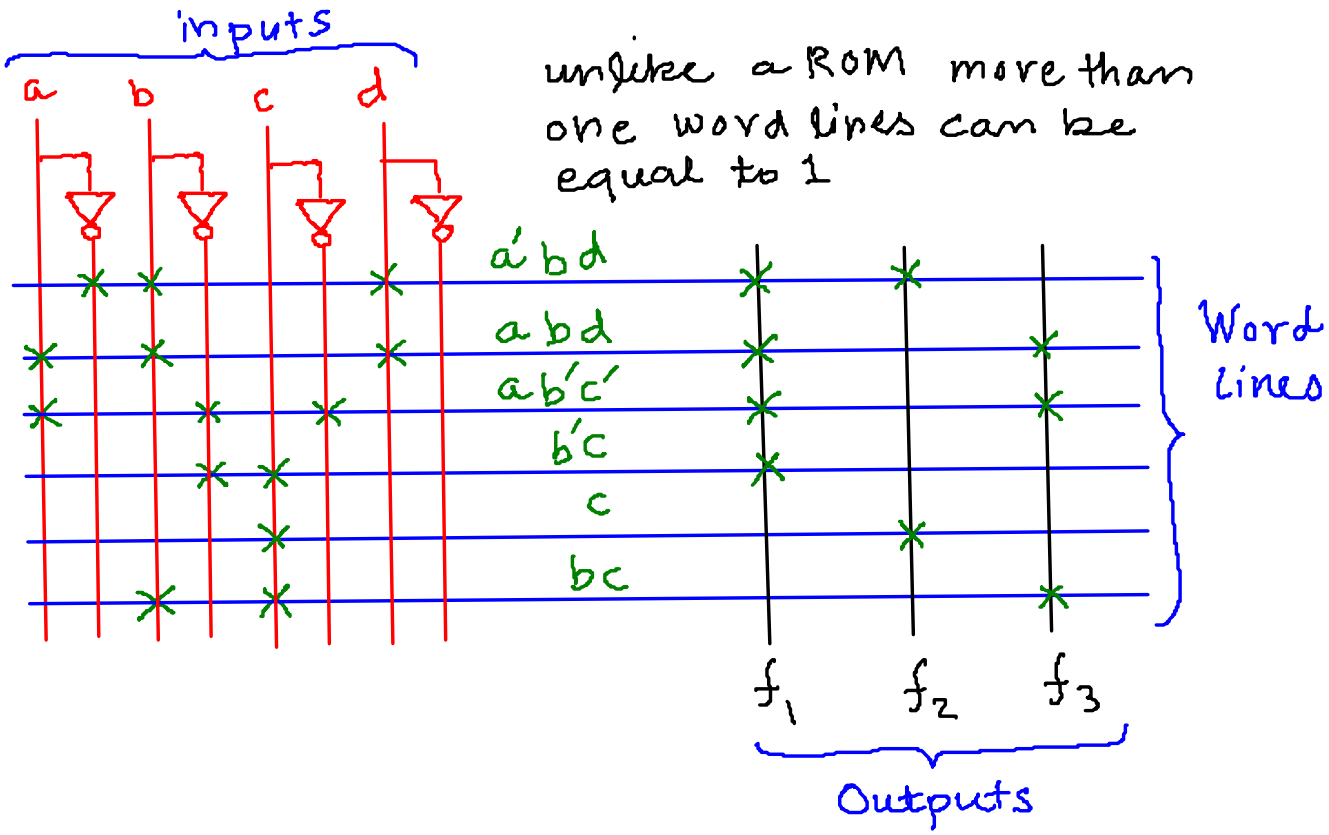
Example:

$f_1 = a'bd + abd + ab'c' + b'c$

$f_2 = c + a'bd$

$f_3 = bc + ab'c' + abd$

	a	b	c	d	f_1	f_2	f_3
$a'bd$	0	1	–	1	1	1	0
abd	1	1	–	1	1	0	1
$ab'c'$	1	0	0	–	1	0	1
$b'c$	–	0	1	–	1	0	0
c	–	–	1	–	0	1	0
bc	–	1	1	–	0	0	1

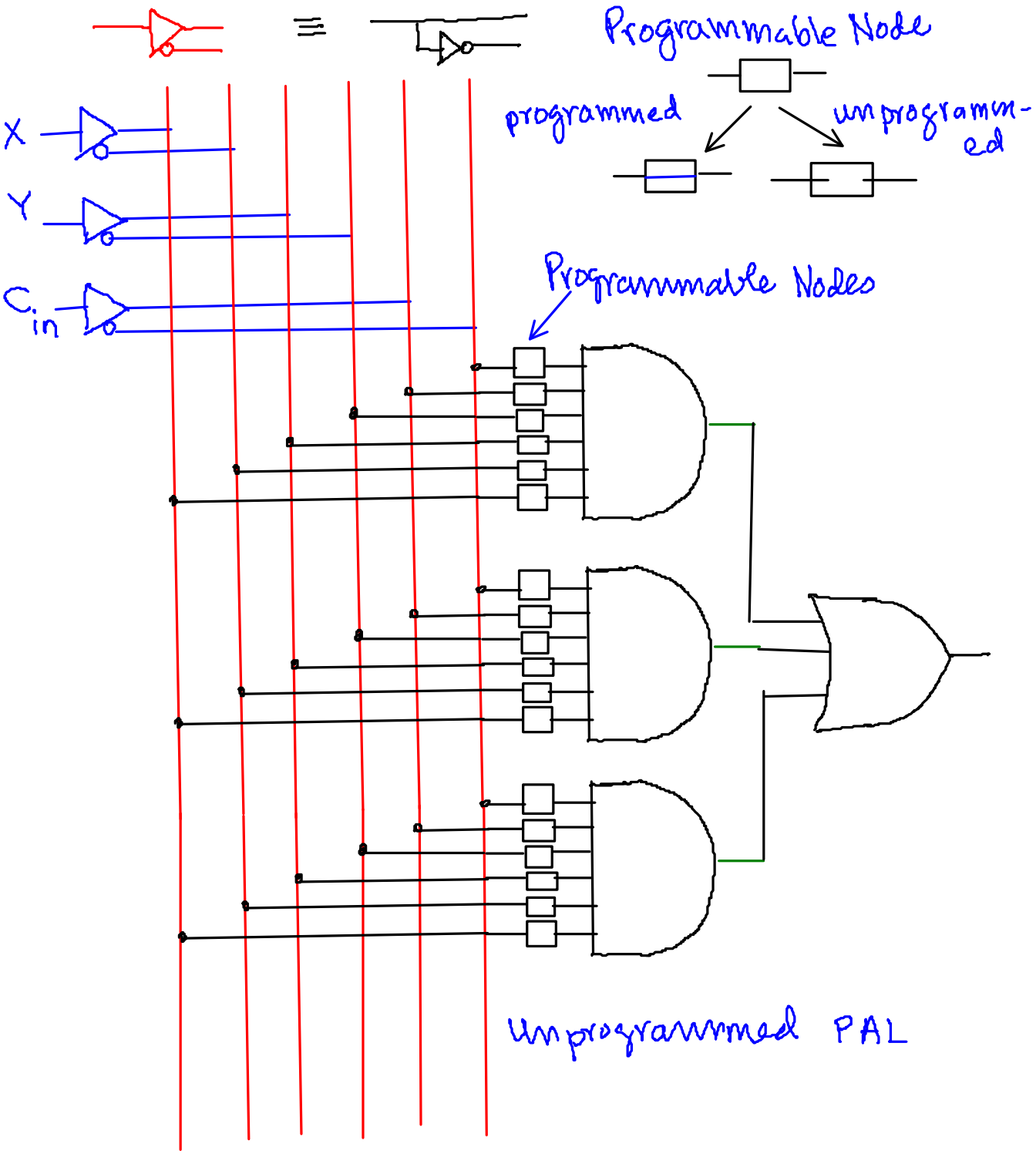


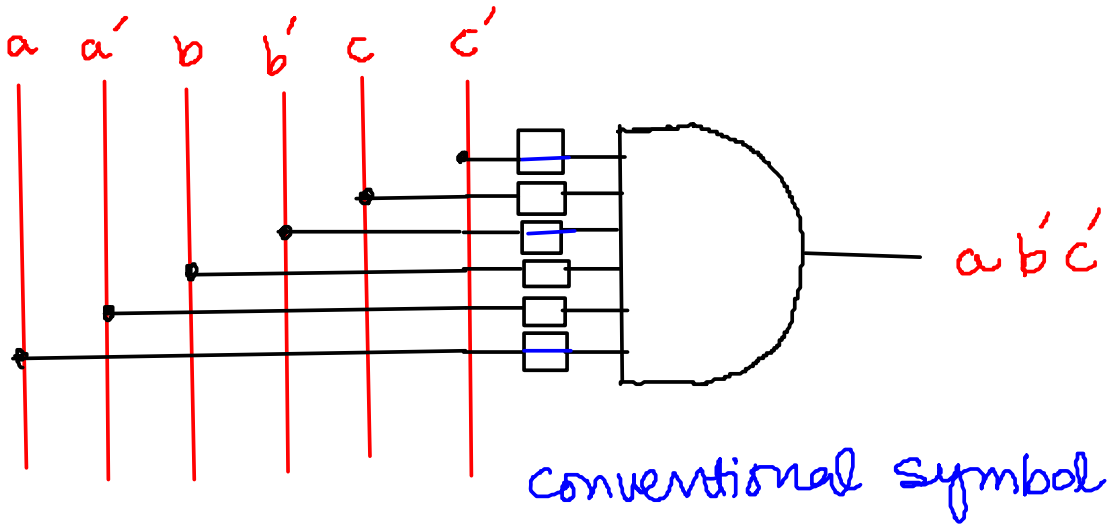
When the number of inputs is small a PROM may be more economical than a PLA.

To realize eight functions of 24 variables would require a PROM of $2^{24} \sim 16$ Million 8 bit words!

The outputs of several PLAs can be ORed together to handle bigger functions

Programmable Array Logic (PAL)





conventional symbol

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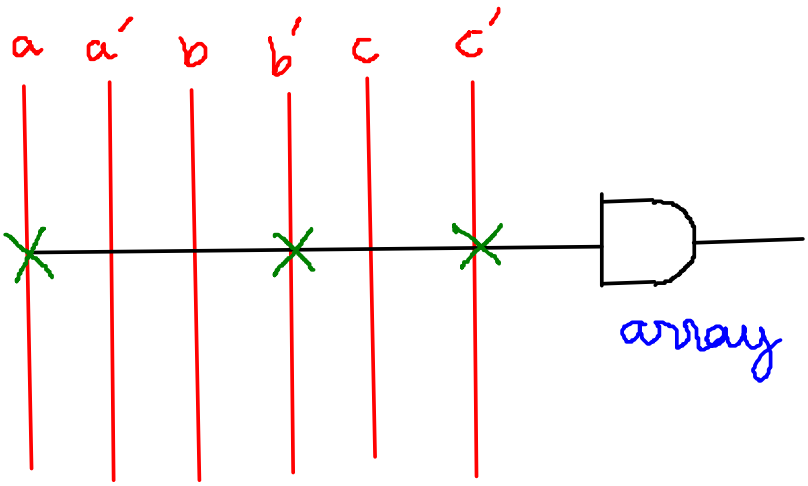
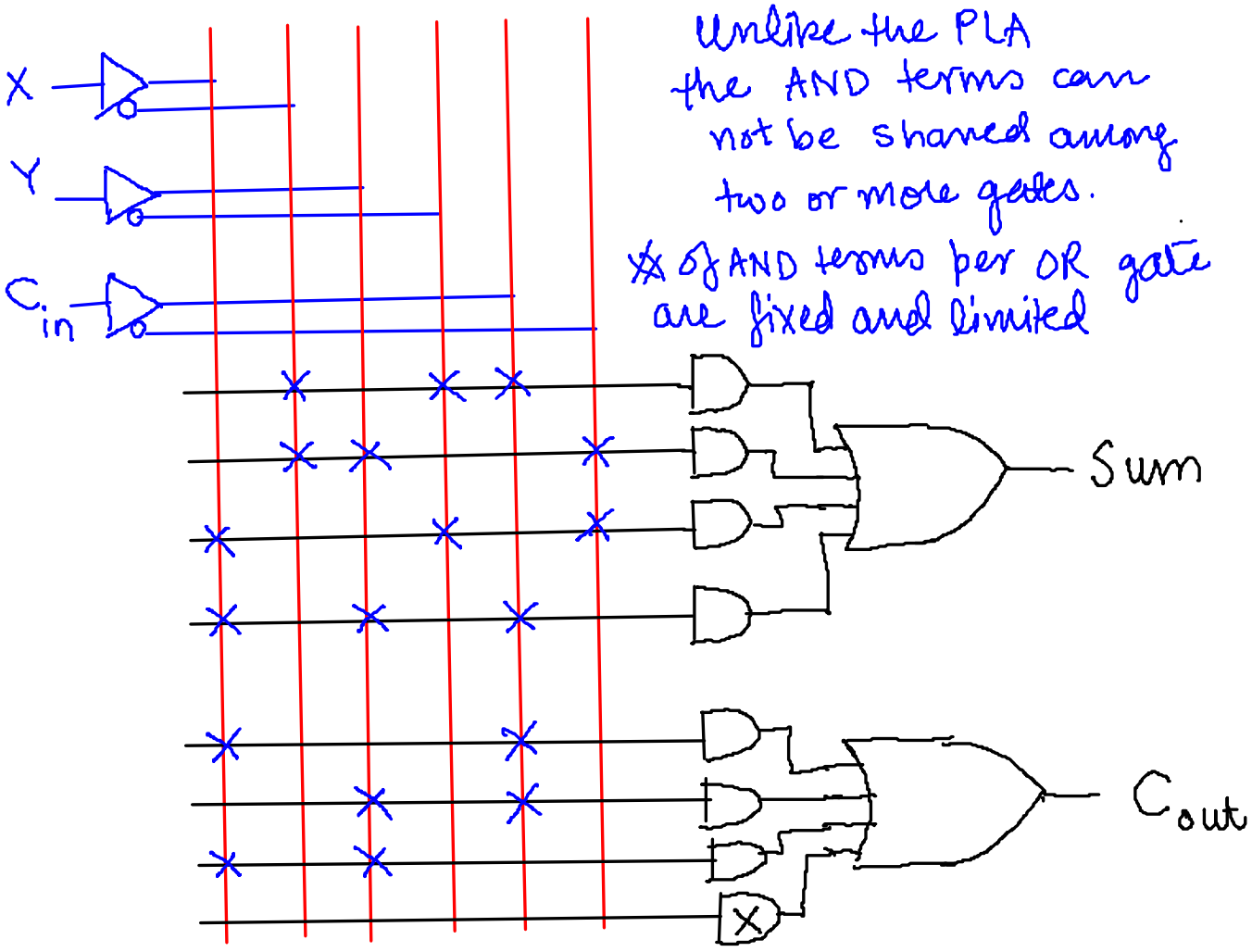


array logic symbol

$$Sum = X'Y'C_{in} + X'YC_{in}' + XY'C_{in}' + XYC_{in}$$

$$C_{out} = XC_{in} + YC_{in} + XY$$



Unlike the PLA the AND terms can not be shared among two or more gates.

# of AND terms per OR gate are fixed and limited