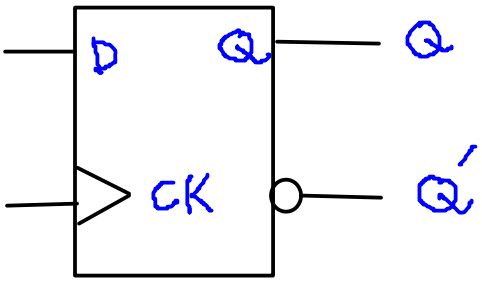
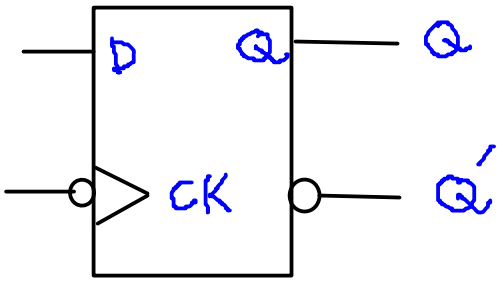
11.4 Edge Triggered D Flip-Flop



Rising Edge Trigger

active edge



Falling Edge trigger

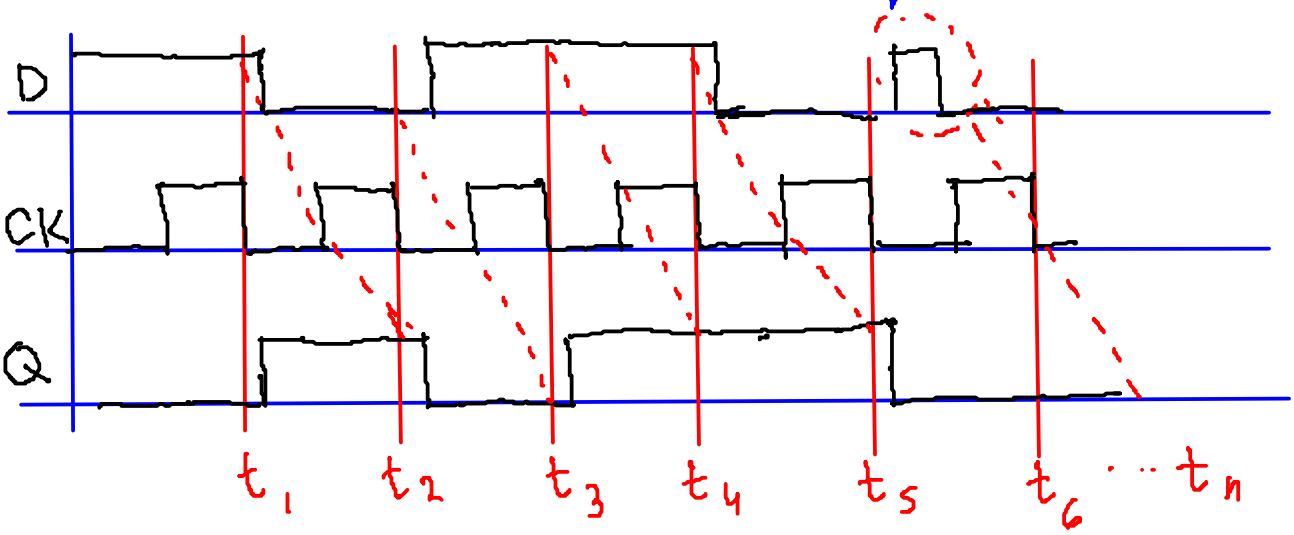
active edge

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

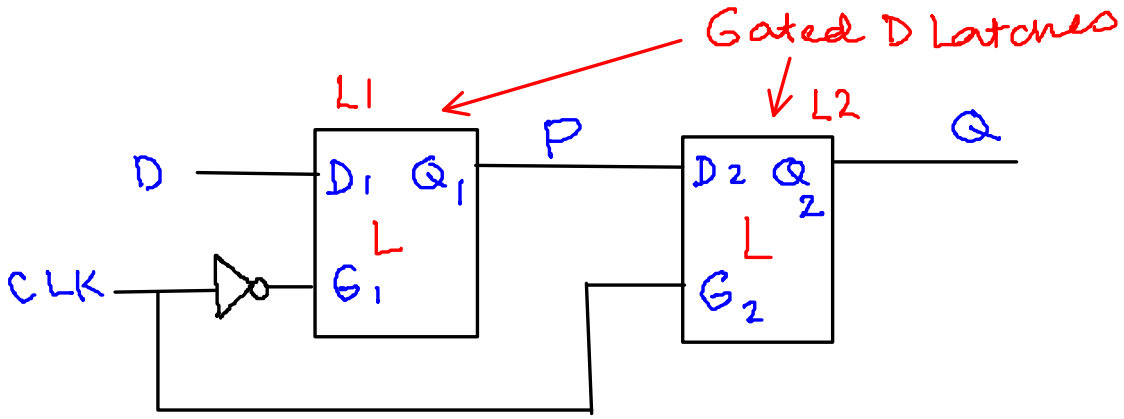
Q^+ ← after the active edge of the clock

$Q^+ = D$ ← at the active edge of the clock

↑ Characteristic equation



$Q(n) = D(n-1)$ ← unity delay



Gated D Latch: $G = 0 \rightarrow$ holds state

$G = 1 \rightarrow$ becomes transparent

$Q(t + \varepsilon) = D(t)$

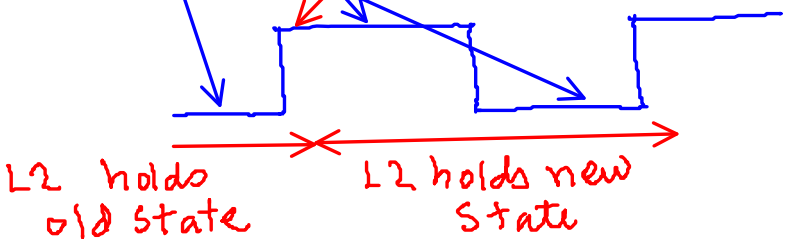
CLK = 0 L1 transparent, L2 holds old state

CLK = 1 L1 holds new state, L2 becomes transparent

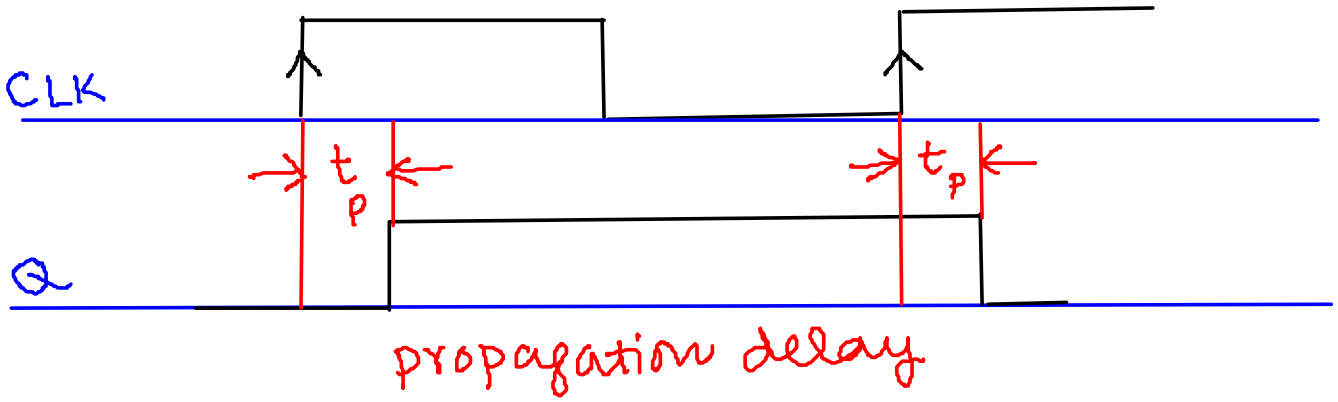
New state flows from L1 to L2

Shortly after the rising edge of the clock

CLK = 0 L1 becomes transparent, L2 holds new state

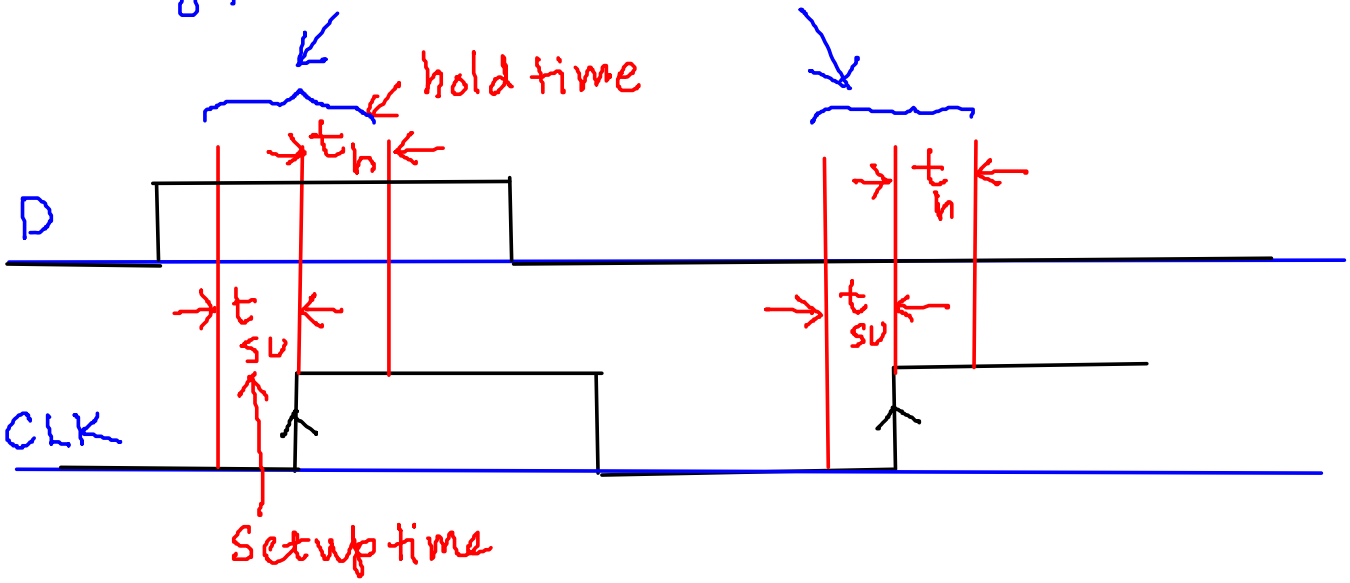


Q is delayed by propagation delay



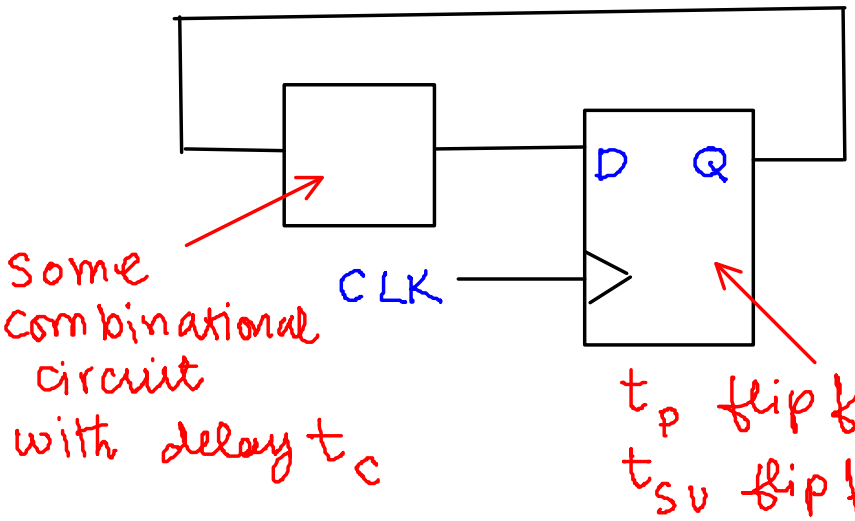
propagation delay

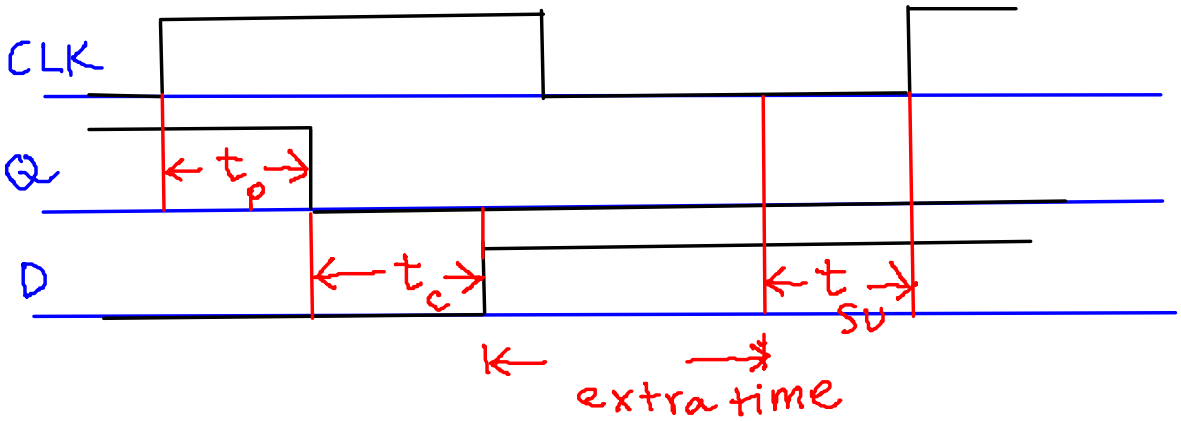
D should remain stable (should not change) in this interval



Setup time

Determination of Minimum clock period

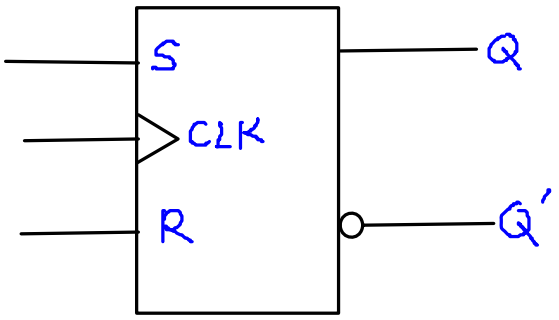




$$T_{CLK} \geq t_p + t_c + t_{su}$$

Fastest circuit with $T_{CLK} = t_p + t_c + t_{su}$

S-R Flip-Flop



$S = R = 0$ No state change

$S = 1, R = 0$ Q set to 1 after active edge of the clock

$S = 0, R = 1$ Q reset to 0 after active edge of the clock

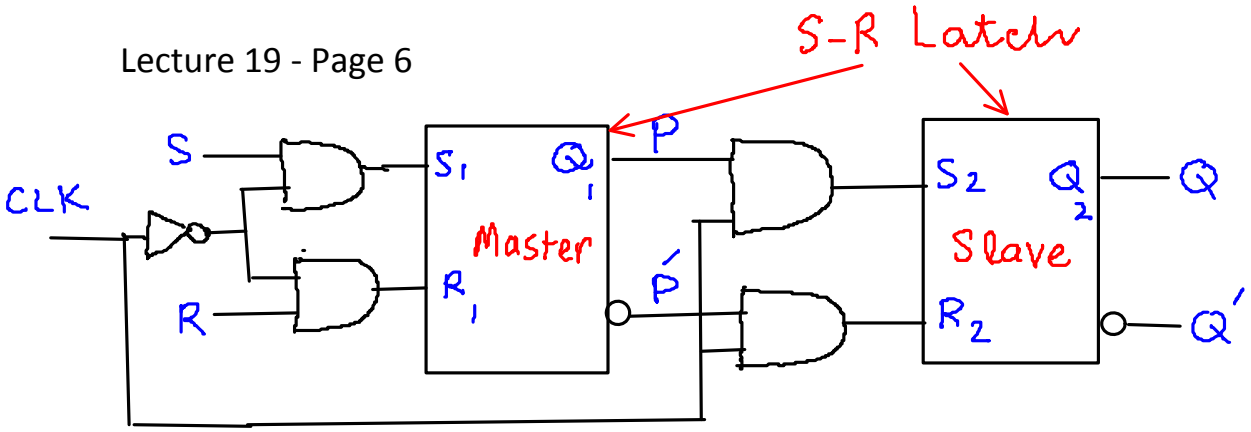
$S = 1, R = 1$ Not allowed

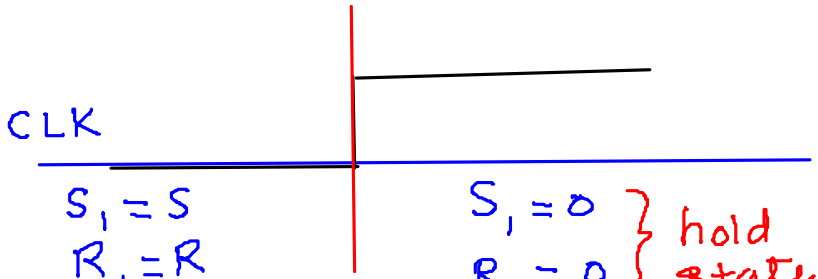
Characteristic equation

$Q^+ = S + R'Q$ ← same as S-R Latch

Q^+: Shortly after the active edge

$S + R'Q$: at the active edge





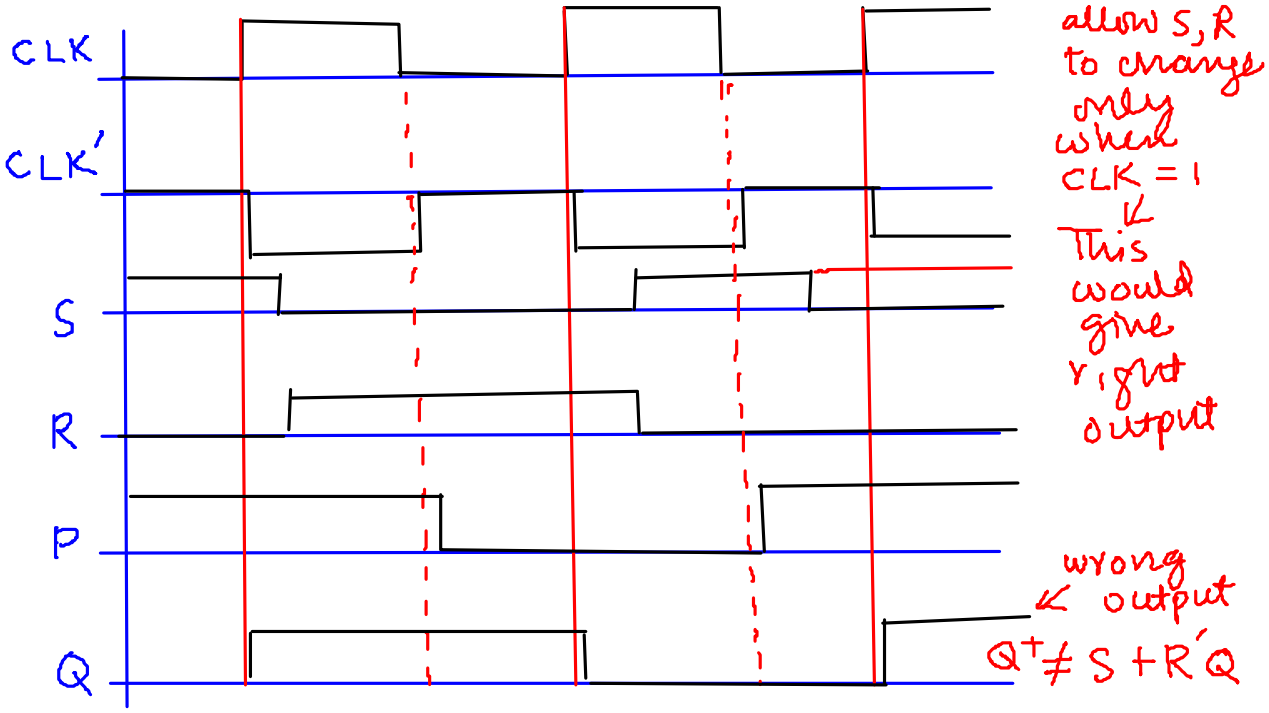
$S_1 = S$
$R_1 = R$

Hold state Q_2: $S_2 = 0$, $R_2 = 0$

$S_1 = 0$, $R_1 = 0$ } hold state Q_1

$S_2 = P = Q_1$

$R_2 = P' = Q_1'$



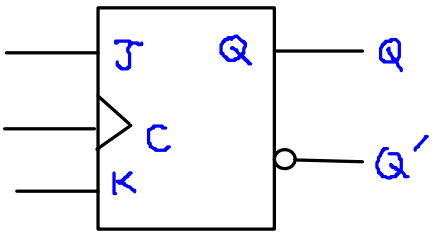
allow S, R to change only when CLK = 1

This would give right output

wrong output

$Q^+ \neq S + R'Q$

11.6 J-K Flip-Flop



extended version of S-R FF

J ↔ S
K ↔ R

J=1, K=0 $Q^+ = 1$
K=1, J=0 $Q^+ = 0$
K=1, J=1 $Q^+ = Q'$

allowed

next state table

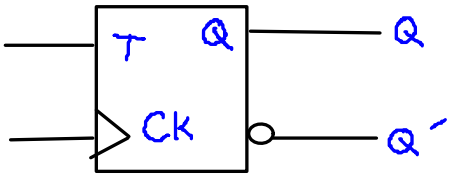
J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q^+ = JQ' + K'Q$

characteristic eq.

see figure 11-20 (c) for timing diagram

11.7 T Flip Flop (Toggle FF)



$T=1 \quad Q^+ = Q'$

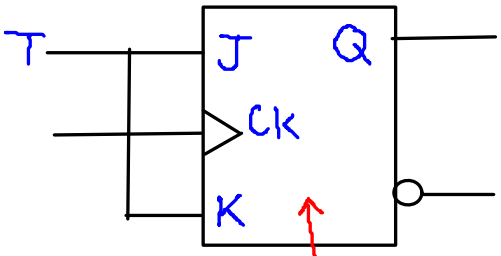
$T=0 \quad Q^+ = Q$

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$Q^+ = T'Q + TQ' = T \oplus Q$

characteristic eq.

See figure 11-23 for timing diagram example

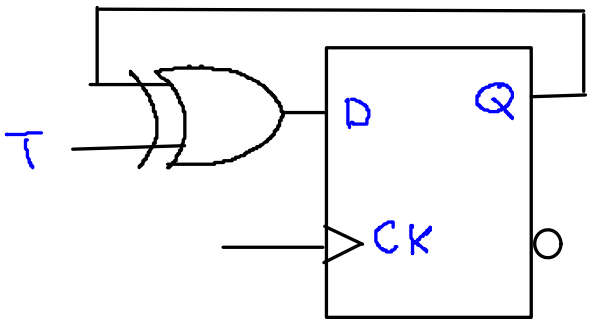


Conversion of J-K to T

$Q^+ = JQ' + K'Q$ (J-K)

$J=T, \; K=T$

$Q^+ = TQ' + T'Q = T \oplus Q$ (T)



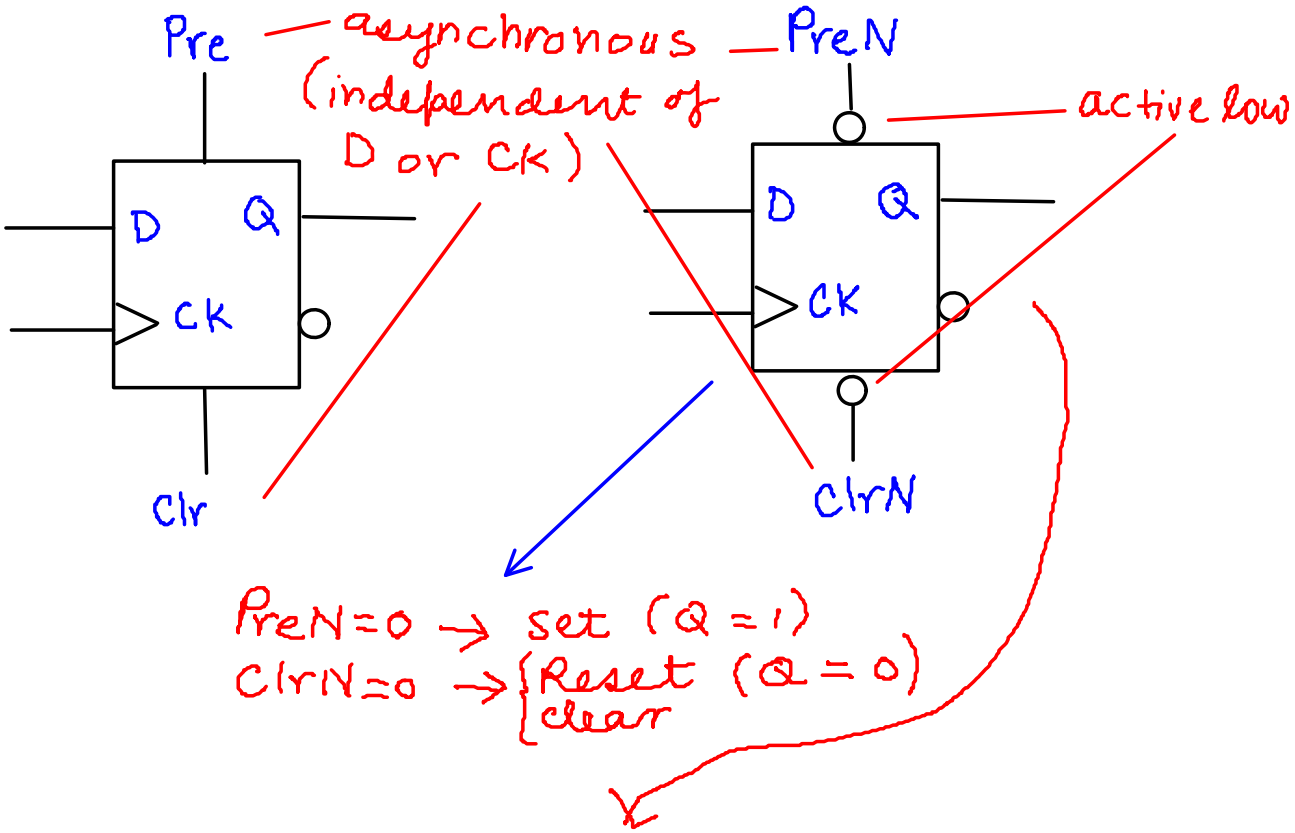
Conversion of D to T

$Q^+ = D$ (D)

$D = Q \oplus T$

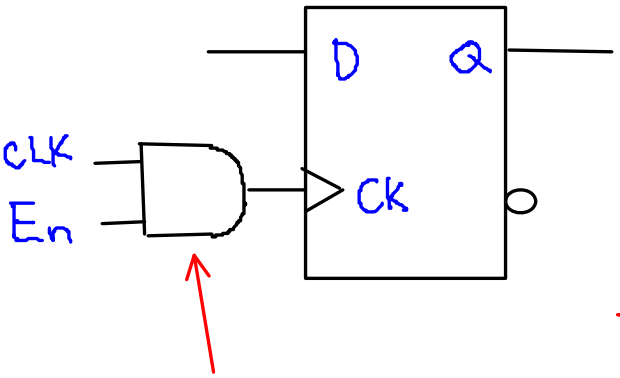
$Q^+ = Q \oplus T$ (T)

11-8 Flip-Flops with additional inputs



CK	D	PreN	ClrN	Q^+
x	x	0	0	not allowed
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0, 1, ↓	x	1	1	no change

Clock enable

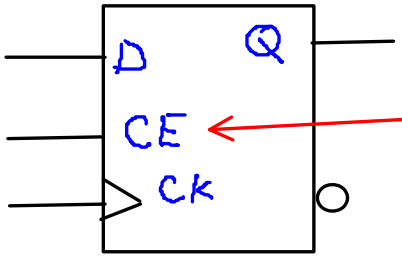


$E_n = 1$ $CK = CLK$
Clock enabled
normal operation

$E_n = 0$ $CK = 0$
Clock disabled
hold state (no ↑ or ↓)

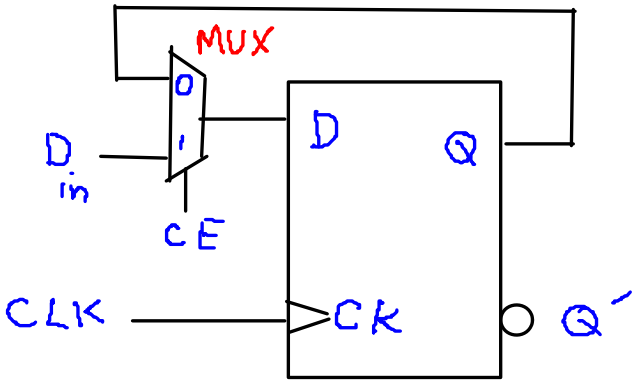
gated clock (not desirable)

D - CE FF



Clock enable

$Q = Q \cdot CE' + D \cdot CE$



MUX

$D = \underbrace{Q \cdot CE' + D_{in} \cdot CE}$

$Q^+ = D$ } DFF

$Q^+ = Q \cdot CE' + D_{in} \cdot CE$

Implementation (CK not gated)
D-CE FF