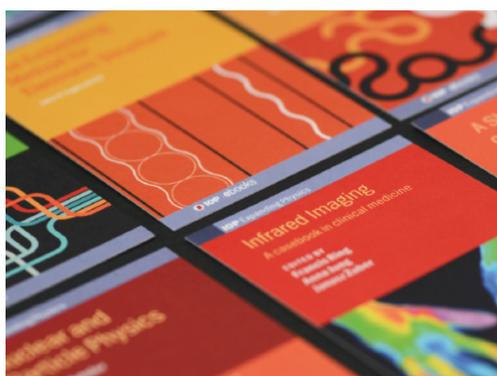


PAPER

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All-MOCVD-grown gallium nitride diodes with ultra-low resistance tunnel junctions

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Abstract

We carefully investigate three important effects including postgrowth activation annealing, delta (δ) dose and magnesium (Mg) buildup delay as well as experimentally demonstrate their influence on the electrical properties of GaN homojunction p - n diodes with a tunnel junction (TJ). The diodes were monolithically grown by metalorganic chemical vapor deposition (MOCVD) in a single growth step. By optimizing the annealing parameters for Mg activation, δ -dose for both donors and acceptors at TJ interfaces, and p^+ -GaN layer thickness, a significant improvement in tunneling properties is achieved. For the TJs embedded within the continuously-grown, all-MOCVD GaN diode structures, ultra-low voltage penalties of 158 mV and 490 mV are obtained at current densities of 20 A cm⁻² and 100 A cm⁻², respectively. The diodes with the engineered TJs show a record-low differential resistivity of $1.6 \times 10^{-4} \Omega \text{ cm}^2$ at 5 kA cm⁻².

Supplementary material for this article is available [online](#)

Keywords: GaN, tunnel junction, MOCVD, delta dose, activation

(Some figures may appear in colour only in the online journal)

1. Introduction

Since the successful demonstration of p -GaN as an active layer [1], GaN-based devices have drawn significant attention in the area of optoelectronics [2, 3] and power electronics [4, 5]. While III-nitride light emitting diodes (LEDs) have been commercially available, a long-standing challenge of reduced external quantum efficiency at higher current levels remains, which limits the usability of LEDs for high intensity applications. One way to circumvent the efficiency droop issue is to use multiple active region LEDs connected by tunnel junctions (TJs) [6]. To achieve this, it is critical to develop TJs that have low added voltage penalty across them to reduce electrical losses in such cascaded LEDs. While there have been significant efforts made over the last decade in developing

low-resistance TJs [7], there are still some challenges associated with achieving low voltage-drop TJs using metal organic chemical vapor deposition (MOCVD).

One of the major challenges for achieving low-resistivity GaN TJs via MOCVD is the activation of magnesium (Mg) dopants in the buried p -GaN layers. Hydrogen (H), which forms a stable complex with Mg acceptors, has low diffusivity through the n -type GaN layers [8, 9], and therefore, activation of p -type GaN through overlying n -type GaN layers is challenging. The well-known technique of high-temperature annealing at 725 °C enables dissociation of the Mg-H complex, and diffusion of the H species laterally, enabling an activated p -GaN layer [10, 11]. Despite the reasonably good electrical performance seen in devices with small dimensions (<50 μm) using such a high-temperature process causes

large-area devices to suffer from insufficient activation, resulting in higher voltage penalties [12–14]. The MOCVD growth-induced Mg-memory [15] and Mg buildup delay effects [15, 16] introduce added challenges towards achieving the sharp doping profiles necessary for efficient GaN TJs. Nonetheless, an all-MOCVD process is highly preferred for its efficacy in terms of providing better-quality InGaN multi quantum well-based active region, enabling high manufacturing throughput and cost-effective devices. Hence, further development of an activation annealing process for buried Mg dopants and *p*-doping engineering within the diode structure are essential so that uniform and reproducible large hole concentrations can be obtained even in large-area devices.

Among several approaches, sidewall activation of Mg:GaN layers through an optimized postgrowth annealing process is one of the simplest techniques to improve. This is usually done by exposing the buried *p*-GaN through dry-etched sidewalls. It is commonly believed that Mg activation occurs as a result of the thermal dissociation of Mg–H complexes followed by the removal of the H⁺ ions, and this process is significantly enhanced as the annealing temperature increases. Another approach to obtaining high *p*-type doping is introducing a delta (δ) dose at the doped layer interfaces [17–19]. Compared to a continuously doped layer, the δ -dose layer shows an order of magnitude higher carrier concentration. The reasons behind this improvement are reduced Mg self-compensation [18], reduction of surface defects [20] and Mg buildup delay compensation [16]. Moreover, a polarization-engineered heterostructure by inserting a thin InGaN interlayer within the TJ shows great promise for interband tunneling [21, 22]. While the InGaN interlayer leads to excellent TJ performance, its presence in transparent GaN TJs may degrade the performance of cascaded LED structures through optical absorption.

Yuka *et al* demonstrated H⁺ outdiffusion by exposing the sidewalls of the *p*-GaN layers after a mesa formation and annealing the sample at 725 °C [12]. Recently, Akatsuka *et al* demonstrated sidewall-activated GaN TJ with differential resistivity as low as $2.4 \times 10^{-4} \Omega \text{ cm}^2$ at 5 kA cm⁻² for a single run without any regrowth [23]. However, a controlled overlap between Mg and Si dopants reported in the work may affect the reproducibility of the device performance. So far, MOCVD-grown TJs [3, 13, 14] exhibit higher voltage penalty compared to structures grown by PAMBE [24, 25], either as all-MBE or hybrid MBE/MOCVD structures [26–28]. This is partly because MBE grown *p*-GaN does not suffer from H passivation. Previous state-of-the-art results on MOCVD TJs [29, 30] and MBE TJs [21, 22] employed non-transparent InGaN interlayers to achieve low TJ voltage penalty.

In this experimental study, we report a significant reduction in voltage penalties of all-MOCVD-grown and InGaN interlayer-free GaN *p*-*n* homojunction TJs. Three methods were employed and their roles towards improving the tunneling properties are carefully investigated. We first investigated the effect of postgrowth activation annealing on the TJ resistance. The remaining two methods related to doping engineering through a δ -dose for both donors and acceptors at TJ interfaces as well as optimizing *p*⁺-GaN layer thickness to

overcome the slow Mg response were also attempted. Utilizing these methods, ultra-low voltage penalties of 158 mV at 20 A cm⁻² and 490 mV at 100 A cm⁻² are achieved, which represent some of the lowest values to-date for MOCVD-based single-step grown TJs buried in GaN *p*-*n* diodes.

2. Experimental description

The *p*-*n* diode structure used in this study were grown by MOCVD in a Taiyo Nippon Sanso SR4000HT reactor at atmospheric pressure. *C*-plane sapphire with a micron-thick GaN template layer was used for the growth. The structure consists of 500 nm-thick *n*⁺-GaN for a bottom *n*-side ohmic contact, 200 nm *n*-GaN with a Si concentration of $2 \times 10^{16} \text{ cm}^{-3}$ and 90 nm *p*-GaN with an Mg concentration of $3 \times 10^{19} \text{ cm}^{-3}$. On top of the *p*-*n* junction, the TJs, comprised of two heavily *p*- and *n*-doped GaN layers with Mg and Si concentrations of $2 \times 10^{20} \text{ cm}^{-3}$ and $3 \times 10^{20} \text{ cm}^{-3}$, respectively, were grown. The growth temperature during the *p*⁺-GaN growth was 950 °C. The growth was ended with a 500 nm-thick *n*-GaN layer to ensure good current spreading and to recover any growth defects.

For the δ -dose study, a Si δ -dose layer was included between the *p*⁺ and *n*⁺ layer, referred to as the sample ‘Si- δ ’, whereas for the sample ‘Mg- δ ’, Mg δ -dose was introduced between the *p* and *p*⁺ layer. One sample with a TJ but without any δ -dose, referred to as ‘No- δ ’ was also grown for a comparison. Note that the ‘Si- δ ’ sample was used for the activation experiment where the annealing parameters, such as temperature and time, were optimized using the multiple pieces. To investigate the Mg buildup delay effect, four Mg- δ TJ samples with *p*⁺ GaN thicknesses of 6 nm, 9 nm, 12 nm and 18 nm were grown. Figure 1 schematically shows the layer structures of all the test samples used in this study.

After the materials growth, the samples were carefully examined under a standard optical microscope. Figure 2(a) shows the Nomarski image of the all-MOCVD-grown *p*-*n* diode samples with a TJ, where no pits or defects can be seen. The surface morphology and topography of the samples were examined using atomic force microscopy (AFM). Figure 2(b) shows the AFM image of the as-grown structures, exhibiting a peak-to-peak variation of only ~7 nm and a root-mean-square (RMS) roughness value of 0.8 nm for the scan area of 10 $\mu\text{m} \times 10 \mu\text{m}$. After the activation annealing, the RMS surface roughness is found to be approximately twice that of the as-grown sample, which is evidenced by the AFM data shown in figure S1 (available online at stacks.iop.org/JPD/54/155103/mmedia). For the samples, square mesas with 54 μm , 74 μm and 105 μm sides were defined by standard UV lithography and subsequent dry etching, down to the bottom *n*⁺-GaN layer in a BCl₃/Cl₂/Ar gas mixture. These three arbitrary sizes of the square mesas were used in this study to measure area-dependent electrical properties.

Prior to metal deposition, activation annealing was performed using a rapid thermal annealing system in the temperature range of 900 °C–970 °C. A pure N₂ gas environment was

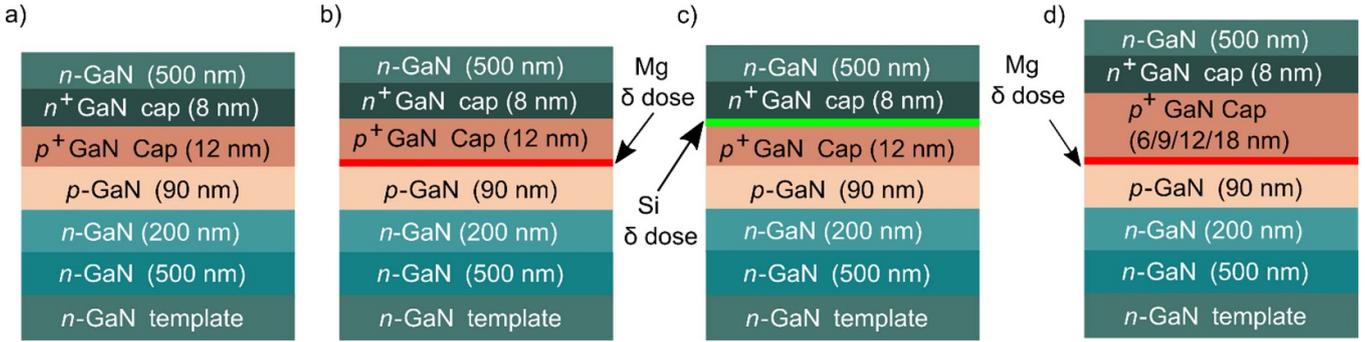


Figure 1. Schematic epitaxial layer structures of the samples with identical p - n diodes. Four samples including (a) TJ with no δ -dose (no- δ), (b) TJ with Mg δ -dose (Mg- δ), and (c) TJ with Si δ -dose (Si- δ), and (d) Mg- δ TJ with different p^+ GaN cap thickness were studied.

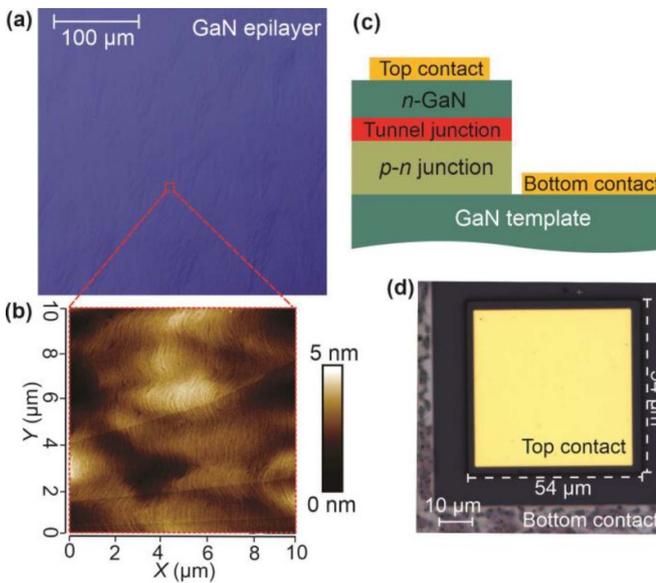


Figure 2. (a) Nomarski microscopy, and (b) $10 \times 10 \mu\text{m}^2$ AFM image of the as-grown sample. (c) Schematic cross-section, and (d) optical microscope image of the fully-processed square-shaped test diodes.

used during annealing since this environment is proven to be sufficient for good electrical and optical performance of LEDs [31]. The n -side ohmic contact was then formed by depositing Ti/Al/Ni/Au (20/120/30/50 nm) on n -GaN followed by annealing at 850 °C for 30 s. An optoelectronic device-compatible fabrication process was employed with an objective of efficient light collection from the backside of the devices. Considering Al to be more reflective than Ti, the p -side Al/Ni/Au top metal stack with thicknesses of 30/30/150 nm was used in order to achieve high reflectance [32]. After the top contact deposition, the p - n diode was annealed at 500 °C for 1 min in N_2 atmosphere.

3. Results and discussion

In order to understand the roles of three techniques on the improvement of the diode electrical properties through

reduced voltage penalties of TJ, it is important to determine the true voltage-drop of the TJ from the measured current–density–voltage characteristics. For that, we first calculated the voltage drop for the p - n junction using the ideal diode equation (1).

$$J = q \left[\frac{D_n n_p}{L_n} + \frac{D_p p_n}{L_p} \right] \left(e^{q(V - I r_s) / nkT} - 1 \right), \quad (1)$$

where J is the current density, D_n and D_p the diffusion coefficients, L_n and L_p diffusion lengths, n_p and p_n minority carrier density, V calculated voltage drop across diode without TJ, r_s series resistance at a particular current density and ideality factor of the p - n diode $\eta = 1$. The series resistance caused by only the sheet resistance at the doped epilayers and the top p -side n -contact resistance were included in equation (1). The resistance due to the large-area bottom n -side contact on the highly-doped n -template layer was negligible. The forward voltage penalty of the TJ can then be extracted by

$$\Delta V_{TJ} = V_1 - V, \quad (2)$$

where ΔV_{TJ} is the TJ voltage penalty and V_1 is measured forward voltage for the p - n diode with TJ samples at the same current density. Throughout the paper, the associated TJ voltage penalty at the two current density values, i.e. 20 A cm^{-2} and 100 A cm^{-2} as a device performance metric is calculated. The reason why 20 A cm^{-2} is chosen is peak EQEs for blue LEDs appears around that current density [28, 33].

3.1. Sidewall activation

A sidewall activation process is critical to achieving low and repeatable electrical properties across relatively large-area devices. For an effective thermal activation process, limited to lateral diffusion of H^+ in p -GaN layer, a long annealing time and high temperature are needed [3, 12]. To prevent the device performance degradation through interlayer diffusion, the activation temperature is usually kept below 750 °C by employing a long annealing time [12, 14]. However, the long annealing time is still sometimes insufficient for large-area devices [3, 13]. Our experimental study shows that the electrical properties of MOCVD-grown p - n devices can be drastically improved by an optimized activation annealing

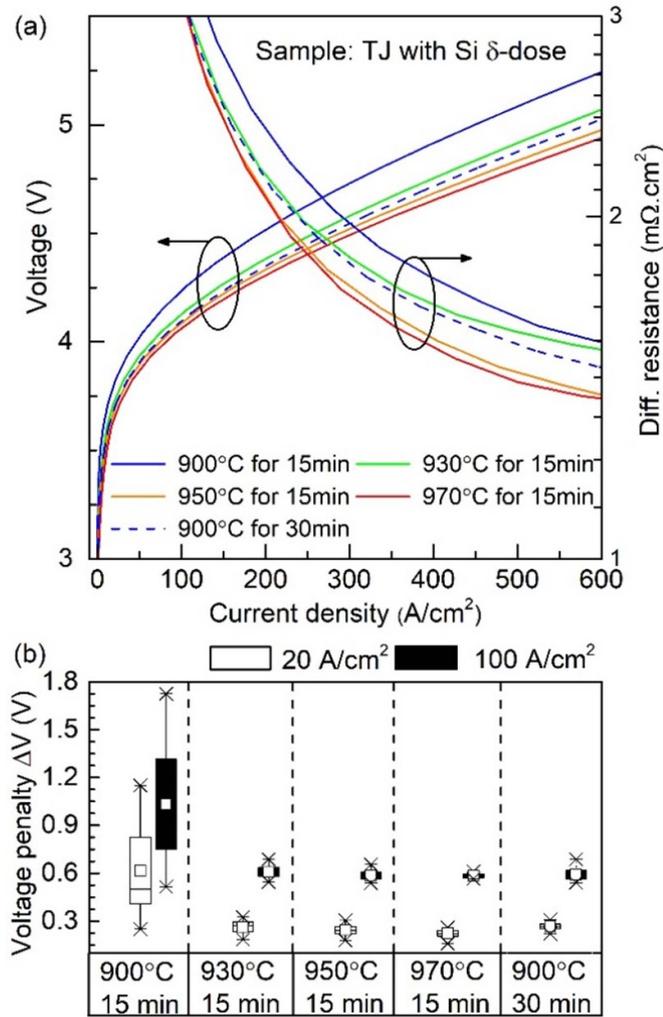


Figure 3. (a) Voltage- and differential resistivity vs current density characteristics, and (b) voltage penalty of the devices activated in different annealing conditions at the current densities of 20 A cm^{-2} and 100 A cm^{-2} .

process without sacrificing optical performance. Figure 3(a) shows the measured voltage and differential resistance versus current density characteristics of the $p-n$ junctions prepared at various activation parameters including annealing temperature and time. As can be seen, there is a decrease in voltage drop due to reduced series resistance as the temperature increases from $900 \text{ }^\circ\text{C}$ and/or the duration increases from 15 min. The voltage drop for each device was measured at 20 A cm^{-2} and 100 A cm^{-2} and plotted in figure 3(b). The voltage penalty variation across the devices is observed to be small except for the ‘ $900 \text{ }^\circ\text{C}-15 \text{ min}$ ’ samples, which shows 400 mV less voltage drop at 100 A cm^{-2} compared to the ‘ $900 \text{ }^\circ\text{C}-15 \text{ min}$ ’ sample. It is worth noting that no significant change in the reverse leakage current is observed, which indicates that the $p-n$ diodes remain unchanged in terms of the electrical properties, resulting in minimum or no device degradation.

The diffusion of H^+ has a square root relationship with the product of duration of the activation process and the diffusion coefficient, where the diffusion coefficient has an exponential dependence on temperature [14, 34]. As the n^+ -GaN layer acts

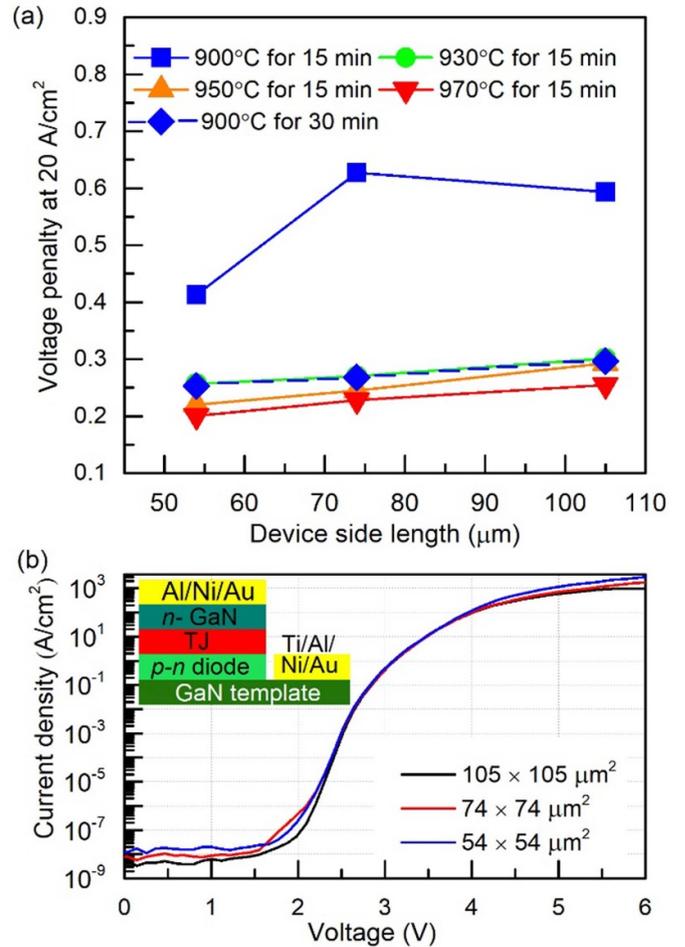


Figure 4. (a) Voltage drop at 20 A cm^{-2} as a function of side length activated at different annealing conditions, and (b) J–V characteristics activated at the optimized condition ‘ $900 \text{ }^\circ\text{C} 30 \text{ min}$ ’ for the square-shaped devices.

as a blocking layer, preventing H^+ from diffusing upward, the H^+ ion diffusion in p -GaN layers is confined to the lateral direction. Once the p -GaN layer is completely activated, the electrical characteristics are expected to be independent of the device size. Figure 4(a) shows the voltage penalty at 20 A cm^{-2} as a function of the side-length of square-shaped devices. The voltage drop is nearly independent of the device size as the annealing time and temperature reach an optimum value. In our study, ‘ $900 \text{ }^\circ\text{C}-30 \text{ min}$ ’ provides the device size independent electrical properties, which cannot be explained by the sole diffusion process. In fact, a deviation from the usual diffusion-driven process is observed when the smallest $54 \text{ } \mu\text{m}$ device shows full-activation like behavior, causing almost same voltage penalty as the largest $105 \text{ } \mu\text{m}$ device after annealing for 30 min at $900 \text{ }^\circ\text{C}$. Prior studies show that the activation of p -GaN is controlled by the surface-barrier effect and surface H^+ removal process in addition to lateral diffusion of H^+ [35–37].

The overall voltage drop is found to be the lowest for devices annealed at $970 \text{ }^\circ\text{C}-15 \text{ min}$. However, to keep the thermal budget as low as possible, the ‘ $900 \text{ }^\circ\text{C}-30 \text{ min}$ ’

annealing condition is a practical compromise, as only 50 mV of extra voltage penalty at 100 A cm^{-2} is recorded with respect to '970 °C–15 min'. For the '900 °C–30 min' sample, the J - V characteristics of different device sizes are plotted in figure 4(b), showing the excellent convergence of the curves. This suggests a uniform Mg doping distribution across all the devices from the optimized activation process. A slight deviation of current density among the devices at a voltage of $>4 \text{ V}$ could be attributed to the self-heating of the test devices.

3.2. Delta dose

The effects of δ -dose on TJs and the resulting electrical properties were investigated next. For that, our optimized activation process was employed to another set of samples with different δ -doses in the TJs. In addition to improving electrical conductivity, the δ -dose is expected to significantly impact an interface morphology. As a matter of fact, with an introduction of Mg and Si δ -dose on materials, a reduction in dislocation density by a factor of $\times 10$ and $\times 2$, respectively, was previously reported [38, 39]. This can be possibly understood through a growth interruption required during the δ -dose introduction, when dislocation density propagation can be partially terminated [39]. Moreover, the Mg δ -dose influences the reduction of the Mg impurity self-compensation and enhancement of free carrier concentration for GaN and AlGaIn [39].

Considering the aforementioned benefits, Mg- δ samples with two sheet charge densities of $2.2 \times 10^{13} \text{ cm}^{-2}$ and $4.5 \times 10^{13} \text{ cm}^{-2}$ (figure 1(b)) and a Si δ -dose sample with a sheet charge density of $3 \times 10^{13} \text{ cm}^{-2}$ (figure 1(c)) were grown, fabricated and tested. The sheet charge density for the Mg- δ samples was controlled by regulating the p -doping precursor flow in the system. To evaluate the diode performance, the voltage and differential resistivity against current density are plotted on a linear scale as shown in figure 5(a). With the incorporation of δ -dose in the devices, the voltage penalties as a performance metric are observed to decrease, and for a $4.5 \times 10^{13} \text{ cm}^{-2}$ Mg δ -dose sample, the voltage penalty is only 158 mV at 20 A cm^{-2} and 490 mV at 100 A cm^{-2} , as shown in figure 5(b).

The lowest differential resistivity among the TJ samples measured so far is $6.6 \text{ m}\Omega\text{-cm}^2$. This excellent result is achieved from the sample with an Mg- δ dose of $4.5 \times 10^{13} \text{ cm}^{-2}$, which is approximately half of the no- δ sample. Since all the p - n diodes underneath the TJs within the test devices have identical structures, the difference in the forward voltage drop is likely caused by the TJs. Both the theoretical and experimental studies show that implementing δ -dose at the interface improves the TJ efficiency by creating a thin, highly-doped layer which reduces the tunneling distance [10, 40]. The voltage penalty is reduced to 490 mV from 660 mV at 100 A cm^{-2} as the Mg δ -dose with a concentration of $4.5 \times 10^{13} \text{ cm}^{-2}$ was introduced into the TJ. It should also be noted that the influence of Mg δ -dose on the TJ efficiency is higher compared to the Si δ -dose, as can be evidenced by the measured voltage penalties. Compare to the Si δ -dose sample, the Mg- δ shows less penalty at low current densities even for the relatively low doping concentration. The

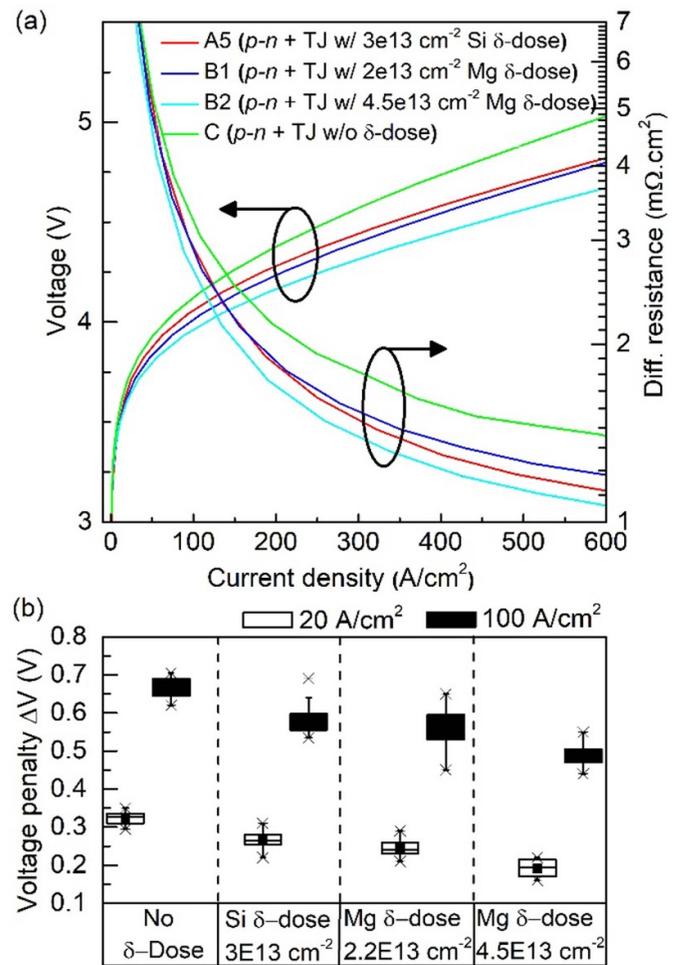


Figure 5. (a) J - V and differential resistivity- V characteristics, and (b) voltage penalty of samples no- δ , Si- δ , Mg- δ dose at 20 A cm^{-2} and 100 A cm^{-2} .

measured differential resistivity is $3 \text{ m}\Omega \text{ cm}^2$ at 100 A cm^{-2} . As the tunneling efficiency improves at high current density for a TJ, an increase in the input current density reduces the TJ resistance, and consequently, the overall resistance. Since no voltage penalty saturation is observed for the Mg δ -dose, it opens a possibility of further reduction in voltage penalty with a higher dose and this will be investigated in future studies. It should be noted that a very high dose of Mg possibly could lead to surface damages, inversion effect and subsequently, Mg depletion [41, 42].

Note that the secondary ion mass spectrometry data of the Mg profiles for our control samples with- and without δ -dose is presented in figure S3.

3.3. Mg buildup delay

While growing p -GaIn structures with MOCVD, the Mg buildup delay [16, 43] from the time Mg shutter is turned on, until the time required to reach the desired peak concentration has significant importance, especially while growing very thin layers required for TJs. To ensure maximum Mg incorporation in the highly p -doped layer, a series of samples of

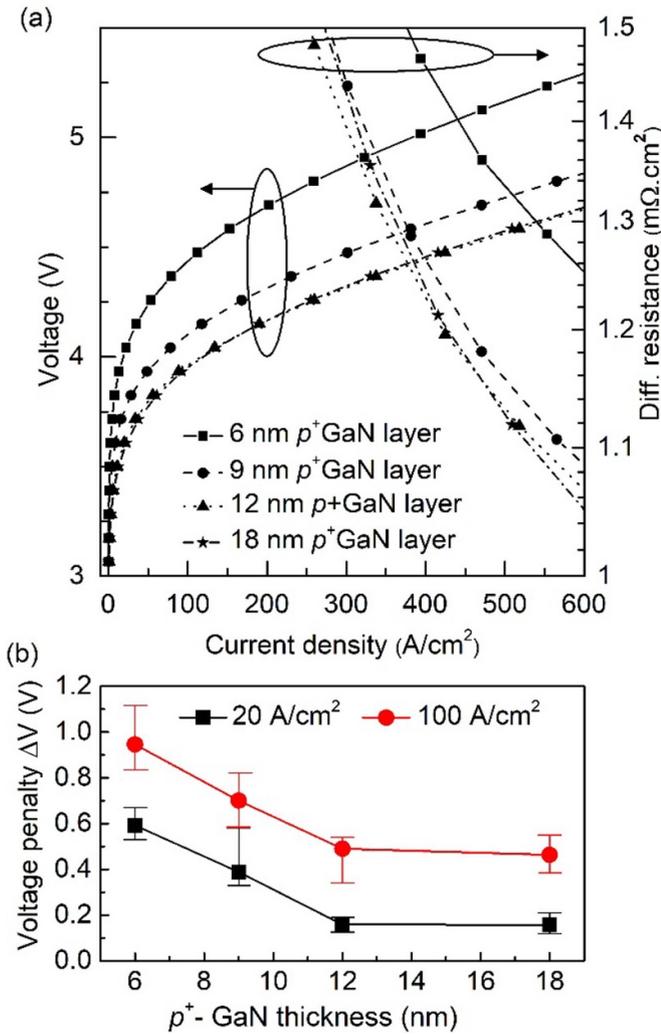


Figure 6. (a) Voltage- and differential resistivity against current density for the samples with different p^+ layer thicknesses, and (b) voltage penalty as a function of thickness of p^+ -GaN at 20 A cm^{-2} and 100 A cm^{-2} .

different p^+ -GaN layer thicknesses was tested. Interestingly, the diodes with a higher p^+ -GaN thickness exhibits a lower voltage drop, as shown in figure 6(a). Measuring the doping concentration or inspecting the surface morphology of the buried p -layers is challenging since all the samples under study were grown in a single-continuous growth. For the constant Mg δ -dose $4.5 \times 10^{13} \text{ cm}^{-2}$ and doping concentration of the p^+ layer of the TJs, it is believed that with an increase of the p^+ layer thickness, p -type conductivity improves and becomes maximum at a thickness of 12 nm. This suggests that 12 nm-thick p^+ -GaN layer results in highest tunneling efficiency due to the maximum achievable hole concentration. Hence, this thickness can be considered as a critical thickness for which all band bending is expected to occur at the p^+ -GaN layer [44]. As can be seen in figure 6(b), further increase of the p -GaN thickness does not improve the electrical properties as the inherent tunneling distance supersedes the advantages of thicker heavily Mg-doped p^+ -GaN layers. Hence, growing the p^+ -GaN layer up to a certain thickness helps compensate the Mg

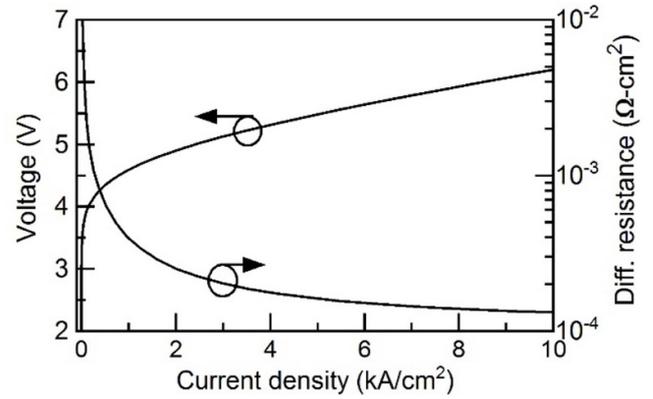


Figure 7. Voltage- and differential resistivity versus current density for the Mg- δ dose ($4.5 \times 10^{13} \text{ cm}^{-2}$) sample up to a current density of 10 kA cm^{-2} .

buildup delay effect, resulting an ultralow-resistance TJ. For clarity, the Mg buildup delay process is schematically shown in figure S2.

To evaluate the TJ performance at a higher current density than reported earlier and to confirm its suitability beyond optoelectronic and low-power electronic devices, devices of the Mg δ -dose sample (figure 1(b)) were tested again. Figure 7 shows the current density- and differential resistivity against voltage characteristics. The devices show a record-low differential resistance of $1.6 \times 10^{-4} \text{ } \Omega \text{ cm}^2$ at 5 kA cm^{-2} which is the lowest value ever reported [23] for all-MOCVD grown GaN TJ devices. After the device turns on, the differential resistance drops until 5 kA cm^{-2} and stays nearly constant in the current range from 5 kA cm^{-2} to 10 kA cm^{-2} .

4. Conclusion

In conclusion, low resistivity TJs and reduced voltage penalties are obtained in all-MOCVD grown p - n diodes with a buried TJ. This was achieved by optimizing the activation annealing time and temperature for buried p -GaN layers. Additional improvement is also observed by implementing δ -dose for both donor and acceptor dopants within the TJs. Annealing at this high temperature is explored for the first time to our knowledge to achieve a uniform p -GaN condition that possibly opens a path for large-area all-MOCVD grown TJ integrated devices in the future. It is expected that combining both the Si and Mg δ -dose in an actual LED structure and activating the Mg-doped layer will result in further improvement in electrical performance, benefitting next-generation of electronic and optoelectronic devices.

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