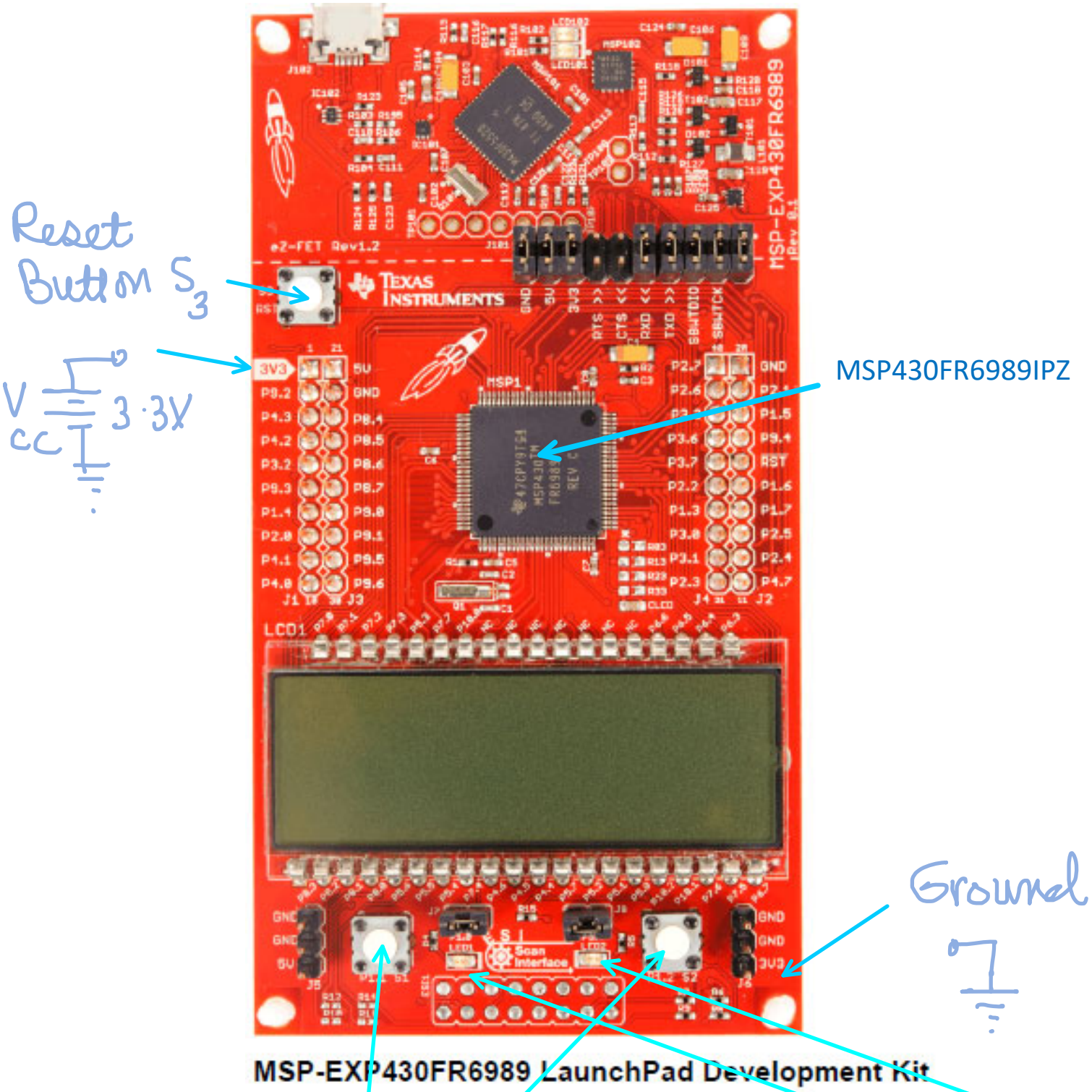

Reset Button S3
V
CC
3.3V
MSP430FR6989IPZ
Ground
MSP-EXP430FR6989 LaunchPad Development Kit
Pushbuttons S1 & S2
LEDs Red & Green

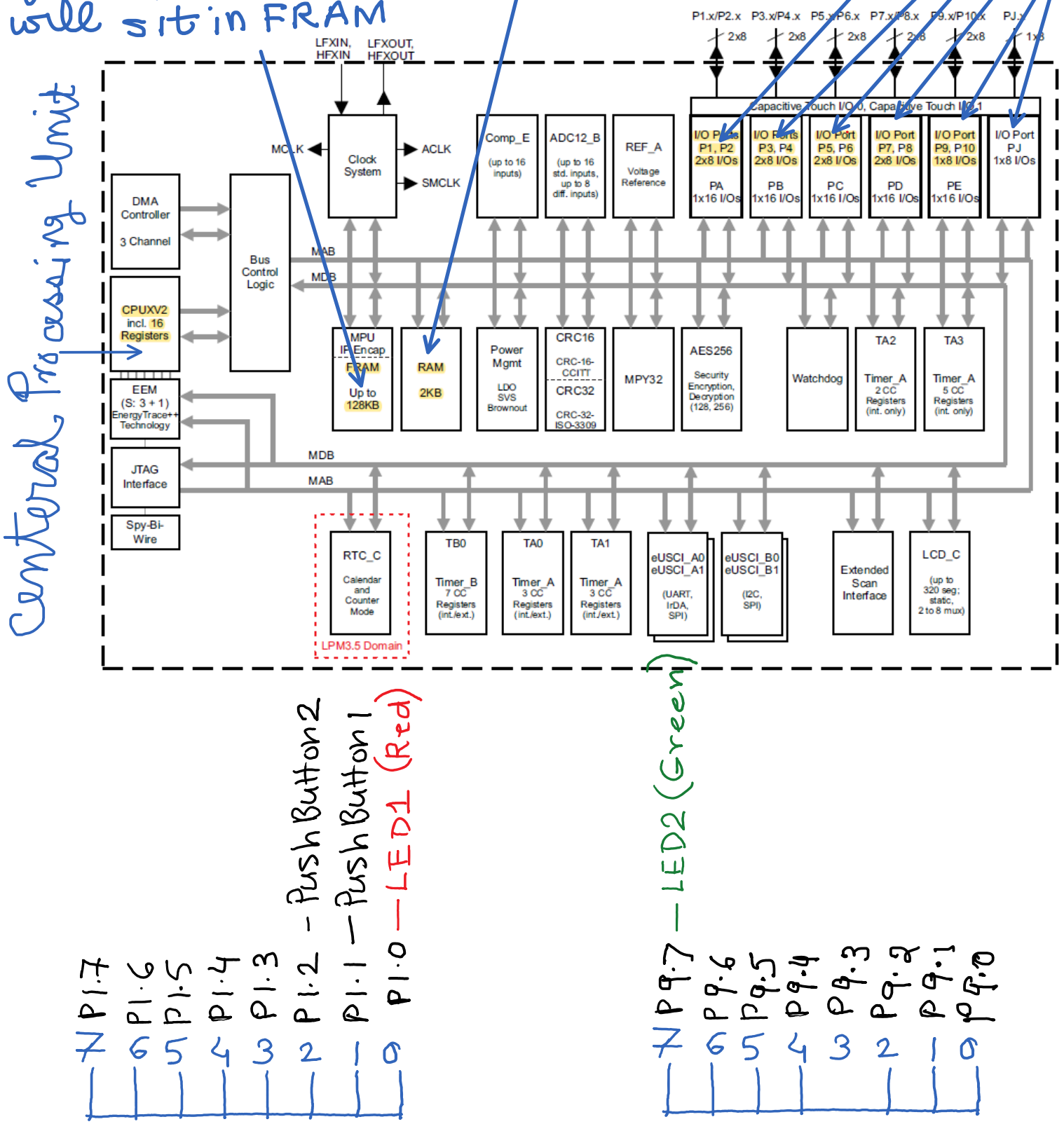
ECE2560 Lesson03 Page_2

From Device User Guide
SLAS789D

Variables and Stack will be in RAM

Ports for Digital GPIO (General Purpose Input Output)

Your program will sit in FRAM

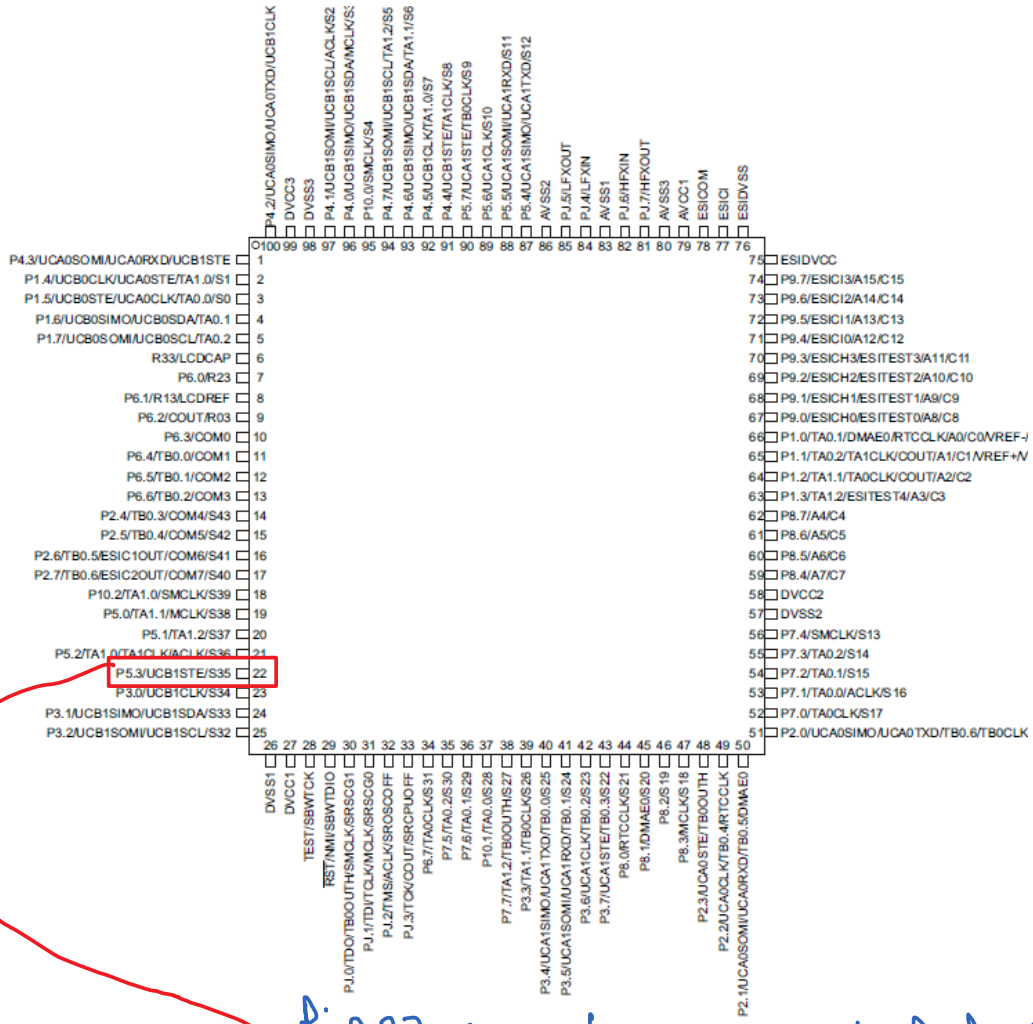



P1.0 — LED1 (Red)
P1.1 — Push Button 1
P1.2 — Push Button 2
P9.7 — LED2 (Green)

P1.7 P1.6 P1.5 P1.4 P1.3 P1.2 P1.1 P1.0
7 6 5 4 3 2 1 0

P9.7 P9.6 P9.5 P9.4 P9.3 P9.2 P9.1 P9.0
7 6 5 4 3 2 1 0

| PART NUMBER | PACKAGE | BODY SIZE(2) |
|---|---|---|
| MSP430FR6989IPZ | LQFP (100) | 14 mm × 14 mm |
| MSP430FR6989IPN | LQFP (80) | 12 mm × 12 mm |
| MSP430FR5989IPM | LQFP (64) | 10 mm × 10 mm |
| MSP430FR5989IRGC | VQFN (64) | 9 mm × 9 mm |

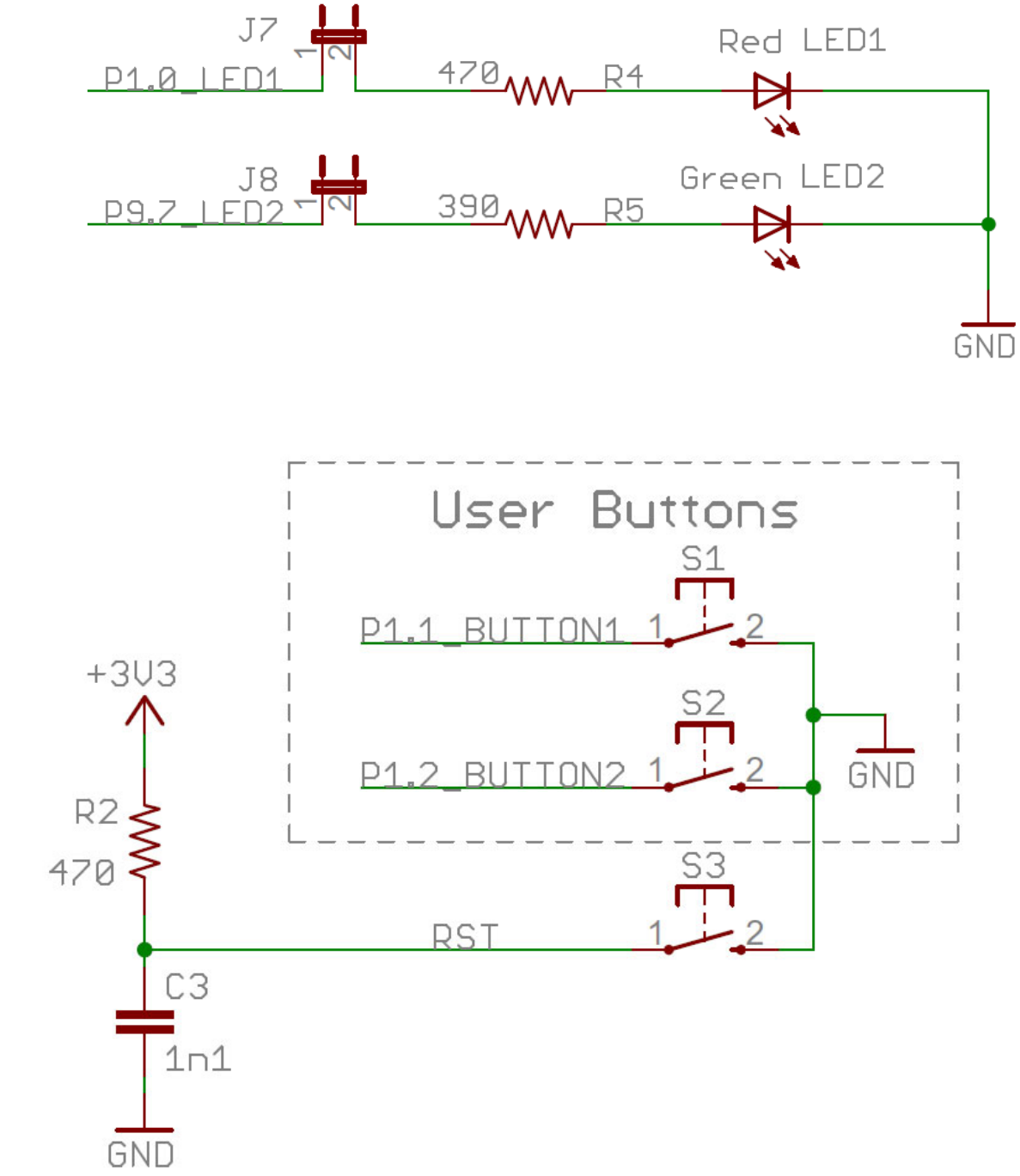



Pin22 can be connected to 3 peripherals

| | | | | | |
|---|---|---|---|---|---|
| P5.3/UCB1STE/Sx | 22 | S35 | | | General-purpose digital I/O<br>USCI_B1: Slave transmit enable (SPI mode)<br>LCD segment output (segment number is package specific) |

From the MSP430FR6989 LaunchPad™ Development Kit USER GUIDE
SLAU627A

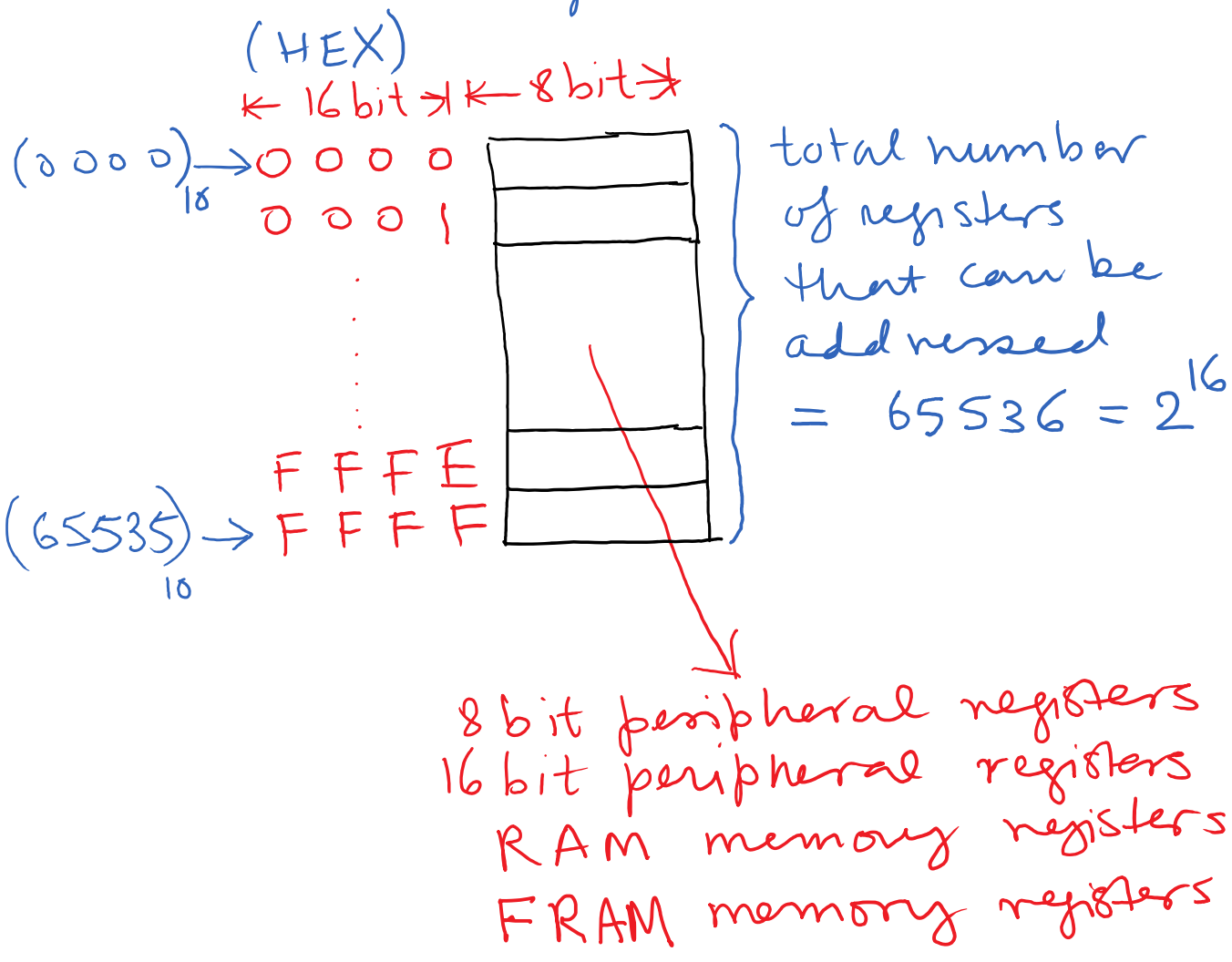
From the Schematic of the Launchpad



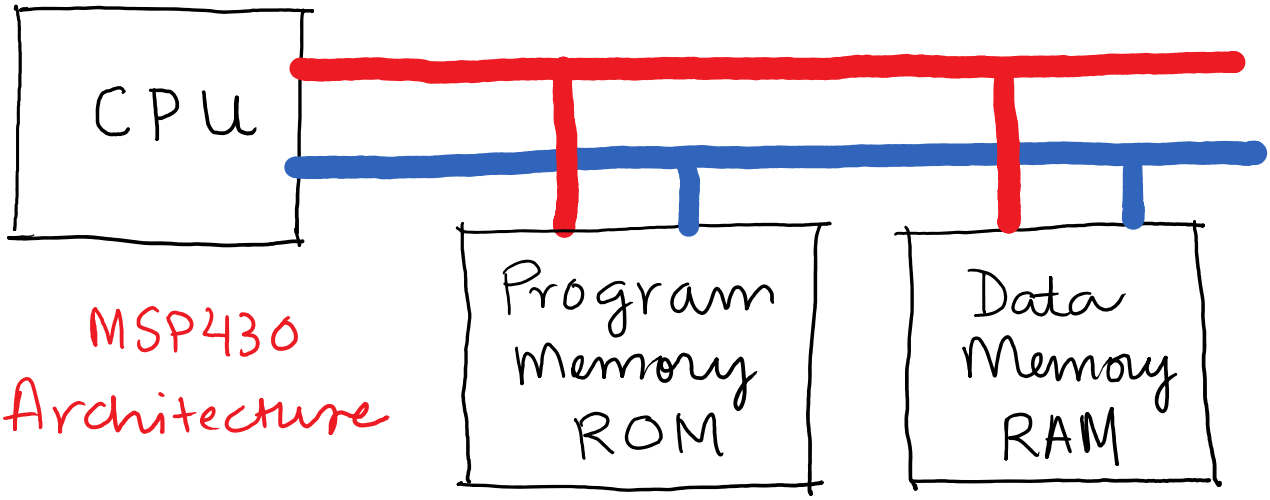
# Memory Mapped

Every peripheral register is mapped to an address, including the memory registers of FRAM and RAM

Address Bus → 16 bit wide



# von Neumann Architecture (Princeton Architecture)

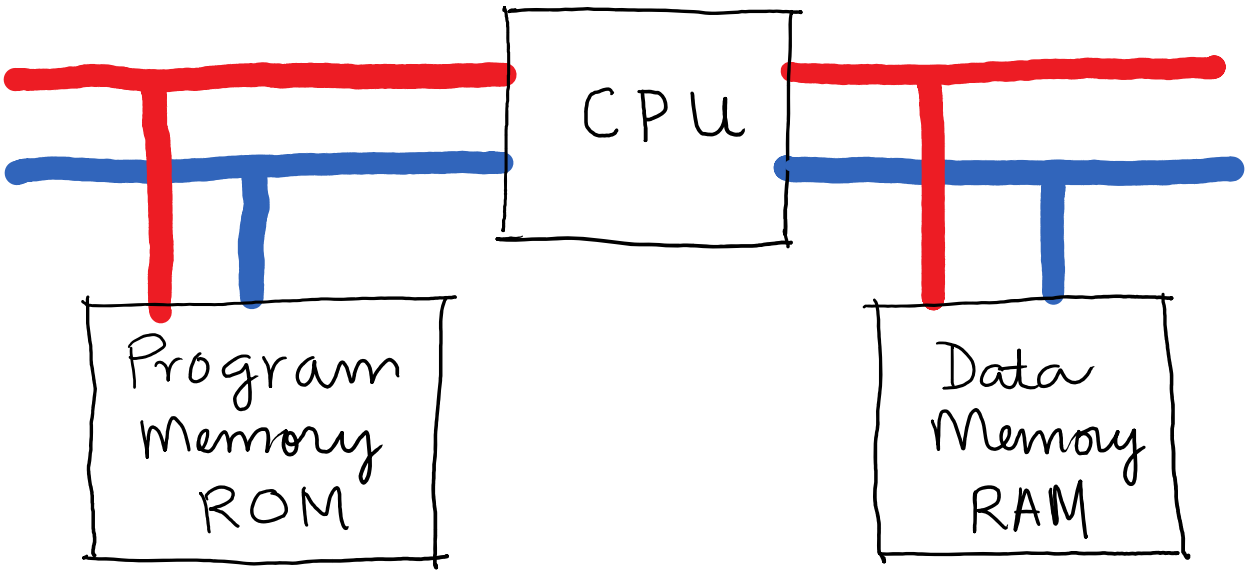



MSP430 Architecture

one set of addresses for ROM and RAM + other peripheral registers

ROM → FRAM

# Harvard Architecture




Seperate set of addresses for ROM

Seperate set of addresses for RAM

# Harvard Architecture

Efficient:
Simultaneous access to the program and data memories

Complex:
constants (in ROM) and variables (in RAM) live in different address spaces and must be treated differently

# von Neumann Architecture
(Princeton Architecture)

Not as efficient as Harvard Architecture

Simpler:
Constants (in RAM) and variables (in RAM) live in the same address space and are treated similarly