ANANT AGARWAL
IEEE FELLOW

Agarwal.334@osu.edu
Cell: 919-360-8215

Experience

August 2017 – Present: **Professor, Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio.**

Responsibilities include:
- Teaching Graduate courses on semiconductor power devices, design, fabrication and characterization. https://cusp.umn.edu/power-electronics/wide-band-gap-wbg-devices
- Research on Wide Band Gap and Ultra-Wide Band Gap power devices. The main focus is design of SiC power devices for ruggedness and reliability. Students are being educated to understand device physics, device simulation, layouts for industrial grade devices and detailed evaluation of reliability and ruggedness. The theme of research is that the commercial devices available in the market are lacking in certain aspects of reliability and therefore they are not ready for the automotive market. We focus on the design approaches to overcome the reliability issues.
- Supporting Power Electronics research at the Center for High Performance Power Electronics (CHHPE)

March 2013 – November 2016: **Advanced Manufacturing Office**, **U.S. Department of Energy, Washington DC**
Technical Advisor for the Wide Bandgap (WBG) Initiative

Responsibilities included:
- Governmental oversight and technical day-to-day management of the first Next Generation Power Electronics Institute, *PowerAmerica*, located at North Carolina State University ($140M total funding, $70 M from DOE). Duties focussed on activities relating to promoting commercial production and adoption of wide bandgap SiC/GaN power devices in power electronics, mentoring young scientists/engineers to create a work force versed in WBG processing and applications, and fostering collaborative activities with industry, universities and Government research laboratories to benefit the U.S. energy infrastructure.

- Creation and oversight of two programs on Next Generation Electric Machines (NGEM) (totaling approximately $50M) to develop both an Integrated System of SiC based Medium Voltage Variable Speed Drives for high RPM (15,000), 1 MW direct drive electric motors and associated enabling technologies such as manufacturing of High Temperature Superconductors (HTS), better bearings, high voltage insulation, >3% Si Steel and other soft magnetic materials.

- Establishment and management of graduate Traineeship programs ($6M funding) at two universities to educate U.S. Graduate students in the design and building of SiC and GaN based power electronics.

- Development of rationale for new topics such as the applications of high voltage(>10 kV) devices in Medium Voltage AC/AC Converters connected between the 13.8 kV Distribution Macrogrid and 13.8 kV asynchronous microgrid to facilitate >50% Renewables on the grid; and development of GaN substrates for low leakage lateral GaN RF and power devices.

March 2008 – March 2013: **North Carolina State University**
Adjunct Professor (unpaid), **ECE Department**

Responsibilities included:
- Mentoring of Graduate students in the area of wide band gap power electronics and being a member of their advisory committee.
- Shared teaching of the Graduate level Semiconductor Device course for 1 semester.
- Helped a number of faculty members with the proposals and teaming arrangements.
- Helped the scientists at Cree to collaborate with NCSU faculty on technical problems of mutual interest.

March 1999 – March 2013: **Cree Inc., Durham, NC**
Technical R&D Manager

Responsibilities included:

- Directing a group of approximately 15 engineers and scientists engaged in short and long term fundamental and applied research on SiC power devices including Schottky diodes, PiN rectifiers, power BJTs, MOSFETs, thyristors, IGBTs and JFETs. Responsibilities included resolving research/development issues involving 2D device simulation, device design and modeling, process development and integration, manufacturing/yield/cost analysis, and issues relating to static/dynamic testing and reliability of SiC power devices. Some specific problems include inversion layer electron mobility in SiC MOS devices, charge sensitivity to electric fields in edge terminations of high voltage power devices to achieve a 17 kV IGBT, optimization of edge terminations in mesa devices to realize 17 kV thyristors and GTOs, reliability of gate oxides under positive and negative gate bias, reduction of point defects to achieve higher minority carrier lifetimes in bipolar devices, reduction of stacking fault formation in bipolar devices due to basal plane dislocations, achieving a current gain in excess of 70 in Bipolar Junction Transistors (BJT), and utilizing the appropriate passivation to protect devices against mobile ions and humidity. Additionally, R&D efforts resulted in the demonstration of the feasibility of RF SiC BJTs for pulsed power amplification in the UHF band by successfully implementing the design, fabrication and testing of SiC RF BJTs up to 2.1 kW in a single package at 400 MHz.

- Managing and directing a large team of scientists and engineers to successfully develop/launch several generations of commercial products. These included 600 V, 1200 V and 1700 V SiC Schottky diodes and MOSFETs; generating sales revenue in excess of $150 M/year in 2016 (*I left Cree in 2013*) with a potential for reaching $500 M/year by 2020 (*already reached*). Duties involved continuously addressing a number of broad ranging issues involving a mix of technical problems (both fundamental and applied), manufacturing yield/cost concerns, patent filings, project management of budgets, processing and delivery times, as well as handling personnel issues.

- Developing technical proposals resulting in approximately $100 M+ of research funding from DoD (DARPA, ONR, ARL, and AFRL), DOE (ARPA-E) and private companies to insure the continuation of research and long-term viability of the company. These activities have resulted in the establishment of a network of contacts and trusted relationships with various government agencies, including the Army Research Laboratory, Air Force Research Laboratory, Office of Naval Research, DARPA and ARPA-E.

- Establishing long term collaborative relationships with universities and National Laboratories to address far ranging research problems, critical to product development. These have included Purdue, RPI, NCSU, Auburn, University of South Carolina and Vanderbilt University as well as NRL, ARL, AFRL, Oak Ridge National Laboratory and Sandia Laboratory. Efforts in this area also involved becoming actively engaged in student educational activities, guiding students at NCSU, establishing summer internship programs, serving on PhD committees and mentoring young scientists and engineers in the identification of issues and understanding device physics as well as encouraging and assisting them with effective presentations and publishing research papers.

July 1990 –March 1999: **Northrop Grumman Science & Technology Center, Pittsburgh (formerly Westinghouse)**
Fellow Engineer

Responsibilities included:

- Managing a group of 5 engineers and scientists working on SiC power switching devices and X-band Si/SiGe MMIC development. Projects and accomplishments included research on:
  1. Silicon RF technology based on fully depleted, 0.35 μm SOI CMOS on high resistivity substrates developed for X-band mixed mode RF circuits. The process employed self-aligned Ti silicide and metal re-enforced submicron polysilicon gates. N-channel devices showed f_T = 20 GHz, f_{MAX} = 42 GHz and a Noise Figure of 1.95 dB at 10 GHz. Spiral inductors and Capacitors with high Q were also demonstrated. Circuits including a low noise amplifier and 4 bit digital attenuator were also demonstrated.

  2. Microwave high power SiC Static Induction Transistors (SIT) for L and S band transmitter applications. This specialized technology involved Schottky barrier gates and exploited the high electric breakdown field and high saturated electron velocity of SiC. As part of this effort the first ion implanted SiC SIT with 400 V breakdown voltage was demonstrated. These devices have generated up to 1 kW at 800 MHz and 300 W at 3 GHz and exhibit a great potential for cost reduction of Radar transmitters through part count reduction and higher power-added efficiency as compared to the SiGe based BJTs.

  3. High power SiC switching devices such as UMOSFETs (also known as Trench MOSFETs), LDMOSFETs, Gate Turn-Off Thyristors, Hybrid MOS Turn-Off Thyristors, Schottky diodes, PiN diodes and JFETs. These devices were targeted for use in high power, high efficiency, high temperature power electronics in the More Electric Aircraft, power conversion in utilities, traction systems in combat hybrid-electric vehicles, pulsed

power weapons and industrial heavy motor drives. It is anticipated that 10-25 kV SiC GTOs and Thyristors will lead to significant cost, weight, and volume reduction of utility power conversion equipment.

4. SiGe HBTs for X-band Radar Transmitter. This technology was based on a 0.8-micron polysilicon emitter and self-aligned 10 ohms/square platinum silicide process. The devices were capable of producing more than 500 mW/mm of emitter periphery at 8 GHz but the gain and power added efficiency were relatively low. It was shown by modeling that these devices suffered from base/emitter de-biasing effect at large currents due to the emitter resistance. It was solved by the metal strapping of emitter fingers and the technology became a viable low-cost alternative for expensive GaAs HBTs and MESFETs in the 8-12 GHz frequency range.

July 1985 - June 1990: **M.N.R. Engineering College, Allahabad, India**
Assistant Professor

- Taught classes in Electrical Engineering including: Digital System Design, SPICE Simulation Laboratory, Electronic Devices, Computer Aided Network Design, Microprocessors
- Supervised Masters' theses
- Developed a Semiconductor Device Characterization Laboratory.
- Mentored undergraduate students to pursue Graduate studies in India and abroad.

July 84 - June 85: **AT&T Bell Laboratories, Murray Hill, New Jersey**
Technical Staff

- Designed GaAs digital and analog Integrated Circuits based on enhancement/depletion (ED) mode GaAs HEMT technology for applications in mobile telephone and light-wave communications. All the circuits performed as expected the very first time. A number of these circuits were utilized in the underwater communications at 1.5 Gbit/s – a dream in 1985.

Education
Ph.D. Electrical Engineering, Lehigh University, June 1984
Thesis: "A Study of Traps in Metal-Insulator-Semiconductor (MIS) System with the Three Terminal Gated-Diode Structure", Supervisor: Prof. Marvin White, GPA 3.8/4.0.

M.S. Electrical Engineering, **University of Tennessee Space Institute**, Tullahoma, TN, March 1980, GPA 3.96/4.0

B.S. Electrical Engineering, M. N. R. Engg. College, University of Allahabad, India, June 1978, graduated with highest honors

Honors, Awards, and Organizations

- Member of IEEE Electron Device Society (1980) and IEEE Fellow in Electron Device Society since January 2012
- Technical Program Co-chair of the International Conference on Silicon Carbide and Related Materials 20011 (ICSCRM 2011), Cleveland, Ohio.
- Technical Program Committee Member of the IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2005 – 2006
- Technical Program Committee Member of the International Conference on Silicon Carbide and Related Materials, 2004-2005.
- Technical Program Committee Member of the Device Research Conference, 2000-2001
- Symposium Organizer, Silicon Carbide – Materials, Processing, and Devices, MRS, Boston, Fall 2000
- Guest Editor, Special Issue on SiC – IEEE Electron Device Transactions, March 1999
- George Westinghouse Signature Award for work on UHF SiC Static Induction Transistor, Feb. 1996
- Chaired Technical Session IV B on Wide Bandgap and Power Devices, 53rd Annual Device Research Conference, University of Virginia, Charlottesville, Virginia, June 19-21, 1995
- Corporate George Westinghouse Innovation Award for a disclosure on SiC Static Induction Transistor, May 1995
- Co-Chaired Technical Session on SiC Devices, at WOCSEMAD, New Orleans, Feb. 1995
- Westinghouse EISD Outstanding Performance Recognition for formulation of a viable approach to SiC NVRAM, August 1992
- Sherman Fairchild Fellowship, Lehigh University, 1981-84

Publications, Presentations, Book Chapters and Patents

- Over (300) co-authored publications and presentations at conferences including invited talks, (7) co-authored book chapters, (1) co-edited book, (1) video lecture series of 28 lectures and over (60) issued patents.
- Reviewer for IEEE Electron Device Letters, Applied Physics Letters, Journal of Applied Physics and Solid-State Electronics.
- Details shown on accompanying pages.

Invited Talks

1. **A. K. Agarwal**, R. C. Clarke, R. R. Siergiej, C. D. Brandt, A. A. Burk, A. Morse, P. Orphanos, "30 W VHF 6H-SiC Power Static Induction Transistors," presented at **WOCSEMAD**, New Orleans, Feb. 1995.
2. **A. K. Agarwal**, Thomas J. Smith, Maurice H. Hanes, Rowan L. Messham, Michael C. Driver and Harvey C. Nathanson, "MICROX^{TM} - An Affordable Silicon MMIC Technology," invited talk at the Workshop - **Silicon RF Technologies, 1995 IEEE MTT-S International Microwave Symposium**, Orlando, Florida, May 1995.
3. **A. K. Agarwal**, "SiC Electronics," invited talk presented at the Emerging Technologies Session, **IEDM** 1996
4. **A. K. Agarwal,** J. B. Casady, L. B. Rowland, S. Seshadri, R. R. Siergiej, and C. D. Brandt, "Silicon Carbide Power Device Development," **Second International All Electric Combat Vehicle (AECV) Conference**, Dearborn, Michigan, June 1997.
5. **A. K. Agarwal,** "Status of SiC Power Devices at Northrop Grumman," **9th European Conference on Diamond, Diamond like Materials, Nitrides and Silicon Carbide (Diamond 98)**, Crete, Greece, 13-18 September, 1998.
6. **Anant Agarwal**, Adrian Powell, Joe Sumakeris, Sei-Hyung Ryu, Craig Capell, Lori Lipkin, Mrinal Das, Ranbir Singh, Calvin Carter and John Palmour, "Recent Developments in SiC Materials and Power Devices at Cree – A Progress Report," presented at **Government Microcircuit Applications and Critical technology Conference, GOMACTech 03**, April 03, 2003, Tampa, Florida.
7. **Anant Agarwal**, "High Temperature Operation of SiC Power Devices," **Workshop on Extreme Environments Technologies for Space Exploration**, Jet Propulsion Laboratory, Pasedena, California, May 15, 2003.
8. **Anant Agarwal**, Jim Richmond, Sei-Hyung Ryu, Mrinal Das, Sumi Krishnaswami and John Palmour, "Latest Advances in SiC Device Technology and Practical Applications," presented **at Government Microcircuit Applications and Critical Technology Conference, GOMACTech 04**, March 17, 2004, Monterey, California.
9. **Anant Agarwal**, Mrinal Das, Sumithra Krishnaswami, John Palmour, James Richmond, and Sei-Hyung Ryu, "SiC Power Devices - An Overview," **Mat. Res. Soc. Symp. Proc.** Vol. 815, pp. 243-254, (2004) Materials research Society Symposium, San Francisco, California, U. S. A., April 14-15, 2004.
10. **A. K. Agarwal** and Charles Scozzie, "Progress in SiC Materials and Devices," presented at the **1st Annual Ground -Automotive Power & Energy Symposium**, July 20-22, 2005, Hilton, Detroit/Troy.
11. **A. Agarwal**, A. Burk, R. Callanan, C. Capell, M. Das, S. Haney, B. Hull, M. O'Loughlin, M. O'Neil, J. Palmour, A. Powell, J. Richmond, S.-H. Ryu, J. Sumakeris, and J. Zhang, "Critical Technical Issues in High Voltage SiC Power Devices," **Materials Science Forum Vols. 600-603** (2009), pp. 895-900, ICSCRM 2007.
12. **A. Agarwal**, "Technical challenges in commercial SiC power MOSFETs," **Semiconductor Device Research Symposium, 2007 International**; College Park, MD, USA, Dec. 12-14, 2007. Digital Object Identifier: 10.1109/ISDRS.2007.4422481.
13. **Anant Agarwal**, "Recent Advances in SiC Power Switching Devices," presented at the **2008 Lester Eastman Conference on High Performance Devices**, University of Delaware, NJ, Aug. 5-8, 2008.
14. **A. Agarwal**, Q. Zhang, M. Das, S. Ryu, L. Cheng, M. O'Loughlin, A. Burk, and J. Palmour, "An Update on High Voltage SiC Power Devices," **Invited**, The Electrochemical Society (ECS) Trans. Vol. 41, Issue 8, pp. 39-41, 2011. DOI 10.1149/1.3631484.
15. **A. Agarwal**, W. J. Sung, L. Marlino, P. Gradzki, J. Muth, R. Ivester, N. Justice, "Wide Band Gap Semiconductor Technology for Energy Efficiency", Plenary talk at **ICSCRM 2015**, Catania, Italy, **Materials Science Forum**, Vol. 858, pp. 797-802, 2016
16. **Anant Agarwal**, Laura Marlino, Robert Ivester, Mark Johnson, "Wide BandGap Power Devices; The U.S. Initiative", to be presented at the **EEDERC 2016**, Lausanne, Switzerland, September 12-15, 2016.
17. Strategies for Commercialization and Market Insertion - Moving from Silicon to SiC: Learning to Think Differently, **Anant Agarwal,** presented at the International Conference on Silicon Carbide and Related Materials (**ICSCRM 2017**), Washington DC, September 17, 2017.

Patents

1. **Anant K. Agarwal**, Richard R. Siergiej, Charles D. Brandt and Marvin H. White, “A non-volatile random access memory Cell Constructed of Silicon Carbide,” U.S. Patent No. 5,510,630, April 23, 1996.
2. **Anant K. Agarwal**, Rowan L. Messham and Michael C. Driver, “Aluminum Gallium Nitride based Heterojunction Bipolar Transistor,” U.S. Patent No. 5,641,975, June 24, 1997.
3. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, Charles D. Brandt, “Static Induction Transistors,” U.S. Patent No. 5,705,830, June 6, 1998.
4. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, abd Charles D. Brandt, "Silicon Carbide Static Induction Transistor Structure," U.S. Patent No. 5,903,020, May 11, 1999.
5. **Anant K. Agarwal**, Rowan L. Messham and Michael C. Driver, "Aluminum Gallium Nitride Heterojunction Bipolar Transistors," U. S. Patent No. 5,923,058, July 13, 1999.
6. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, abd Charles D. Brandt, "Static Induction Transistor," U.S. Patent No. 5,945,701, Aug. 31, 1999.
7. R. Singh, **A. K. Agarwal**, and S. Ryu, **“**Method of fabricating a self-aligned bipolar junction transistor in silicon carbide and resulting devices,” U.S. Patent #6,218,254, April 17, 2001.
8. R. Singh, **A. K. Agarwal**, and S. Ryu, **“**Self-aligned bipolar junction silicon carbide transistors,” U.S. Patent #6,329,675, Dec. 11, 2001.
9. S. Ryu, J.J. Sumakeris, **A. K. Agarwal**, and R. Singh **“**Methods of fabricating silicon carbide inversion channel devices without the need to utilize P-type implantation,” U.S. Patent #6,429,041, Aug. 6, 2002.
10. S. Ryu, **A. K. Agarwal**, C. Capell, and J. W. Palmour, **“**Large area silicon carbide devices and manufacturing methods therefor,” U.S. Patent #6,514,779, Feb. 4, 2003.
11. S. Ryu, J.J. Sumakeris, **A. K. Agarwal**, and R. Singh, **“**Silicon carbide inversion channel mosfets,” U.S. Patent #6,653,659, Nov. 25, 2003.
12. **A. K. Agarwal,** S. Ryu, and J. W. Palmour, **“**Large area silicon carbide devices,” U.S. Patent #6,770,911, Aug. 3, 2004.
13. Sei-Hyung Ryu, **Anant Agarwal**, Mrinal Kanti Das, Lori A. Lipkin, John W. Palmour, Ranbir Singh, "Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors having a shorting channel and methods of fabricating Silicon Carbide Field Effect Transistors having a shorting channel," U. S. Patent #6,956,238, October 18, 2005.
14. Sei-Hyung Ryu and **Anant K. Agarwal**, "Multiple Floating Guard Ring Edge Termination for Silicon Carbide Devices," U. S. Patent #7,026,650, April 11, 2006.
15. **Agarwal; Anant**, Ryu; Sei-Hyung, Palmour; John W., “Manufacturing methods for large area silicon carbide devices,” U. S. Patent #7,135,359, Nov. 14, 2006.
16. **Agarwal; Anant K**., Krishnaswami; Sumithra, Ryu; Sei-Hyung, Hurt; Edward Harold, “Silicon carbide bipolar junction transistors having epitaxial base regions and multilayer emitters and methods of fabricating the same,” U. S. Patent #7,304,334, Dec. 4, 2007.
17. **Agarwal; Anant K**., Krishnaswami; Sumithra, Ryu; Sei-Hyung, Capell; D. Craig, “Silicon carbide bipolar junction transistors having a silicon carbide passivation layer on the base region thereof,” U. S. Patent #7,345,310, March 18, 2008.
18. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., Hobgood; Hudson McDonald, **Agarwal; Anant K.**, Palmour; John W., “High voltage silicon carbide devices having bi-directional blocking capabilities,” U. S. Patent #7,391,057, June 24, 2008.
19. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., Hobgood; Hudson McDonald, **Agarwal; Anant K.**, Palmour; John W., “High voltage silicon carbide MOS-bipolar devices having bi-directional blocking capabilities,” U. S. Patent #7,414,268, Aug. 19, 2008.
20. Ryu; Sei-Hyung, **Agarwal; Anant K**., “Methods of fabricating silicon carbide devices including multiple floating guard ring edge termination,” U. S. Patent #7,419,877, Sept. 2, 2008.
21. **Agarwal; Anant** , Ryu; Sei-Hyung, Donofrio; Matthew, “Methods of processing semiconductor wafers having silicon carbide power devices thereon,” U. S. Patent #7,547,578, June 16, 2009.
22. Das; Mrinal K., **Agarwal; Anant K.**, Palmour; John W., Grider; Dave, “Methods of fabricating oxide layers on silicon carbide layers utilizing atomic oxygen,” U. S. Patent #7572741, Aug. 11, 2009.
23. Hefner; Allen, Ryu; Sei-Hyung, **Agarwal; Anant**, “Power switching semiconductor devices including rectifying junction-shunts,” U. S. Patent #7,598,567, Oct. 06, 2009.
24. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., **Agarwal; Anant K.**, Palmour; John W., Hobgood; Hudson McDonald, “High voltage silicon carbide devices having bi-directional blocking capabilities,” U. S. Patent #7,615,801, Nov. 10, 2009.
25. **Agarwal; Anant K.**, Krishnaswami; Sumithra, Richmond, Jr.; James T., “Optically triggered wide bandgap bipolar power switching devices and circuits,” U. S. Patent #7,679,223, Mar. 06, 2010.
26. Zhang; Qingchun, Ryu; Sei-Hyung, **Agarwal; Anant**, “Semiconductor devices including schottky diodes with controlled breakdown,” U. S. Patent #7,728,402, Jun. 01, 2010.

27. Zhang; Qingchun, Haney; Sarah, **Agarwal; Anant**, "Semiconductor transistor with P type re-grown channel layer," U. S. Patent #7,795,691, Sept. 14, 2010.
28. Zhang; Qingchun, **Agarwal; Anant K.**, "Power semiconductor devices with mesa structures and buffer layers including mesa steps," U. S. Patent #7,838,377, Nov. 23, 2010.
29. Ryu; Sei-Hyung, **Agarwal; Anant K.**, "Methods of fabricating silicon carbide devices incorporating multiple floating guard ring edge terminations," U. S. Patent #7,842,549, Nov. 30, 2010.
30. Zhang; Qingchun, **Agarwal; Anant**, Jonas; Charlotte, "Transistor with A-face conductive channel and trench protecting well region," U. S. Patent # 7,989,882, Aug. 2, 2011.
31. Hefner; Allen, Ryu; Sei-Hyung, **Agarwal; Anant**, "Methods of forming power switching semiconductor devices including rectifying junction-shunts," U. S. Patent #8,034,688, Oct. 11, 2011.
32. Zhang; Qingchun, **Agarwal; Anant K.**, "Mesa termination structures for power semiconductor devices including mesa step buffers," U. S. Patent #8,097,919, Jan. 17, 2012.
33. Das; Mrinal K., Agarwal; Anant K., Palmour; John W., Grider; Dave, "Methods of fabricating oxide layers on silicon carbide layers utilizing atomic oxygen," U. S. Patent #8,119,539, Feb. 21, 2012.
34. Ryu; Sei-Hyung, **Agarwal; Anant K.**, "Methods of fabricating silicon carbide devices incorporating multiple floating guard ring edge terminations," U. S. Patent #8,124,480, Feb. 28, 2012.
35. Bipolar junction transistor structure for reduced current crowding, Lin Cheng, Anant K. Agarwal, Sei-Hyung Ryu, US 20130146894 A1, Jun 13, 2013
36. Stable power devices on low-angle off-cut silicon carbide crystals, Qingchun Zhang, **Anant Agarwal**, Doyle Craig Capell, Albert Burk, Joseph Sumakeris, Michael O'Loughlin, US 8536582 B2, Sep 17, 2013
37. Mesa termination structures for power semiconductor devices and methods of forming power semiconductor devices with mesa termination structures, Qingchun Zhang, **Anant Agarwal**, US 8460977 B2, Jun 11, 2013
38. Semiconductor devices with current shifting regions and related methods, Qingchun Zhang, Anant K. Agarwal, US 8497552 B2, Jul 30, 2013
39. Power switching semiconductor devices including rectifying junction-shunts, Allen Hefner, Sei-Hyung Ryu, **Anant Agarwal**, US 8546874 B2, Oct 1, 2013
40. Electronic device structure including a buffer layer on a base layer, US 8552435 B2Oct 8, 2013 Qingchun Zhang, **Anant Agarwal**
41. Forming SiC mosfets with high channel mobility by treating the oxide interface with cesium ions, Sarit Dhar, Sei-Hyung Ryu, **Anant Agarwal**, John Robert Williams, US 20130034941 A1, Feb 7, 2013
42. Edge termination structure employing recesses for edge termination elements, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8618582 B2, Dec 31, 2013
43. Schottky diode employing recesses for elements of junction barrier array, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8664665 B2, Mar 4, 2014
44. High power insulated gate bipolar transistors, Qingchun Zhang, Sei-Hyung Ryu, Charlotte Jonas, **Anant Agarwal**, US 8710510 B2, Apr 29, 2014
45. Schottky diode, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8680587 B2, Mar 25, 2014
46. Diffused junction termination structures for silicon carbide devices and methods of fabricating silicon carbide devices incorporating same, Qingchun Zhang, **Anant K.Agarwal**, Tangali S. Sudarshan, Alexander Bolotnikov, US 8637386 B2, Jan 28, 2014
47. Silicon carbide junction barrier Schottky diodes with suppressed minority carrier injection, Sei-Hyung Ryu, , **Anant K.Agarwa**l, US 8901699 B2, Dec 2, 2014
48. Diffused Junction Termination Structures for Silicon Carbide Devices, Qingchun Zhang, **Anant K.Agarwal**, Tangali S. Sudarshan, Alexander Bolotnikov, US 20140097450 A1, Apr 10, 2014
49. Monolithically integrated vertical power transistor and bypass diode, Vipindas Pala, Lin Cheng, **Anant K.Agarwal**, John Williams Palmour, Edward Robert Van Brunt, US 20150084125 A1, Mar 26, 2015
50. Field effect transistor devices with regrown p-layers, Lin Cheng, **Anant Agarwal**, John Palmour, US 9012984 B2, Apr 21, 2015
51. Field effect transistor devices with low source resistance, Sei-Hyung Ryu, Doyle Craig Capell, Lin Cheng, Sarit Dhar, Charlotte Jonas, **Anant Agarwal**, John Palmour, US 9142662 B2, Sep 22, 2015
52. Field effect device with enhanced gate dielectric structure, Daniel Jenner Lichtenwalner, **Anant Agarwal**, Lin Cheng, Vipindas Pala, John Williams Palmour, US 9111919 B2, Aug 18, 2015
53. Methods of forming junction termination extension edge terminations for high power semiconductor devices and related semiconductor devices, Edward Robert Van Brunt, Vipindas Pala, Lin Cheng, **Anant Agarwal,** US 9064738 B2 Jun 23, 2015
54. Field effect transistor devices with buried well protection regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 9142668 B2, Sep 22, 2015
55. Electronic device structure with a semiconductor ledge layer for surface passivation, Qingchun Zhang, **Anant Agarwal**, US 9059197 B2, Jun 16, 2015
56. Enhanced gate dielectric for a field effect device with a trenched gate, Daniel Jenner Lichtenwalner, Lin Cheng, **Anant Kumar Agarwal**, John Williams Palmour, US 20150021623 A1, Jan 22, 2015

57. Transistor with A-face conductive channel and trench protecting well region, Qingchun Zhang, **Anant Agarwal**, Charlotte Jonas, US 9064710 B2, Jun 23, 2015
58. Edge termination technique for high voltage power devices, Edward Robert Van Brunt, Vipindas Pala, Lin Cheng, **Anant Kumar Agarwal**, US 20150048489 A1, Feb 19, 2015
59. Field effect transistor devices with protective regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 9306061 B2, Apr 5, 2016
60. Vertical power transistor device, Vipindas Pala, **Anant Kumar Agarwal**, Lin Cheng, Daniel Jenner Lichtenwalner, John Williams Palmour, US 20160211360 A1 Jul 21, 2016
61. Field Effect Transistor Devices with Buried Well Protection Regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 20160005837 A1, Jan 7, 2016
62. Transistors with semiconductor interconnection layers and semiconductor channel layers of different semiconductor materials, Qingchun Zhang, Sei-Hyung Ryu, **Anant K. Agarwal**, Sarit Dhar, US 9312343 B2, Apr 12, 2016
63. Semiconductor devices in SiC using vias through N-type substrate for backside contact to P-type layer, Vipindas Pala, Edward Robert Van Brunt, Daniel Jenner Lichtenwalner, Lin Cheng, **Anant Agarwal**, John Williams Palmour, US 9236433 B2, Jan 12, 2016
64. Semiconductor device with increased channel mobility and dry chemistry processes for fabrication thereof, Sarit Dhar, Lin Cheng, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Jason Gurganus, US 9269580 B2, Feb 23, 2016.
65. Bipolar junction transistor structure for reduced current crowding, Inventors: Lin Cheng, **Anant K. Agarwal**, Sei-Hyung Ryu, Filed: December 12, 2011, Date of Patent: September 5, 2017, Assignee: Cree, Inc., Patent number: 9755018
66. Power module having a switch module for supporting high current densities, Inventors: Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Kumar Agarwal**, John Williams Palmour, Scott Allen, Filed: April 10, 2017, Date of Patent: December 11, 2018, Assignee: Cree, Inc., Patent number: 10153364
67. Schottky diode, Inventors: Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Kumar Agarwal**, John Williams Palmour, Scott Allen, Filed: July 28, 2015, Date of Patent: January 9, 2018, Assignee: Cree, Inc., Patent number: 9865750

Book Chapters

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