Patents

1. **Anant K. Agarwal**, Richard R. Siergiej, Charles D. Brandt and Marvin H. White, “A non-volatile random-access memory Cell Constructed of Silicon Carbide,” U.S. Patent No. 5,510,630, April 23, 1996.
2. **Anant K. Agarwal**, Rowan L. Messham and Michael C. Driver, “Aluminum Gallium Nitride based Heterojunction Bipolar Transistor,” U.S. Patent No. 5,641,975, June 24, 1997.
3. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, Charles D. Brandt, “Static Induction Transistors,” U.S. Patent No. 5,705,830, June 6, 1998.
4. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, abd Charles D. Brandt, "Silicon Carbide Static Induction Transistor Structure," U.S. Patent No. 5,903,020, May 11, 1999.
5. **Anant K. Agarwal**, Rowan L. Messham and Michael C. Driver, "Aluminum Gallium Nitride Heterojunction Bipolar Transistors," U. S. Patent No. 5,923,058, July 13, 1999.
6. Richard R. Siergiej, **Anant K. Agarwal**, Rowland C. Clarke, abd Charles D. Brandt, "Static Induction Transistor," U.S. Patent No. 5,945,701, Aug. 31, 1999.
7. R. Singh, **A. K. Agarwal**, and S. Ryu, **“**Method of fabricating a self-aligned bipolar junction transistor in silicon carbide and resulting devices,” U.S. Patent #6,218,254, April 17, 2001.
8. R. Singh, **A. K. Agarwal**, and S. Ryu, **“**Self-aligned bipolar junction silicon carbide transistors,” U.S. Patent #6,329,675, Dec. 11, 2001.
9. S. Ryu, J.J. Sumakeris, **A. K. Agarwal**, and R. Singh **“**Methods of fabricating silicon carbide inversion channel devices without the need to utilize P-type implantation,” U.S. Patent #6,429,041, Aug. 6, 2002.
10. S. Ryu, **A. K. Agarwal**, C. Capell, and J. W. Palmour, **“**Large area silicon carbide devices and manufacturing methods therefor,” U.S. Patent #6,514,779, Feb. 4, 2003.
11. S. Ryu, J.J. Sumakeris, **A. K. Agarwal**, and R. Singh, **“**Silicon carbide inversion channel mosfets,” U.S. Patent #6,653,659, Nov. 25, 2003.
12. **A. K. Agarwal,** S. Ryu, and J. W. Palmour, **“**Large area silicon carbide devices,” U.S. Patent #6,770,911, Aug. 3, 2004.
13. Sei-Hyung Ryu, **Anant Agarwal**, Mrinal Kanti Das, Lori A. Lipkin, John W. Palmour, Ranbir Singh, "Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors having a shorting channel and methods of fabricating Silicon Carbide Field Effect Transistors having a shorting channel," U. S. Patent #6,956,238, October 18, 2005.
14. Sei-Hyung Ryu and **Anant K. Agarwal**, "Multiple Floating Guard Ring Edge Termination for Silicon Carbide Devices," U. S. Patent #7,026,650, April 11, 2006.
15. **Agarwal; Anant**, Ryu; Sei-Hyung, Palmour; John W., “Manufacturing methods for large area silicon carbide devices,” U. S. Patent #7,135,359, Nov. 14, 2006.
16. **Agarwal; Anant K**., Krishnaswami; Sumithra, Ryu; Sei-Hyung, Hurt; Edward Harold, “Silicon carbide bipolar junction transistors having epitaxial base regions and multilayer emitters and methods of fabricating the same,” U. S. Patent #7,304,334, Dec. 4, 2007.
17. **Agarwal; Anant K**., Krishnaswami; Sumithra, Ryu; Sei-Hyung, Capell; D. Craig, “Silicon carbide bipolar junction transistors having a silicon carbide passivation layer on the base region thereof,” U. S. Patent #7,345,310, March 18, 2008.
18. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., Hobgood; Hudson McDonald, **Agarwal; Anant K.**, Palmour; John W., “High voltage silicon carbide devices having bi-directional blocking capabilities,” U. S. Patent #7,391,057, June 24, 2008.
19. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., Hobgood; Hudson McDonald, **Agarwal; Anant K.**, Palmour; John W., “High voltage silicon carbide MOS-bipolar devices having bi-directional blocking capabilities,” U. S. Patent #7,414,268, Aug. 19, 2008.
20. Ryu; Sei-Hyung, **Agarwal; Anant K**., “Methods of fabricating silicon carbide devices including multiple floating guard ring edge termination,” U. S. Patent #7,419,877, Sept. 2, 2008.
21. **Agarwal; Anant** , Ryu; Sei-Hyung, Donofrio; Matthew, “Methods of processing semiconductor wafers having silicon carbide power devices thereon,” U. S. Patent #7,547,578, June 16, 2009.
22. Das; Mrinal K., **Agarwal; Anant K.**, Palmour; John W., Grider; Dave, “Methods of fabricating oxide layers on silicon carbide layers utilizing atomic oxygen,” U. S. Patent #7572741, Aug. 11, 2009.
23. Hefner; Allen, Ryu; Sei-Hyung, **Agarwal; Anant**, “Power switching semiconductor devices including rectifying junction-shunts,” U. S. Patent #7,598,567, Oct. 06, 2009.
24. Ryu; Sei-Hyung, Jenny; Jason R., Das; Mrinal K., **Agarwal; Anant K.**, Palmour; John W., Hobgood; Hudson McDonald, “High voltage silicon carbide devices having bi-directional blocking capabilities,” U. S. Patent #7,615,801, Nov. 10, 2009.
25. **Agarwal; Anant K.**, Krishnaswami; Sumithra, Richmond, Jr.; James T., “Optically triggered wide bandgap bipolar power switching devices and circuits,” U. S. Patent #7,679,223, Mar. 06, 2010.
26. Zhang; Qingchun, Ryu; Sei-Hyung, **Agarwal; Anant**, “Semiconductor devices including schottky diodes with controlled breakdown,” U. S. Patent #7,728,402, Jun. 01, 2010.

27. Zhang; Qingchun, Haney; Sarah, **Agarwal; Anant**, "Semiconductor transistor with P type re-grown channel layer," U. S. Patent #7,795,691, Sept. 14, 2010.
28. Zhang; Qingchun, **Agarwal; Anant K.**, "Power semiconductor devices with mesa structures and buffer layers including mesa steps," U. S. Patent #7,838,377, Nov. 23, 2010.
29. Ryu; Sei-Hyung, **Agarwal; Anant K.**, "Methods of fabricating silicon carbide devices incorporating multiple floating guard ring edge terminations," U. S. Patent #7,842,549, Nov. 30, 2010.
30. Zhang; Qingchun, **Agarwal; Anant**, Jonas; Charlotte, "Transistor with A-face conductive channel and trench protecting well region," U. S. Patent # 7,989,882, Aug. 2, 2011.
31. Hefner; Allen, Ryu; Sei-Hyung, **Agarwal; Anant**, "Methods of forming power switching semiconductor devices including rectifying junction-shunts," U. S. Patent #8,034,688, Oct. 11, 2011.
32. Zhang; Qingchun, **Agarwal; Anant K.**, "Mesa termination structures for power semiconductor devices including mesa step buffers," U. S. Patent #8,097,919, Jan. 17, 2012.
33. Das; Mrinal K., Agarwal; Anant K., Palmour; John W., Grider; Dave, "Methods of fabricating oxide layers on silicon carbide layers utilizing atomic oxygen," U. S. Patent #8,119,539, Feb. 21, 2012.
34. Ryu; Sei-Hyung, **Agarwal; Anant K.**, "Methods of fabricating silicon carbide devices incorporating multiple floating guard ring edge terminations," U. S. Patent #8,124,480, Feb. 28, 2012.
35. Bipolar junction transistor structure for reduced current crowding, Lin Cheng, Anant K. Agarwal, Sei-Hyung Ryu, US 20130146894 A1, Jun 13, 2013
36. Stable power devices on low-angle off-cut silicon carbide crystals, Qingchun Zhang, **Anant Agarwal**, Doyle Craig Capell, Albert Burk, Joseph Sumakeris, Michael O'Loughlin, US 8536582 B2, Sep 17, 2013
37. Mesa termination structures for power semiconductor devices and methods of forming power semiconductor devices with mesa termination structures, Qingchun Zhang, **Anant Agarwal**, US 8460977 B2, Jun 11, 2013
38. Semiconductor devices with current shifting regions and related methods, Qingchun Zhang, Anant K. Agarwal, US 8497552 B2, Jul 30, 2013
39. Power switching semiconductor devices including rectifying junction-shunts, Allen Hefner, Sei-Hyung Ryu, **Anant Agarwal**, US 8546874 B2, Oct 1, 2013
40. Electronic device structure including a buffer layer on a base layer, US 8552435 B2Oct 8, 2013 Qingchun Zhang, **Anant Agarwal**
41. Forming SiC mosfets with high channel mobility by treating the oxide interface with cesium ions, Sarit Dhar, Sei-Hyung Ryu, **Anant Agarwal**, John Robert Williams, US 20130034941 A1, Feb 7, 2013
42. Edge termination structure employing recesses for edge termination elements, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8618582 B2, Dec 31, 2013
43. Schottky diode employing recesses for elements of junction barrier array, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8664665 B2, Mar 4, 2014
44. High power insulated gate bipolar transistors, Qingchun Zhang, Sei-Hyung Ryu, Charlotte Jonas, **Anant Agarwal**, US 8710510 B2, Apr 29, 2014
45. Schottky diode, Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Scott Allen, US 8680587 B2, Mar 25, 2014
46. Diffused junction termination structures for silicon carbide devices and methods of fabricating silicon carbide devices incorporating same, Qingchun Zhang, **Anant K.Agarwal**, Tangali S. Sudarshan, Alexander Bolotnikov, US 8637386 B2, Jan 28, 2014
47. Silicon carbide junction barrier Schottky diodes with suppressed minority carrier injection, Sei-Hyung Ryu, , **Anant K.Agarwa**l, US 8901699 B2, Dec 2, 2014
48. Diffused Junction Termination Structures for Silicon Carbide Devices, Qingchun Zhang, **Anant K.Agarwal**, Tangali S. Sudarshan, Alexander Bolotnikov, US 20140097450 A1, Apr 10, 2014
49. Monolithically integrated vertical power transistor and bypass diode, Vipindas Pala, Lin Cheng, **Anant K.Agarwal**, John Williams Palmour, Edward Robert Van Brunt, US 20150084125 A1, Mar 26, 2015
50. Field effect transistor devices with regrown p-layers, Lin Cheng, **Anant Agarwal**, John Palmour, US 9012984 B2, Apr 21, 2015
51. Field effect transistor devices with low source resistance, Sei-Hyung Ryu, Doyle Craig Capell, Lin Cheng, Sarit Dhar, Charlotte Jonas, **Anant Agarwal**, John Palmour, US 9142662 B2, Sep 22, 2015
52. Field effect device with enhanced gate dielectric structure, Daniel Jenner Lichtenwalner, **Anant Agarwal**, Lin Cheng, Vipindas Pala, John Williams Palmour, US 9111919 B2, Aug 18, 2015
53. Methods of forming junction termination extension edge terminations for high power semiconductor devices and related semiconductor devices, Edward Robert Van Brunt, Vipindas Pala, Lin Cheng, **Anant Agarwal,** US 9064738 B2 Jun 23, 2015
54. Field effect transistor devices with buried well protection regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 9142668 B2, Sep 22, 2015
55. Electronic device structure with a semiconductor ledge layer for surface passivation, Qingchun Zhang, **Anant Agarwal**, US 9059197 B2, Jun 16, 2015
56. Enhanced gate dielectric for a field effect device with a trenched gate, Daniel Jenner Lichtenwalner, Lin Cheng, **Anant Kumar Agarwal**, John Williams Palmour, US 20150021623 A1, Jan 22, 2015

57. Transistor with A-face conductive channel and trench protecting well region, Qingchun Zhang, **Anant Agarwal**, Charlotte Jonas, US 9064710 B2, Jun 23, 2015
58. Edge termination technique for high voltage power devices, Edward Robert Van Brunt, Vipindas Pala, Lin Cheng, **Anant Kumar Agarwal**, US 20150048489 A1, Feb 19, 2015
59. Field effect transistor devices with protective regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 9306061 B2, Apr 5, 2016
60. Vertical power transistor device, Vipindas Pala, **Anant Kumar Agarwal**, Lin Cheng, Daniel Jenner Lichtenwalner, John Williams Palmour, US 20160211360 A1 Jul 21, 2016
61. Field Effect Transistor Devices with Buried Well Protection Regions, Lin Cheng, **Anant Agarwal**, Vipindas Pala, John Palmour, US 20160005837 A1, Jan 7, 2016
62. Transistors with semiconductor interconnection layers and semiconductor channel layers of different semiconductor materials, Qingchun Zhang, Sei-Hyung Ryu, **Anant K. Agarwal**, Sarit Dhar, US 9312343 B2, Apr 12, 2016
63. Semiconductor devices in SiC using vias through N-type substrate for backside contact to P-type layer, Vipindas Pala, Edward Robert Van Brunt, Daniel Jenner Lichtenwalner, Lin Cheng, **Anant Agarwal**, John Williams Palmour, US 9236433 B2, Jan 12, 2016
64. Semiconductor device with increased channel mobility and dry chemistry processes for fabrication thereof, Sarit Dhar, Lin Cheng, Sei-Hyung Ryu, **Anant Agarwal**, John Williams Palmour, Jason Gurganus, US 9269580 B2, Feb 23, 2016.
65. Bipolar junction transistor structure for reduced current crowding, Inventors: Lin Cheng, **Anant K. Agarwal**, Sei-Hyung Ryu, Filed: December 12, 2011, Date of Patent: September 5, 2017, Assignee: Cree, Inc., Patent number: 9755018
66. Power module having a switch module for supporting high current densities, Inventors: Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Kumar Agarwal**, John Williams Palmour, Scott Allen, Filed: April 10, 2017, Date of Patent: December 11, 2018, Assignee: Cree, Inc., Patent number: 10153364
67. Schottky diode, Inventors: Jason Patrick Henning, Qingchun Zhang, Sei-Hyung Ryu, **Anant Kumar Agarwal**, John Williams Palmour, Scott Allen, Filed: July 28, 2015, Date of Patent: January 9, 2018, Assignee: Cree, Inc., Patent number: 9865750