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A 600V Half-Bridge Power Stage Fully Integrated with 25V Gate-Drivers in SiC CMOS Technology

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***Abstract*— A 600V half-bridge power stage fully integrated with 25V gate-drivers is presented to demonstrate a new 0.5µm Silicon Carbide (SiC) CMOS technology. The technology allows for integrating low-voltage CMOS devices with multiple lateral high-voltage NMOS devices. Thus, multi-switch power converters or multiple power converters can be integrated along with their gate-drivers and low-voltage control circuits in the same SiC chip. The half-bridge power stage has two power switches with 500mΩ ON resistance, and it operates from a 600V input with up to 1A load and a switching frequency of 1MHz. The gate-drivers employ a capacitive level shifter and a bootstrap circuit to convert the PWM control signal from the 25V control domain to the 600V power domain. The gate-driver has a total delay of 36ns and provides a gate-driver signal with a slew rate of 23V/ns.**

***Keywords*— Half-Bridge Power Stage, SiC Integrated Circuits, SiC Gate-Drivers.**

I. INTRODUCTION

The high breakdown voltage and temperature resiliency of Silicon Carbide (SiC) makes it an attractive technology for designing power converters in a variety of applications, such as electrical vehicles, photovoltaic power generation, and aerospace applications [1-3]. However, existing power converter solutions use SiC only for the realization of the power switches, while the gate drivers and any other low-voltage analog and mixed-signal control and processing circuitry are typically realized in a separate silicon CMOS chip [4-5]. However, these multi-chip solutions significantly increase the complexity, cost, and footprint of the design. Moreover, in applications where the power converter must tolerate high temperature, such as subterranean exploration and monitoring in oil, gas and geothermal exploration [6], such approach requires large physical separation between the low-voltage gate-drivers and the control and processing circuits implemented in silicon CMOS on the one side, and the power stage implemented in SiC on the other side. This large physical separation may not be feasible in some applications and further complicates the design and increases cost and footprint. Thus, there is a need for fully integrating high-voltage power switches with low-voltage gate-drivers and other processing circuits together in the same SiC chip.

Early attempts for developing SiC technologies capable of integrating low-voltage and high-voltage devices together on the same chip have been recently reported. One example is the technology introduced in [7], which integrates a 1.2kV vertical power MOSFET with a 25V CMOS inverter in a single SiC chip. However, due to its vertical structure, only one power MOSFET can be realized on the chip. This makes the technology unsuitable for power converters with multiple power switches or for integrating multiple power converters. Another example is the technology introduced in [8-9], which integrates low-voltage CMOS circuits with a 600V lateral power MOSFET. However, the lack of isolation between the CMOS devices and the power MOSFET, as well as between the power MOSFETs themselves, makes it difficult to design complex or multiple power converters in the same chip.

In this paper, we introduce a capacitive 25V gate-driver circuit integrated with a 600V half-bridge power stage in the same SiC CMOS chip. The purpose is to demonstrate a new SiC technology that allows for the integration of low-voltage CMOS circuits with multiple high-voltage lateral power MOSFETs, and thus, can be used for realizing multi-switch power converters or multiple power converters in the same chip, along with gate-drivers and low-voltage control circuits. First, we will give an overview of the technology, then the design details and results of the gate-driver and power stage.

II. OVERVIEW OF THE PROPOSED SIC TECHNOLOGY

Fig. 1(a) illustrates the physical structure of the low-voltage CMOS devices, and the high-voltage NMOS power device in the proposed 0.5µm SiC technology [10-11]. The P+ isolation regions serve two key purposes. First, they allow independent biasing of the bulk of each low-voltage transistor. This provides circuit design flexibility and eliminates the body effect by allowing connecting the bulk of any transistor to its source. Second, they allow multiple high-voltage devices to coexist in the same chip without sharing the same drain terminal. This enables designers to integrate multiple power converters (or converters with several power switches) in the same chip. The P+ isolation regions are designed to withstand 600V. The low-voltage CMOS devices have a threshold voltage of ~6V with a rating of 25V across all junctions. The high-voltage NMOS power devices have a threshold voltage of ~6V with a rating of 600V across the drain-source and gate-drain junctions and 25V across the gate-source junction. Level-2 SPICE models have been developed for the devices through TCAD process and device simulations. Fig. 1(b) shows the simulated output characteristics of samples of the low-voltage and high-voltage devices. Additional details about this proposed SiC technology can be found in [10-11].

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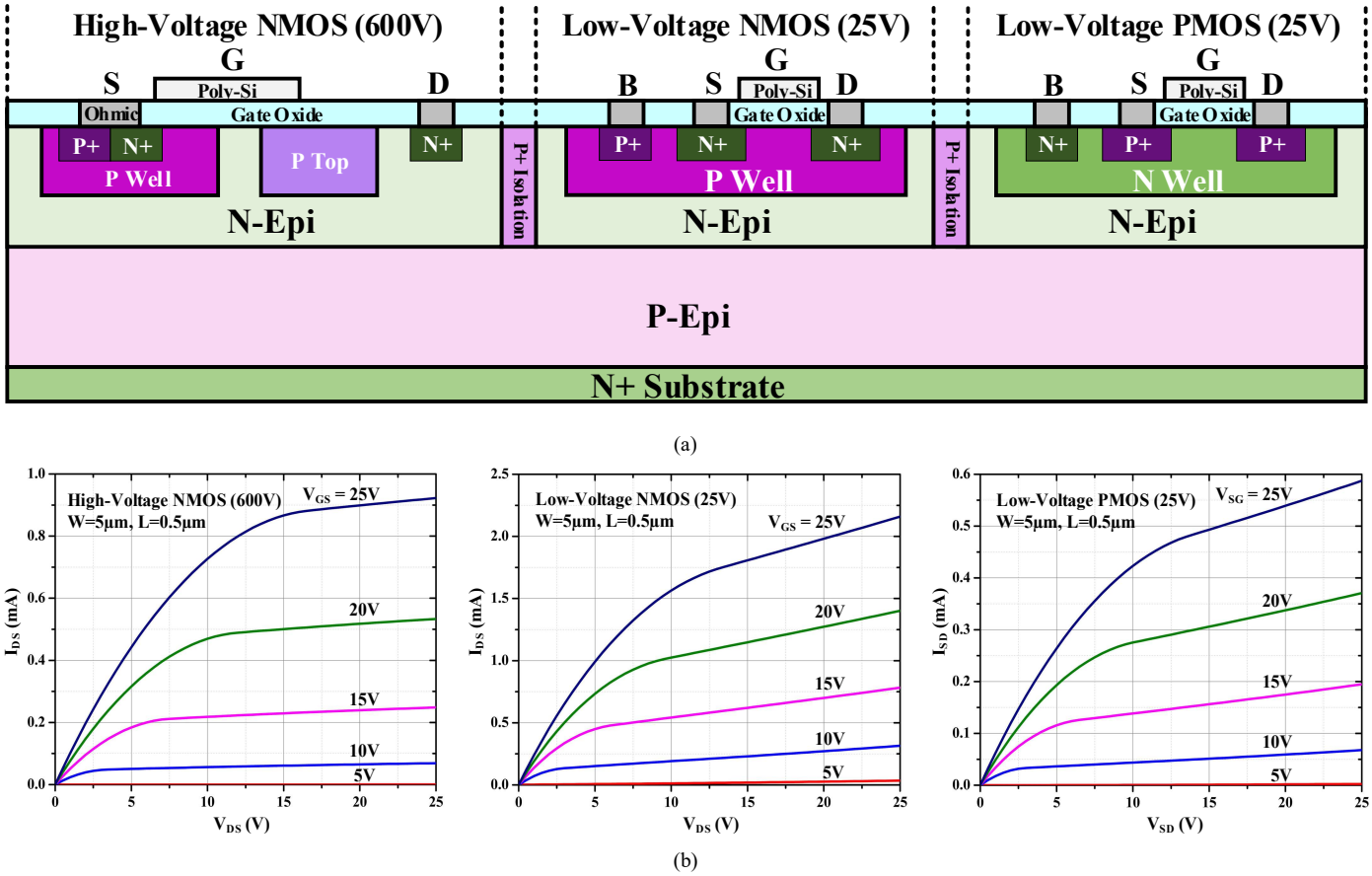

Fig. 1: (a) Cross-sectional views of the various types of MOS transistors in the proposed SiC technology, and (b) their corresponding current-voltage characteristics

III. GATE-DRIVER AND HALF-BRIDGE POWER STAGE

A half-bridge power stage is an essential building block in many power converters, such as buck, boost, and buck-boost. Thus, it is typically the first circuit to be implemented to demonstrate any new power IC technology. The block diagram of a half-bridge power stage and its gate-drivers is shown in Fig. 2. The power stage is formed by two power switches that share a switching node "V_{SW}". The high-side switch controls the current flow from the input power source, while the low-side switch controls the current flow to ground. Although it is common in low-power applications to use a PMOS for the high-side switch, an NMOS is favored in high-power applications due to its lower overall losses compared to PMOS. This results in better power conversion efficiency but at the expense of a more complicated gate-driver.

The gate-drivers are mixed-voltage circuits that receive the control signals from the low-voltage processing domain, operating from V_{DDC} and GND_C, and produce corresponding signals at the appropriate voltage levels and drive capability to control the power switches operating from V_{IN} and GND_P. As shown in Fig. 2, the gate-drivers are composed of a level shifter and a buffer. The level shifter is responsible for translating the control signals from the low-voltage domain to the power domain, while the buffer, which is simply an inverter chain, is responsible for enhancing the drive

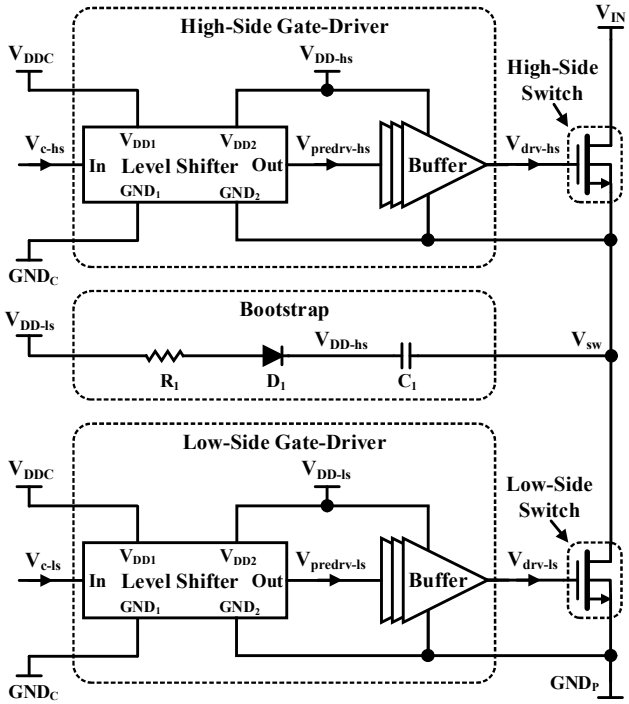

Fig. 2 Block diagram of the half-bridge power stage and its gate-drivers. V_{IN}, $V_{DD\text{-}hs}$, and V_{DDC} are 600V, 625V, and 25V, respectively.

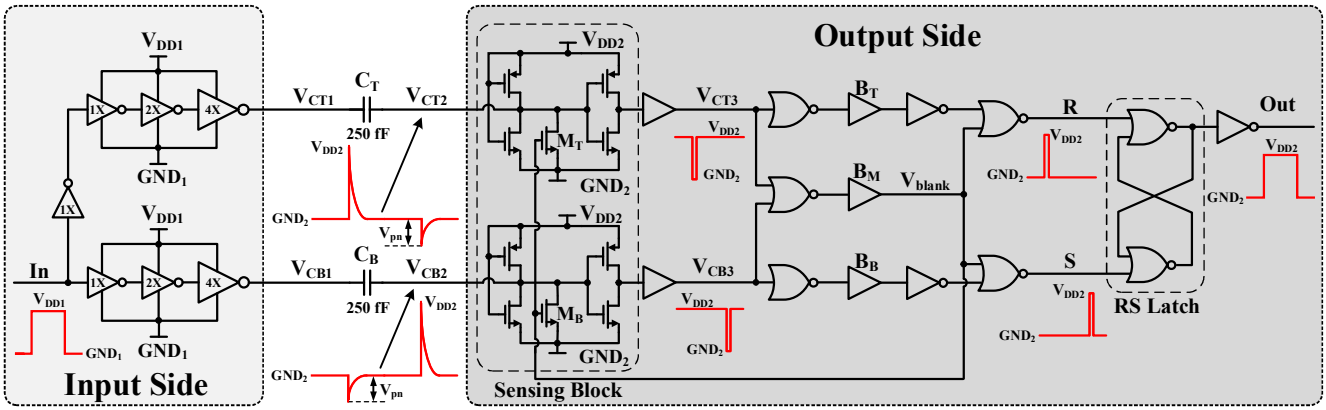

Fig. 3 Schematic diagram of the level shifter within the gate-driver of Fig. 2.

capability of these signals in order to drive the large gate capacitance of the power switches. The high-side and low-side gate-drivers are identical from a circuit design standpoint, except for their power supplies and ground levels. On the one hand, in order to turn the low-side NMOS power switch OFF, its driving signal $V_{drv\text{-}ls}$ needs its logic-low level to be GND_P, while its logic-high must exceed GND_P by a sufficient amount (i.e. $V_{DD\text{-}ls}$) to turn the power switch ON. Thus, the buffer stage and the output side of the level shifter in the low-side gate-driver must operate from $V_{DD\text{-}ls}$ and GND_P. On the other hand, in order to turn the high-side NMOS power switch OFF, the driving signal $V_{drv\text{-}hs}$ must have a logic-low level that is equal to the dynamic switching node V_{sw} of the power stage, while its logic-high must be higher than V_{sw} with an amount sufficient to turn the power switch ON. Therefore, the buffer stage and the output side of the level shifter in the high-side gate-driver must use V_{sw} as their ground and $V_{DD\text{-}hs}$ as their power supply, where $V_{DD\text{-}hs}$ is always higher than V_{sw} by the fixed amount $V_{DD\text{-}ls}$. Since V_{sw} reaches V_{IN} when the high-side power switch is turned ON, $V_{DD\text{-}hs}$ can be realized using the simple bootstrap circuit shown in Fig. 2. Finally, the input side of the level shifter in both gate-drivers must operate from V_{DDC} and GND_C since they interface with the low-voltage control domain. For this SiC technology, the low-voltage CMOS devices are rated for 25V, and thus, V_{DDC} is selected to be 25V to maximize the dynamic range of any analog/digital circuits implemented in the technology. Moreover, since the gate-source junction of the high-voltage NMOS devices is rated for 25V, $V_{DD\text{-}ls}$ is selected to be 25V and $V_{DD\text{-}hs}$ is selected to be higher than the switching node voltage V_{sw} by also 25V. These selections minimize the ON resistance of the power switches by using the maximum allowed gate-source voltage. They also reduce the number of power supplies needed for the design as only one power supply is needed for $V_{DD\text{-}C}$, $V_{DD\text{-}ls}$, and $V_{DD\text{-}hs}$.

Fig. 3 shows the design of the level shifter, which is a modified version of the topology in [12]. A key advantage of this capacitive-coupling-based topology over conventional topologies is its mostly digital realization. This makes it very robust to process, voltage, and temperature (PVT) variations, as well as device model inaccuracy, which is very convenient for demonstration of new implementation technologies.

The working principle of the level shifter can be understood through the signal depictions shown in Fig. 3. First, two complementary versions, V_{CT1} and V_{CB1}, of the input signal are generated at one side of the coupling capacitors C_T and C_B. At the rising edge of the input signal, the other side of the capacitors, V_{CT2} and V_{CB2}, will exhibit a positive and a negative pulse, respectively. These pulses will propagate through the sensing block and the following digital logic to reset the RS latch, which produces a final logic-high output. At the falling edge of the input signal, a similar but complementary dynamic takes place that yields a final logic-low output. Since the sensing block, the following logic, and the RS latch are all operating in the power domain, the logic-high and logic-low levels of the output side of the level shifter will be $V_{DD\text{-}hs}$ and V_{sw}, respectively, in the case of the high-side gate-driver, and $V_{DD\text{-}ls}$ and GND_p, respectively, in the case of the low-side gate-driver. It is worth noting that the pull-down transistors M_T and M_B (controlled by the feedback signal V_{blank}) are used for two key reasons: (a) clamping the negative pulses in V_{CT2} and V_{CB2} to only one diode voltage drop (i.e. V_{pn}) below GND_2, and (b) preventing any racing conditions at the inputs of the RS latch, which may emerge if GND_2 is dynamic. This is necessary in the high-side gate-driver since GND_2 is connected to V_{sw}. It is also worth noting that the buffers B_T, B_B, and B_M ensure that the rising edge of V_{blank} always arrives earlier at the following NOR-gate stages than the rising edges of V_{CT3} and V_{CB3}, while its falling edge arrives later. This prevents unintended glitches when if GND_2 is dynamic, which is the case in the high-side gate-driver.

IV. Simulation Results And Layout

The half-bridge power stage with integrated gate-drivers is designed in the proposed 0.5µm SiC technology described in section II. Fig. 4 shows the layout of the design with the various parts highlighted. The total area of the design is 21.5mm^2, 15.8% of which is for the power switches and 84.2% is for the gate-drivers. As shown in Fig. 4, the level shifters take up only a small area of the gate-drivers (less than 2.5%), while most area is taken by the gate-drivers buffer stages.

The half-bridge power stage is designed to operate with a 600V input, up to 1A load, and switching frequency of 1MHz. In applications with a 5V output, 90% efficiency would

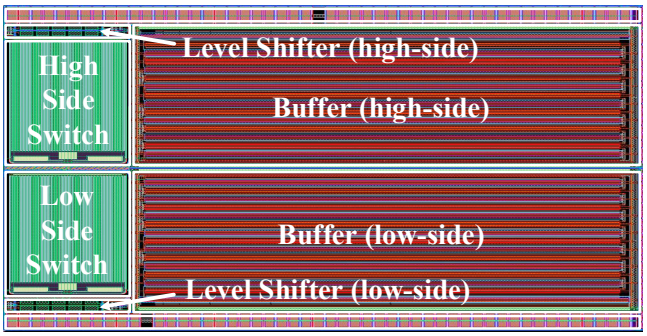

Fig. 4 Layout of the half-bridge power stage and gate-drivers in SiC.

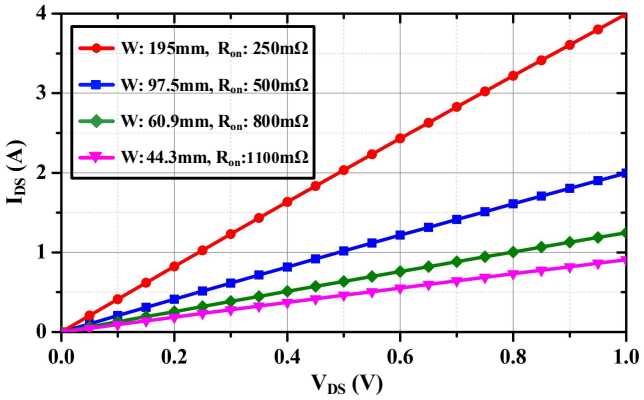

Fig. 5 The I-V characteristics and ON-resistance of the high-voltage NMOS power switch with 0.5µm length, 25V gate-source voltage, and various widths.

require the power switches to have ~555mΩ ON-resistance. In order to achieve such ON-resistance with the minimum possible device width, the power switches are turned ON using their maximum rated gate-source voltage (25V). They are also designed with the minimum length of the technology (0.5µm). Fig. 5 shows the simulated output characteristics of the power switches under these conditions for various widths. For this design, a width of 97.5mm is selected, which yields an ON-resistance of 500mΩ. Finally, the full design is simulated using Level-2 SPICE models of the technology with 50% switching duty cycle. Fig. 6 shows the waveforms of the key signals within the design. The switching node V_{sw} has a slew rate of 31V/ns, while the final gate-drive signals $V_{drv\text{-}hs}$ and $V_{drv\text{-}ls}$ has a slew rate of 23V/ns and 21V/ns, respectively. The delay of the entire gate driver circuit is 36ns.

V. Conclusion

A fully integrated half-bridge power stage with 25V gate-drivers is designed to demonstrate a new 0.5µm SiC CMOS technology. The power stage has two 0.5Ω power FETs switching at 1MHz with 600V input and up to 1A load. The gate-drivers employ a capacitive level shifter to convert the PWM control signal from the 25V control domain to the 600V power domain. The propagation delay of the gate driver is 36ns, while the slew rate of the high-side and low-side gate-drive signals are 23V/ns and 21V/ns, respectively. The switching node of the power stage has a slew rate of 31V/ns.

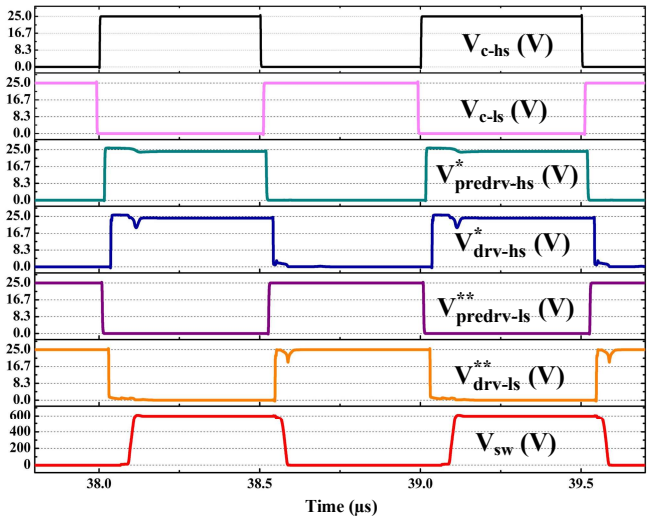

Fig. 6 Tranisent simulations of the proposed half-bridge power stage and gate-drivers in SiC. * Referenced to V_{sw} , ** Referenced to GND_P.

Ackownledgement

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