Bias-induced Threshold Voltage Instability and Interface Trap Density Extraction of 4H-SiC MOSFETs

Susanna Yu, Minseok Kang, Tianshi Liu, Diang Xing, Arash Salemi, Marvin H. White and Anant K. Agarwal
Department of Electrical and Computer Engineering
The Ohio State University, Columbus, OH, 43210, USA
Email: yu.2452@osu.edu

***Abstract*—In this paper, the results of electrical reliability measurements of commercially available 1200 V Silicon Carbide (SiC) MOSFETs are reported. The threshold voltage shift caused by interface states and the trapped charges near the SiC/SiO_2 interface is observed under positive and negative DC-bias-stress over 50 hours. Threshold voltage reduction with temperature is also reported for devices from different vendors. Negative shift of subthreshold characteristics under the negative bias stress and high drain bias at elevated temperature indicates that the threshold voltage of the devices should be increased by at least 1-2 V. Extracted interface state density using subthreshold *I-V* curves indicates very different SiC/SiO_2 interface for devices from different vendors.**

Keywords—Silicon Carbide (SiC), MOSFETs, reliability, threshold voltage instability.

I. INTRODUCTION

Given the unique properties such as wide bandgap, high electric field, and high thermal conductivity, Silicon Carbide (SiC) semiconductor devices are being developed to replace the conventional Silicon (Si) power devices that are approaching the fundamental material limits in power electronic applications [1]. However, MOS-based SiC devices that are currently commercially available in the market may lack ruggedness in certain aspects. In order to reduce device cost, some tradeoffs between device size and ruggedness have to be made. In recent years, a number of potential issues for SiC MOSFETs have been reported including very low short-circuit times [2], threshold voltage instability [3], body-diode robustness [4], and gate leakage currents at high temperatures [5]. Threshold voltage instability, studied in this work is caused by a high density of traps and trapped charges at or near the interface of SiC/SiO_2 [6, 7]. This charge trapping is closely related to the low inversion layer mobility which results in high channel resistance. Although the exact reason of high interface state density is not known, the possibility of presence of silicon dangling bonds and carbon clusters at the interface of SiC/SiO_2 has been reported in the literatures [8].

Threshold voltage instability arises when carriers are injected into the near interface traps. Due to the existence of these traps, the threshold value shifts in the positive direction as electrons are captured by traps when a positive DC bias is applied to the gate over a long period of time. Conversely, when a negative bias is applied to the gate over a long period of time, the threshold voltage shifts in the negative direction resulting in a significant increase in leakage current in the off-state. It is worthwhile to study the threshold voltage instability of the commercial devices in order to evaluate whether the devices are deemed robust for automotive applications which require stringent reliability requirements. It should be noted that a negative shift of threshold voltage might cause devices to turn on unexpectedly and lead to failures. In this work, threshold voltage instability of commercial SiC MOSFETs is observed under bias-stress and elevated temperature. Increase of leakage current caused by negatively shifting subthreshold characteristics is also presented as a function of various stresses. Measured values of interface state densities indicate that further improvement is required to achieve the reliable operation of commercial devices.

II. EXPERIMENTAL RESULTS AND DISCUSSION

A. Bias-induced threshold voltage instability

Particular trap-induced device degradation on commercially available SiC MOSFETs is investigated by applying a positive and negative DC voltage stress on the gate over a long period of time with source and drain grounded. The devices under test are from three vendors and the general information is shown in Table I. For this test, 5 devices from each vendor were utilized. Test circuits were fabricated to stress 15 devices at the same time by tying the gates together in parallel. Two positive (20 V, 30 V) and one negative (-10 V) bias stresses were applied to the gate for 10, 20, and 50 hours at room temperature. Before and after each stress test, drain current was measured as a function of gate voltage when gate and drain were tied together to determine the threshold voltage shift. Threshold voltage was obtained by the constant-current (CC) method as a gate voltage required to flow 10 mA of drain current using an Agilent 4145 parameter analyzer [9]. After the completion of positive gate stress for 50 hours, -10 V was applied to the gate for 10 minutes to release the electrons captured near the SiC/SiO_2 interface during the positive bias stress and reset the devices. Likewise, after completing the negative bias stress measurements, +10 V was applied for 10 minutes to restore devices to initial condition. The sequence for bias-induced threshold voltage instability measurement is depicted in Fig. 1.

TABLE I. DEVICES UNDER TEST (DUTS)

Vendors	*Type*	*Voltage Rating*	*Current Rating*	*Typ. RDS-on*
C	DMOSFET	1200 V	12 A	600 mΩ
D	T-MOSFET	1200 V	17 A	200 mΩ
E'	DMOSFET	1200 V	10 A	380 mΩ

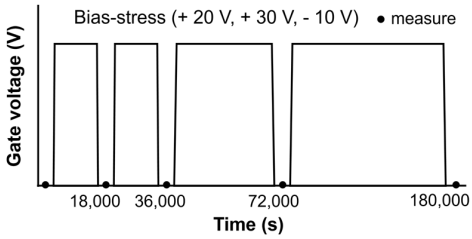

Fig. 1. The sequence for bias-induced threshold voltage instability measurement.

Time-dependent threshold voltage shifts with various bias-stresses are shown in Fig. 2. Error bars at each point represent the variation in 5 devices. The threshold shift was determined by subtracting the pre-stress threshold voltage from post-stress threshold voltage. When a positive DC bias of +20 V is applied to the gate for 50 hours, the threshold values shift in the positive direction about 0.5 V, 0.35 V, and 0.06 V for devices from vendor C, D, and E', respectively (see Fig. 2 (a)). For the DC bias of +30 V, again devices from vendor C (device C) show the largest amount of shift about 0.74 V after 50 hours of stress and devices from vendor E' (device E) show the smallest amount of shift about 0.27 V (see Fig.2 (b)). Conversely, when a negative bias of -10 V is applied to the gate for 50 hours, the threshold voltage shifts in the negative direction. The maximum shift about -0.2 V is shown in device C while others show less than -0.1 V shift. Thus, one can conclude that device C has the most number of near interface traps as far as negative bias-stress is concerned (see Fig. 2 (c)). These threshold voltage shifts are caused by the capture of electrons and holes by traps in the oxide layer near the SiC/SiO_2 interface for positive and negative gate stresses respectively.

Fig. 3 illustrates the energy band diagrams when a bias-stress is applied on the gate. During a positive bias-stress, in Fig. 3 (a), electrons are injected into the near interface traps from the inversion layer in the conduction band via band-to-trap tunneling. This injection efficiency is determined by the tunneling probability and the barrier height as a function of time and electric field [10]. As time goes on from t_1 to t_3, carriers are injected into the deeper traps in the oxide. These trapped electrons increase the threshold voltage as shown in Fig. 2 (a) and (b). Under the negative bias-stress, there is an accumulation of holes in the valence band (see Fig. 3 (b)). These holes can tunnel into near interface traps and neutralize the negatively charged traps, thus resulting in negative shift in threshold voltage as shown in Fig. 3 (c). When the energy band diagrams are drawn to the scale, it is noted that the same near interface traps are charged and discharged under positive and negative bias stress. Considerable variance between devices from different vendors was observed implying that some vendors have been able to significantly reduce the near interface traps in the gate oxide.

B. Threshold voltage reduction at elevated temperatures

Threshold voltages are measured as a function of temperature. The temperature was ramped up from 25°C to 200°C where the devices were placed on a hot plate. Transfer characteristics (I_D-V_G) is measured with the constant drain voltage of 0.1 V using an Agilent 4145 parameter analyzer to

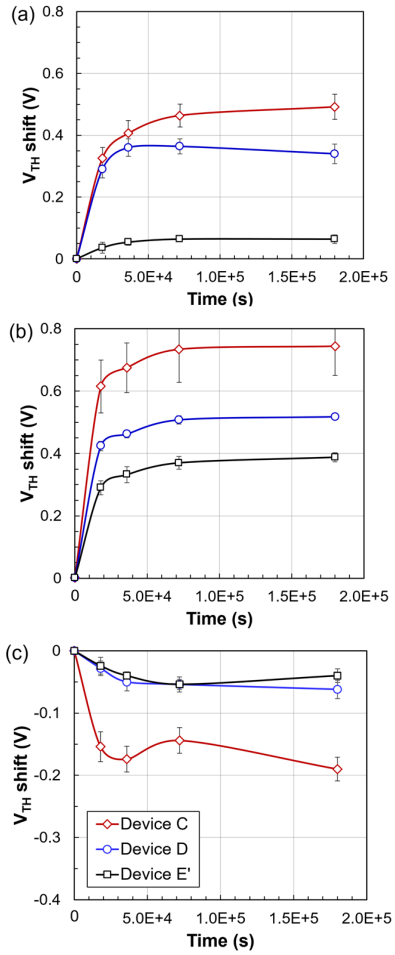

Fig. 2. Time-dependent threshold voltage shifts for (a) positive bias-stress of +20 V, (b) +30 V, and (c) negative bias-stress of -10 V for 50 hours.

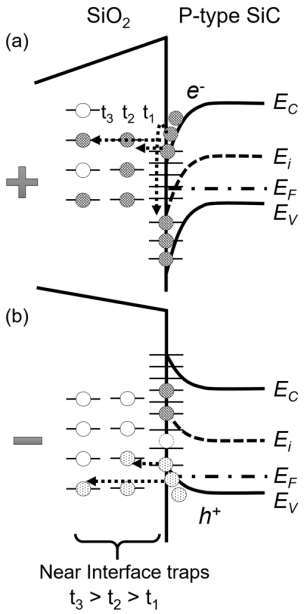

Fig. 3. Energy band diagram under (a) positive bias-stress and (b) negative bias-stress.

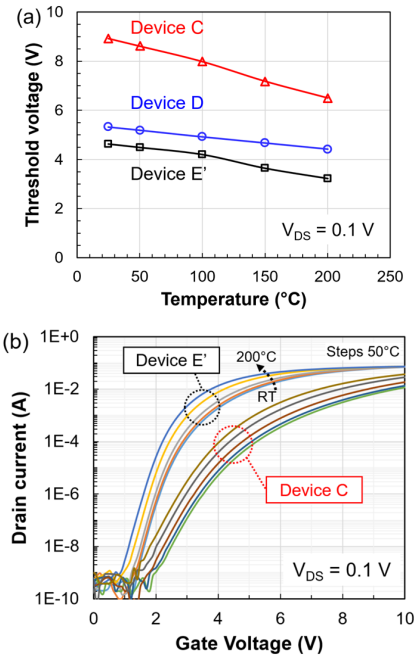

Fig. 4. Temperature-dependent (a) threshold voltage values and (b) I_D-V_G transfer characteristics of device E' and C.

determine the threshold voltage. Threshold voltage is extracted by the linear extrapolation (LE) method where the intercept of gate voltage is obtained by extrapolating from the maximum transconductance, g_m, point in that linear region [9].

As temperature increases, threshold voltages of all devices decrease. Device C shows the maximum threshold voltage reduction of about 2.5 V in negative direction whereas device D and E' show a reduction about 1 V at 200°C. The subthreshold characteristics for various devices are shown in Fig. 4 (b). It is clearly seen that the slope of curves in subthreshold region for device E' is much steeper than that of device C indicating device E' has lower interface state density than device C where the slope is gradual [11]. Device D is not shown in the figure but is located between the other two.

In a virgin device, there are a lot of positive charges in the oxide which are balanced by the negative charges in the interface states. When the device gets into strong inversion, these negative charges define the threshold voltage of the device. As temperature increases, electrons in the interface states get enough energy to emit out of the interface traps into the conduction band reducing the negative charge at the interface [12]. This contributes to the reduction in threshold voltage. Therefore, since device C has higher interface states density, it shows larger shift in threshold voltage (see Fig. 2 (b)).

C. Leakage current under high drain bias and temperature

Subthreshold *I-V* characteristics under the various bias conditions and temperature are shown in Fig. 5. Constant drain bias of 0.1 V is applied for pre-stress measurement. Higher drain bias of 600 V which is half of the rated voltage results in negative shifts of the subthreshold curves as shown with green lines (circle markers) in all devices. Shifts under high drain voltage are considered due to change in potential barrier within the channel region due to high electric field in the JFET region. In general, 1200 V SiC MOSFETs have high channel resistance, which takes up 65% of total on-resistance due to poor inversion layer mobility. In order to reduce channel resistance, channel length has been reduced to sub-micron dimensions to overcome high channel resistance. However, reduced channel length also lowers the potential barrier at the source as drain voltage increases. Consequently, lowered potential barrier allows carrier injection from the source [13]. Under high drain bias, device C shows the larger shift than other two as shown in Fig. 5 (a). Assuming the channel lengths are similar in all devices, it indicates device C gets higher potential at the junction between the channel and the JFET region when 600 V is applied to drain. At temperature of 150˚C, subthreshold curves are further shifted toward negative direction as shown in orange and red curves (triangle and diamond markers, respectively) in Fig. 5 (b) and (c) as discussed in experimental result B.

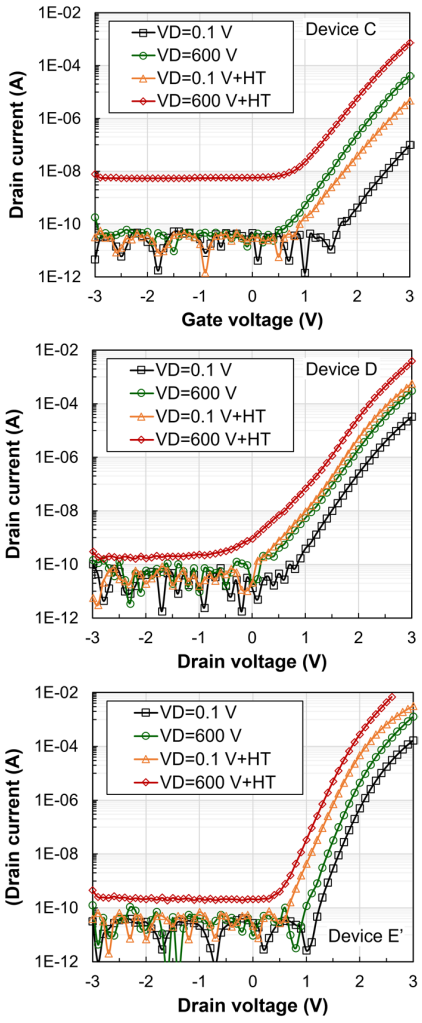

Fig. 5. Leakage current under various bias and temperature conditions (high drain voltage of 600 V and high temperature of 150˚C) in the devices from (a) vendor C, (b) vendor D, and (c) vendor E'.

As observed in Fig. 5, device C displays the highest shift in negative direction. The combination of elevated temperature with high drain bias accelerates the negative shift with increased leakage current. This increase in leakage current is only observed when high temperature and high drain bias are combined (see red curves with diamond markers in Fig. 5) signifying that the leakage current is coming from the depletion region in the drift layer. In case of device D (see Fig. 5 (b)), the threshold voltage and leakage current level are getting into dangerous territory, which can make the device normally on. The threshold voltage of device C is high enough even at elevated temperature, as shown in Fig. 4. This seems reliable in terms of leakage current in the off state. However, when high drain bias is applied at high temperature, the device is no longer in the safe region.

Difference in shifts indicates these devices are different not only in the oxide quality but also in the device design such as channel length, JFET length and management of electric field. Therefore, to avoid device failure, one can improve the oxide reliability by reducing near interface traps, interface state density and design the device to have higher threshold voltage.

D. Interface state density extraction

In most cases, the extraction of interface trap density requires a capacitance-voltage (*C-V*) measurement on capacitors which is not applicable to commercial devices. Therefore, the method which is solely based on the subthreshold *I-V* characteristics is used in this work [14]. Since all DUTs are commercial devices, the oxide thickness of 500 Å has been assumed.

Fig. 6 shows the calculated interface state densities as a function of energy. Trap density increases near the edge of the conduction band where the inversion is taking place. Therefore, carriers in the inversion layer would be trapped in the high trap density region reducing the number of carriers, and effective electron mobility will consequently be reduced. Device C shows the highest interface trap density of about $6x10^{12}$ /cm^2·eV while device D and E' show the similar trap density values of about $3x10^{12}$ /cm^2·eV near the conduction band edge. This is in good agreement with the result from higher threshold voltage shift at elevated temperature measurement in Fig. 4.

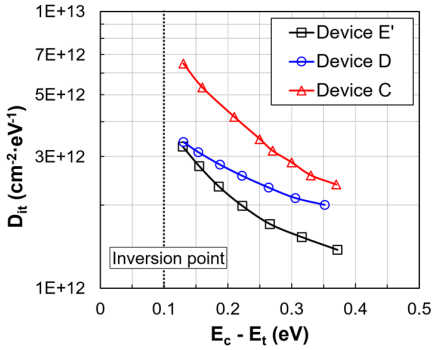

Fig. 6. Interface state density of device C, D, and E' as a function of energy level.

III. Conclusions

Threshold voltage instability under various stress conditions has been presented with commercial 4H-SiC MOSFETs from 3 vendors. Positive and negative bias DC stresses for 50 hours induced threshold voltage shift up to 0.74 V and -0.2 V, respectively in vendor C. Vendor E' showed the smallest shift implying that they have reduced near interface oxide traps effectively. Temperature-dependent threshold voltage measurements and interface trap density extraction showed consistent results. This indicates higher interface trap density results in larger threshold voltage shift due to emission of electrons from interface states at elevated temperature. Choosing a threshold voltage with safe margin consideration of trap density is important to prevent the device from becoming normally-on as discussed in experimental results. The variation of threshold voltage of devices with temperature, from device to device in the same family and shift under sustained DC stress (positive or negative) has implications for current sharing in parallel operation of multiple devices in a power module. The efforts to reduce interface and near interface trap density should continue. The vendor E' has achieved the best results, so far, in this respect.

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References

[1] J. A. Cooper, Jr. and A. K. Agarwal, "SiC power-switching devices—The second electronics revolution?," Proc. IEEE, vol. 90, no. 6, pp. 956-968, 2002.

[2] E. P. Eni, S. Beczkowski, S. Munk-Nielsen, T. Kerekes, R. Teodorescu, R. R. Juluri, B. Julsgaard, E. VanBrunt, B. Hull, S. Sabri, D. Grider, and C. Uhrenfeldt, "Short-circuit degradation of 10-kV 10-A SiC MOSFET," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9342-9354, 2017.

[3] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements," IEEE Trans. Electron Devices, vol. 55, no. 8, pp. 1835-1840, 2008.

[4] A. Agarwal, H. Fatima, S. Haney, and S.H. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs" IEEE Electron Device Lett. vol. 28, no. 7, pp. 587-589, 2007.

[5] A. K. Agarwal, S. Seshadri, L. B. Rowland, "Temperature dependence of Fowler-Nordheim current in 6H-and 4H-SiC MOS capacitors," IEEE Electron Device Lett., vol. 18, no. 12, pp. 592–594, 1997.

[6] A. K. Agarwal and S. Haney, "Some critical Materials and Processing Issues in SiC Power Devices," J. Electron. Mater., vol. 37, no. 5, pp. 646-654, 2008.

[7] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 316–323, 2015.

[8] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications. John Wiley & Sons, 2014.

[9] A. Ortiz-Conde, F. J. Garcia-Sanchez, J. Muci, A. T. Barrios, J. J. Liou, and C. S. Ho, "Revisiting MOSFET threshold voltage extraction methods," Microelectron. Reliab., vol. 53, no. 1, pp. 90-104, 2013.

[10] A. J. Lelis, D. B. Habersat, R. Green, and N. Goldsman, "Two-way tunneling model of oxide trap charging and discharging in SiC MOSFETs," Material Science Forum, vol. 717-720, pp. 465-468, 2012.

[11] R. Schörner, P. Friendriches, and D. Peters, "Detailed investigation of N-channel enhancement 6H-SiC MOSFETs," IEEE Trans. on Electron Devices, vol. 46, no. 3, pp. 533-541, 1999.

[12] S. Potbhare, N. Goldsman, G. Pennington, A.J. Lelis, and J. McGarrity, "Numerical and experimental characterization of 4H-silicon carbide lateral metal–oxide–semiconductor field-effect transistor," J. Appl. Phys., vol. 100, no. 4, pp. 044515, 2006.

[13] T. A. Fjeldly and M. Chur, "Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs," IEEE Trans. Electron Devices, vol. 40, no. 1, pp. 137-145, 1993.

[14] Y. A. Zheng, A. Softic, and M. H. White, "Characterization of interface traps in the subthreshold region of implanted 4H and 6H-SiC MOSFETs," Solid-State Electron., vol. 46, no. 10, pp. 1579-1582, 2002.