Bias Temperature Instability on SiC n- and p-MOSFETs for High Temperature CMOS Applications

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***Abstract*—The circuit functionalities of Complementary Metal-Oxide-Semiconductor (CMOS) devices on 4H-SiC for digital and analog circuit applications beyond 200˚C have been extensively studied, however, the reliability of the devices on SiC needs to be demonstrated due to the traps at/near the dielectric interface. In this report, the reliability of n- and p- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has been studied on three different gate oxide conditions – thick thermally grown, ultrathin thermal + thick CVD oxide and ultrathin thermal + thin CVD oxide in terms of their bias temperature instability (BTI) measurement. The MOSFETs were stressed at various constant bias voltages at 150˚C and up to 10^5s. The threshold voltage shift due to positive bias on n-MOSFET is <0.5V after 10^5s at +25Vwhile p-MOSFET shows a larger shift of -1.9V shift after 10^5s at -25V and 150˚C for ultrathin + thick CVD oxide. The report also establishes improvement in reliability of p-MOSFETs with ultrathin + CVD oxides over thermally grown oxides.**

***Index Terms*—CMOS, reliability, field-effect mobility, threshold voltage, transconductance**

I. INTRODUCTION

SiC has been well-established as a replacement of silicon at harsh conditions such as high field and high temperature due to its superior thermal, mechanical and electrical properties compared to silicon at those conditions [1], [2]. The ability to operate at cryogenic as well as elevated temperatures enables sensing applications such as temperature sensor, gas sensors, pressure sensors and other microelectromechanical systems (MEMS) at extreme environment [3]. As a wide bandgap semiconductor, SiC has the potential for high-power electronics due to high breakdown voltage, low on-resistance, high thermal conductivity and high radiation tolerance [4]. Both 4H and 6H polytypes have been widely used in high voltage DC-DC converters, aerospace industries, chargers for electronic vehicles and smart high-power home and industry appliances. Digital and analog circuits based on SiC CMOS can operate beyond 200˚C [5] where silicon devices have limited operations. Complex integrated circuit (IC) control electronics on SiC such as flipflops (FF), ring oscillators and operational amplifiers (Op Amp) have been demonstrated already at high temperature [5]–[7]. The ability to integrate lateral high voltage (HV) MOSFETs into ICs enables high voltage switching and controlling equipment at extreme conditions [8].

However, one of the major drawbacks of SiC MOSFETs is the density of traps (D_{it}) at/near the SiO_2/SiC interface[9], [10]. Even though thermal oxide can easily be grown on SiC unlike any other wide bandgap semiconductors, a strong increase of D_{it} close to the conduction band is observed due to the defects located at the oxide near the SiO_2/SiC interface. As the silicon carbide crystal is oxidized, carbon-based oxides form complex structures that do not diffuse out of the SiO_2 layer. To passivate the traps near the conduction band, nitridation via NO or N_2O has been common to SiC MOSFETs [11]–[13]. Recently, incorporation of high-K dielectrics and other deposited oxides has been proven to reduce the interface states and improve mobility [14]–[18].

Even though deposited oxides improve the device characteristics, their low conduction band offsets and poor band alignment with SiC substrate results in higher rate of injection [19]. Higher carrier-injection means capture of electrons/holes through traps and/or generation of traps. The issue becomes severe at elevated temperature since the trapping/de-trapping barrier lowers and raises reliability concerns e.g. threshold voltage shift [20], [21] and time dependent dielectric breakdown [22], [23]. The improvements in reliability and mitigations of instabilities have drawn significant interests lately. A. J. Lelis et al. [24] has reported on an in-depth

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understanding of threshold voltage instabilities. The transfer characteristics shift right and left with positive and negative bias stress even after 3 minutes of stress. R. Green et al. [25] observed threshold voltage instability in commercially-available power MOSFETs. A positive shift results in an increase in specific on-resistance while a negative shift increases the leakage current. The polarity of the bias also has an asymmetric effect. With positive bias stress, the threshold voltage of SiC n-MOSFETs exhibited small shifts whereas at negative bias stress, the n-MOSFETs exhibited much larger shifts [26], [27]. Passivation engineering of traps improves the interface states near the conduction band but does not sufficiently passivate traps near the valence band. As a result, there are improvements in the n-MOSFET reliability, where electron is the majority carrier, however the p-MOSFET reliability is still poor and needs to be addressed for potential high temperature CMOS applications. This work reports on performance and reliability studies of both n- and p-channel SiC MOSFETs with ultrathin thermal oxide followed by chemical vapor deposition (CVD) oxide. The results are compared to the standard thermally grown gate oxide.

II. Design and Fabrication Process

N- and P-channel lateral MOSFETs were fabricated on a 6-inch N-epi 4H-SiC Wafer at the Analog Devices Inc. (ADI) Hillview Fabrication facility. The implanted channel MOSFETs were fabricated using aluminium as p-species and nitrogen as n-species. The P-well doping was $2x10^{16}$ /cm^3 and the N-well doping was $4x10^{16}$ /cm^3. The source/drain junctions had $0.5x10^{19}$ /cm^3 doping concentration of the corresponding species. In this study, three separate gate oxide conditions are reported. Wafer 1 has thermally grown oxide with a target thickness of 50nm. Wafer 2 and Wafer 3 have ultrathin oxide formed by thermal oxidation followed by high-temperature chemical vapor deposition (CVD) oxides with a target thickness of 50 nm (Wafer 2) or 25 nm (Wafer 3). The grown or deposited oxides were annealed at 1250˚C in diluted N_2O for densification and nitridation of the interface. Wafer 3 has shorter duration of post deposition anneal (PDA) due to smaller thickness compared to thicker gate oxides (Wafer 1 and Wafer 2). The thermal oxide was subjected to a separate post oxidation anneal (POA) to better eliminate oxidation clusters due to carbon atoms prior to N_2O anneal. The gate oxide conditions, and their effective oxide thicknesses (EOTs) extracted from capacitance-voltage characteristics are listed in Table 1. A 0.5µm thick n-type polysilicon layer was deposited and patterned as the gate electrode contact for n- and p-MOSFETs. Ohmic contacts for the junctions were formed using 100 nm Nickel which was annealed at 750˚C for two minutes for silicide formation followed by another anneal at 965˚C for two minutes to improve the contact. A 1 µm thick interlayer dielectric was deposited, and a 500 nm thick aluminum was used as metal interconnect and contact pads. The cross section of the MOSFETs and a photo of the fabricated 6-inch Wafer (#1) are shown in Fig. 1. A detailed fabrication process can be found in [8].

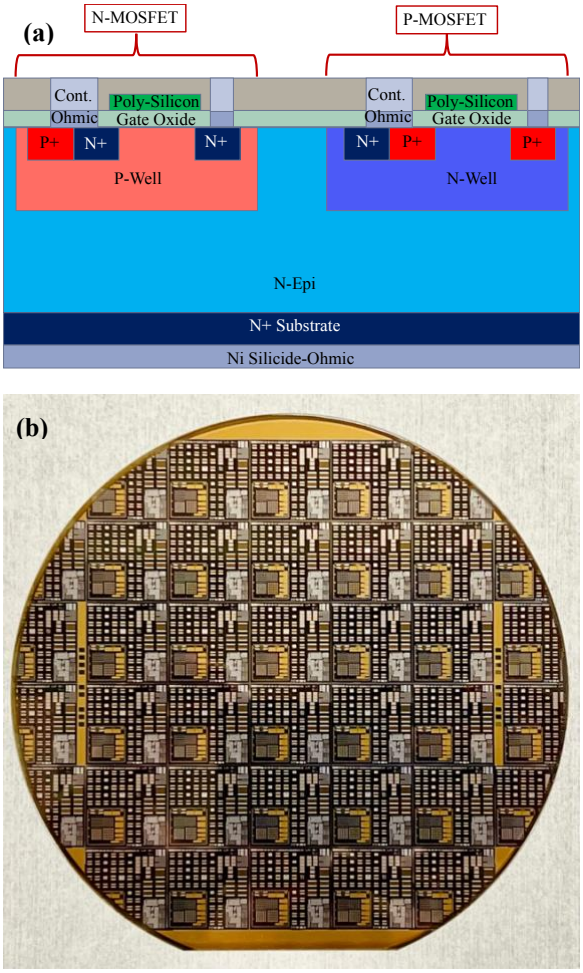

Figure 1. (a) The cross-sectional view of n- and p-MOSFET. Ni-Silicide was used as ohmic contact and 0.5µm aluminum was used as top metal interconnect. (b) A photo of 6" Wafer *with HV and LV n- and p-MOSFETs, capacitors, logic IC and test structures.*

Table 1. Gate oxide split plan for the three Wafers. EOT is the effective oxide thickness calculated from the capacitance-voltage characteristics.

Wafer ID	Thermal Oxidation	Ultra-thin Ox	HTO GOx	POA-1	POA-2	**EOT**
W1	40nm at 1175˚C	N	N	800˚C 3h	1250˚C diluted N_2O, 20% N_2, 3h	54 nm
W2	N	2nm	40nm	N	1250˚C diluted N_2O, 20% N_2, 3h	46.7 nm
W3	N	2nm	20nm	N	1250˚C diluted N_2O, 20% N_2, 1.5h	28.9 nm

III. Characterization Methodology

The Capacitance-Voltage (C–V) and current-voltage (I–V) measurement was done using HP 4284 LCR meter and a Keithley 4200SCS system, respectively. EOT was calculated using the formula EOT= ϵ_{ox}*A/C_{OX}, where C_{OX} is the oxide capacitance, A is the capacitor area and ϵ_{ox} is the electrical permittivity of SiO_2. Device parameters including EOT, flatband voltage, surface doping, and bulk potential were extracted using NCSU CVC program [28]. To extract the transfer characteristics, drain was biased at 0.1V and the source

and the substrate is at zero volt. Gate voltage was varied from zero to ±20V. All the devices have W/L = 1 (where, W = channel width, L = channel length) to accurately extract the mobility by minimizing a geometry effect. The field effect mobility was extracted using the following formula,

$$\mu_{FE,peak} = \frac{\max\left(\frac{\delta I_D}{\delta V_{GS}}\right)}{V_{DS} C'_{OX}}$$

Where, I_D is the drain current, V_{GS} is gate to source voltage, V_{DS} is drain to source voltage which is 0.1V throughout this work and C'_{OX} is the oxide capacitance per unit area (F/cm^2).

The device reliability is evaluated through bias temperature instability (BTI) measurement. To report BTI measurements, we adopted stress-sense-stress technique [25]. The threshold voltage was primarily extracted using the intercept of maximum slope via linear extrapolation from the transfer characteristics [29] at measurement temperature prior to applying any stress. At this threshold voltage, the current level was determined and used to extract threshold voltage using the current level method [30]. Each BTI measurement was conducted by selecting the current level using this method and extracting only the required portion of transfer characteristics near the selected current level to minimize the delay between two 'stress' steps.

A constant voltage stress was applied to the gate during the "stress" step. The electric field was extracted using the formula, $E = (V_{BIAS}-V_{TH})/t_{OX}$ instead of $E = V_{BIAS}/t_{OX}$ due to the fact that the applied voltage at the gate terminal is not essentially across the gate oxide. Rather, one part is used to provide the surface potential until the flatband of the metal oxide semiconductor (MOS) structure and the other part is across the dielectric [31]. The accurate gate oxide capacitance (C_{OX}) was extracted from capacitance-voltage characteristics of 100 x 100 µm MOS capacitor fabricated on N-epi layer. The transfer characteristics, leakage currents, PBTI and NBTI measurements were conducted on 30 x 30 µm (W/L = 1) n- and p-channel MOSFETs.

IV. Results and Discussions

Fig. 2 shows the transfer characteristics of n- and p-MOSFETs at room temperature. The peak field effect mobility for n-MOSFET was 21.8, 22.4 and 24.1 cm^2/Vs for Wafer 1, 2 and 3 respectively. On the other hand, for p-MOSFET, the mobility values are 7.5, 6.8 and 7.5 cm^2/Vs for Wafer 1, 2 and 3 respectively. The mobility is higher for ultrathin + CVD oxides compared to thermally grown oxide due to better interface states of ultrathin + CVD oxides. In addition, Wafer 3 has higher mobility than Wafer 2 possibly owing to shorter N_2O annealing which leads to less interfacial oxidation and C-related traps [9]. The improvement between Wafer 1 and Wafer 2 is small because the longer POA causes addition thermal oxidation [32]. The low mobility of p-MOSFET is due to the combination of heavier effective mass of hole than electron for SiC [33] and lack of passivation of traps near valence band which will be explained later. Also, due to low field-effect-mobility and use of only n-type polysilicon as the gate, the threshold voltage is higher for the p-MOSFET compared to n-MOSFET and will need further optimization for CMOS applications.

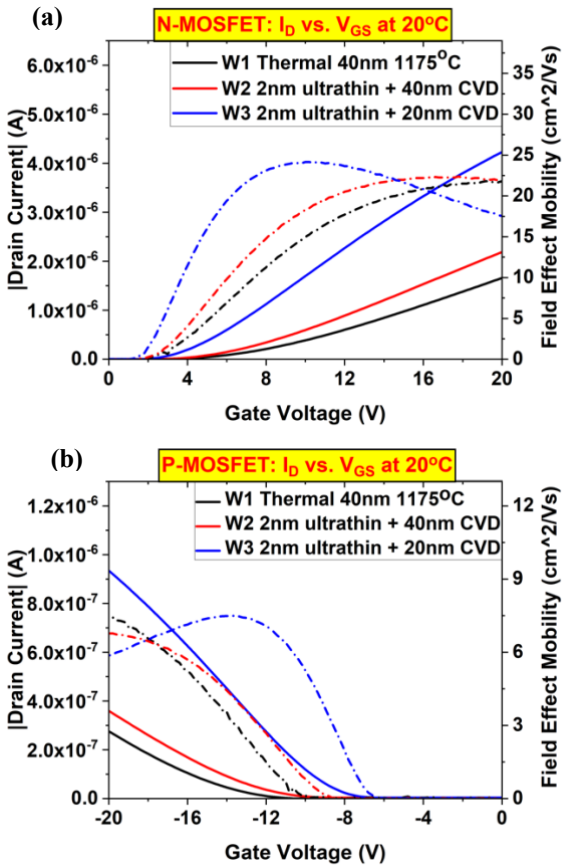

Figure 2. Room temperature transfer characteristics of (a) n-MOSFET and (b) p-MOSFET. The electrical oxide thickness is different from what shown in the figure since the POA/PDA have further oxidation that results in a different C_{OX}.

The transfer characteristics at elevated temperature (150˚C) are shown in Fig. 3. The mobility increases to 25~27 cm^2/Vs for n-MOSFET and 8~9 cm^2/Vs for p-MOSFET. The threshold voltage decreases in magnitude for both n- and p-channel MOSFETs at elevated temperatures due to more available carriers in the channel at that temperature. The increase in mobility and decrease in threshold voltage for both n- and p-MOSFET indicates that the mobility is coulombic scattering limited. It is also observed that the thinner dielectric (Wafer 3) has smaller threshold voltage since threshold voltage is directly proportional to the dielectric thickness [31].

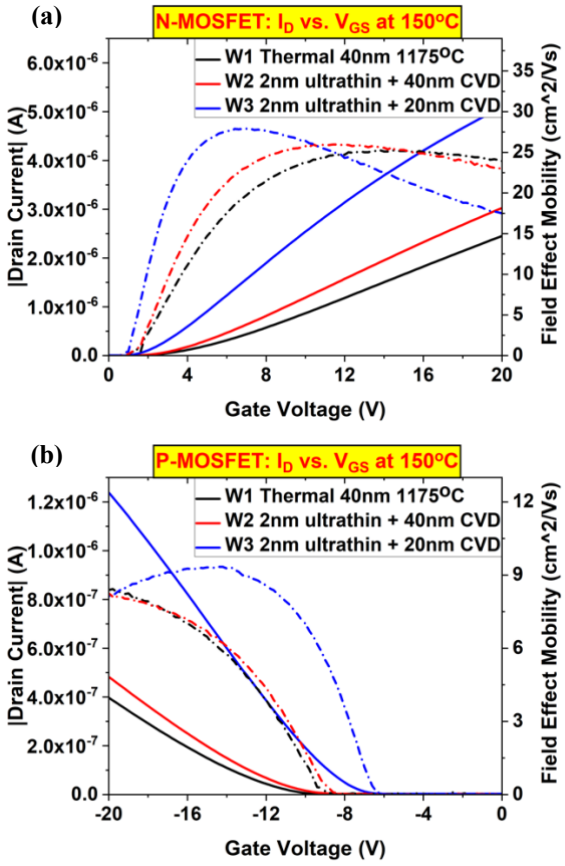

Figure 3. Transfer characteristics of (a) n-MOSFET and (b) p-MOSFET at 150˚C. At elevated temperature, there is more carrier available for conduction and the current increases. Both n-and p-MOSFET mobility increases with temperature indicating coulombic scattering limited mobility.

Fig. 4 shows the gate leakage characteristics measured at 150˚C for n- and p-MOSFETs. For this measurement, source, drain, and substrate terminals were tied together and kept at zero bias while a voltage was applied to the gate. Voltages applied to the gate were translated to corresponding electric field using the definition from Section III. The breakdown field of n-MOSFETs occurs 10.2 MV/cm for thermal oxide (W1) and 11.6 MV/cm for ultrathin thermal + CVD oxides (W2 and W3). The p-MOSFETs have slightly lower breakdown field, likely due to traps near the valance band. Ultrathin + CVD oxides have higher breakdown fields than thermal oxide due to higher C-related traps and defects during thermal oxidation [34]. It is important to note that the p-MOSFET leakage currents start to increase at approximately -2 MV/cm for thermal oxide and at -3 MV/cm (Wafer 2) and 2.8 MV/cm (Wafer 3) for ultrathin + CVD oxides while the n-MOSFET leakage currents start increasing above 5 MV/cm.

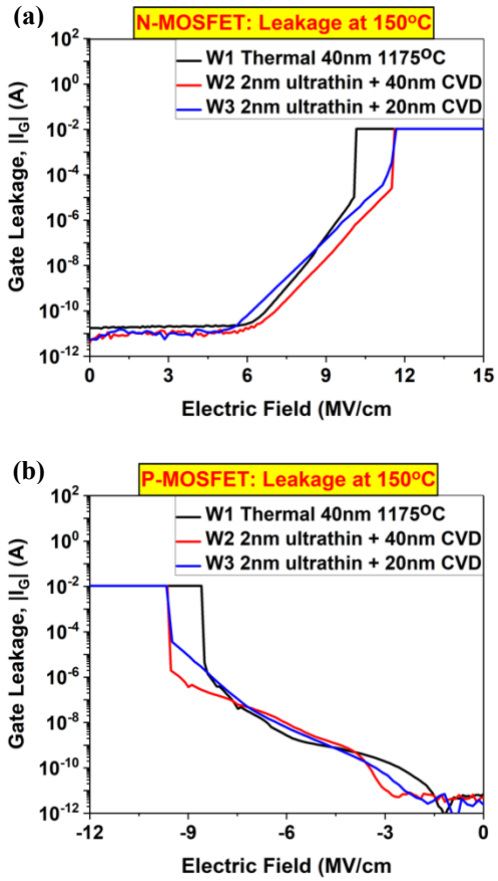

Figure 4. Gate oxide leakage currents vs applied electric field for (a) n-MOSFET and (b) p-MOSFET. Ultrathin + CVD oxides have higher breakdown field than thermal oxides.

Positive bias temperature instabilities (PBTI) of n-MOSFETs on three Wafers are illustrated in Fig. 5. All three Wafers show similar behavior under +4 MV/cm stress. The shift in threshold voltage was linear in log(time) scale and less than 0.5 V after 100,000 seconds at 150˚C. It is noted that the applied voltage was set to +13.56 V to achieve an effective oxide electric field of +4 MV/cm for wafer 3 as it has thinner oxide thickness compared to Wafer 1 and Wafer 2. The linear change in threshold voltage with time in log scale is attributed to the charging of as-processed oxide traps located at/near interface states. Since the shift in V_{TH} did not lead to additional permanent trap creation [35] the stressed devices recovered to the initial value within two days from the removal of the stress. The leakage current is below 10^{-10} A at +4 MV/cm in the time-zero leakage current plot shown in Fig. 4(a) for all three wafers.

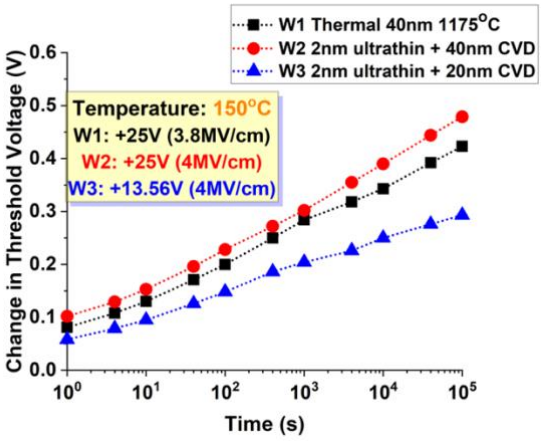

Figure 5. PBTI on n-MOSFETs with +4 MV/cm stress at 150˚C. Wafer *3 has the least shift in threshold voltage (+0.29V) and* Wafer *2 has the most (+0.48 V). As* Wafer *1 has thicker EOT, +25 V gives slightly lower effective electric field and has lower shift (+0.423 V)* compared to Wafer 2.

Fig. 6 shows the PBTI on n-MOSFET at +25V stress. As Wafer 3 has a thinner EOT, this voltage results in +7.8 MV/cm of an effective electric field across the dielectric. From Fig. 4(a), +7.8 MV/cm falls within the Fowler-Nordheim (FN) tunneling region [36]. Due to the large injection of charges into the dielectric via FN tunneling when stressed, a second slope was observed after $4x10^3$ seconds. We define the slope in PBTI characteristics as $d(\partial V_{TH})/d(\log_{10}t)$. The first and the second slopes are defined before and after $4x10^3$ seconds respectively. The 2nd slope is 1.44 while the 1st slope is 0.11 for Wafer 3 at +25V stress. PBTI on the thinner EOT n-MOSFET with two slopes did not recover even after two months whereas others recovered within two days. This suggests generation of traps during stress applied in BTI measurements.

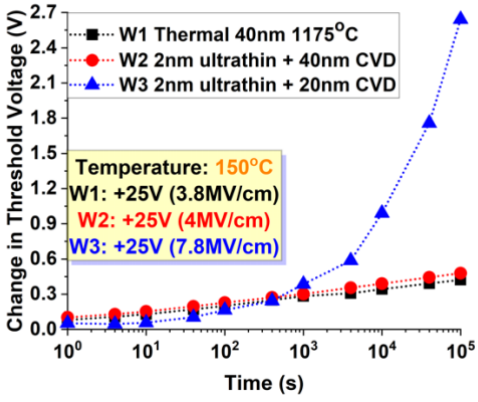

Figure 6. PBTI on n-MOSFETs with +25 stress at 150˚C. Wafer *3 has thinner EOT resulting 7.8MV/cm effective electric field and operating in FN tunneling region. The MOSFET on* Wafer *3 did not recover after two months of relaxation.*

Negative bias temperature instabilities (NBTI) on p-MOSFETs are reported in Fig. 7. The p-MOSFETs on different Wafers were stressed at -25V for Wafer 1 and Wafer 2, and at -16.52V for Wafer 3. The shift in threshold voltage is much higher for NBTI as the devices were stressed near high injection region (Fig. 4(b)). Larger shift (-3.219V) was observed for Wafer 1 at -2.3 MV/cm (-25V) compared to Wafer 2 (-1.9V at -2.7 MV/cm) and Wafer 3 (-1.52V at -2.7 MV/cm). All three curves show two slopes, and they did not recover after two days as it did for n-MOSFETs. The two slopes originate from high injection and the high injection comes from a combination of FN tunneling and trap-assisted tunneling (TAT). Thermal oxide shows the worst NBTI characteristics because the device is already operating at high injection region as it appears in the leakage current characteristics (Fig. 4). Even though the negative BTI on p-MOSFETs of Wafer 2 and 3 operates below the FN tunneling dominant region, they have 2nd slope. To investigate this, we vary the electric field stress. As the ultrathin + CVD oxides perform better than thermal oxides, we focus on further BTI measurements on Wafer 2 and 3 only.

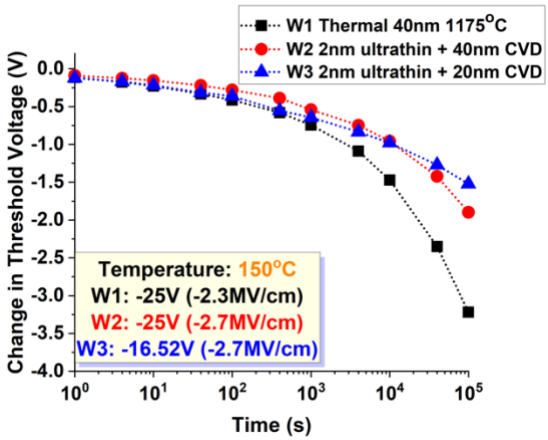

Figure 7. NBTI on p-MOSFETs with -2.3 and -2.7MV/cm stress at 150˚C. p-MOSFETs on all three Wafers *show two slopes and they do not recover. Thermal oxide has higher slope and higher shift in threshold voltage compared to ultrathin + CVD oxides.*

Fig. 8 shows NBTI on p-MOSFETs of Wafer 2 and Wafer 3 at different electric field stresses. As the stress was reduced in magnitude from -2.7MV/cm to -1.4MV/cm, the secondary slope reduced from -0.82 to -0.33. As we move further away from high injection region, there is still a second slope. It is evident that while the interface passivation technique used with N_2O was able to passivate the traps near the conduction band, it was not able to fully passivate the traps near the valence band. Hence, the stress applied for 100,000 seconds not only keep filling the existing traps but also create new traps by injecting charges through TAT and the secondary slope persists. During relaxation, there is -0.11V shift in threshold voltage after three days for -1.4MV/cm while the device stressed at -2.7MV/cm had -1V shift in threshold voltage after two months. Wafer 3 was stressed with -16.523, -19 and -25V, for 100,000 seconds as shown in Fig. 8(b). As the bias was increasing, the 1st slope was also increasing as the devices were pushed further into FN injection region. The 1st slopes are -0.176, -0.316 and -0.35 while the 2nd slopes are -0.49, -1.5 and -3.94 for -16.523, -19 and -25V respectively. Device stressed with -16.523 recovered completely after seven days, device stressed with -19 had -0.178V shift after three weeks and the device stressed with -25V failed during measurement.

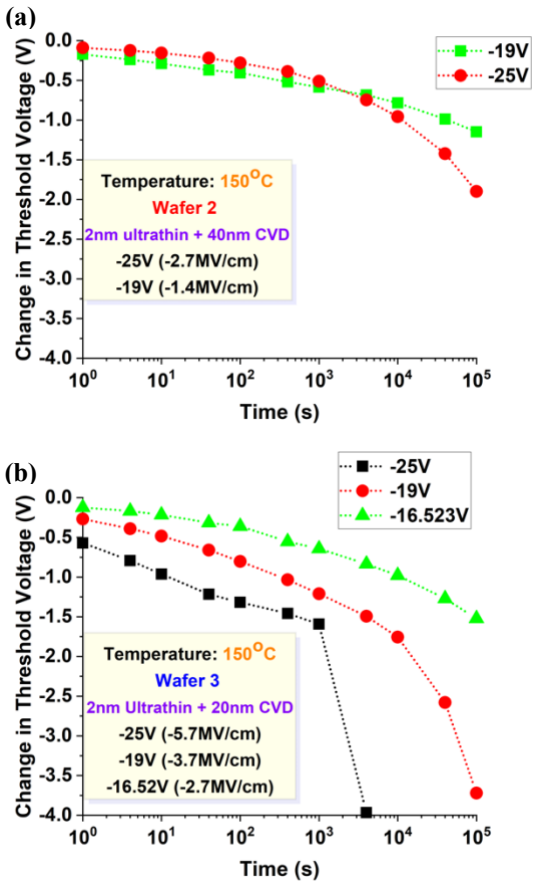

Figure 8. (a) NBTI of p-MOSFETs on Wafer *2 at 150˚C. The devices were stressed with -2.7 and -1.4MV/cm. The 2nd slope reduced from -0.82 to -0.33. (b) NBTI of p-MOSFETs on* Wafer *3 at 150˚C. The devices were stressed at -2.7, -3.7 and -5.7MV/cm for 100,000 seconds. At -5.7 MV/cm, the device destructively broke at some point between 4000 and 10,000 seconds.*

From the results, it is clear that all NBTI measurements (both n-MOSFETs and p-MOSFETs) have two slopes. The second slope can be lowered if the applied electric field stress is reduced but it is still present. Even at reduced stress there is a second slope. A hypothesis is presented in Fig. 9 to realize the reason for the two slopes. The constant bias stress (V_{GS}) is varied from 1 to 6 arbitrary units (a.u.). At lower bias, the charge injection is lower and hence the slope is small. As V_{GS} is increased, the slope of the threshold voltage change vs log(time) also increases. At V_{GS} = 5 a.u. there is generation of traps as the stress field is increased and FN tunneling starts. The new rate of injection is a combination of TAT and FN tunneling and this gives a further increase in the slope. As FN tunneling process creates more traps, the BTI stress becomes harder to recover. In addition, at an elevated temperature (150˚C) there are more carriers available for capture and the trapping/de-trapping barrier is lowered [37]. As the negative bias stress is applied, the positive charges pile up near the SiO_2/SiC interface which results in a negative shift in threshold voltage. Hole capture continues with time and hence the threshold voltage keeps increasing. As the applied voltage is further increased in magnitude, there is a generation of traps as well as more positive charges at a higher voltage. The second slope is from a two-fold effect with the combination of trap-assisted injection and further creation of traps via FN injection [38], [39]. The 2nd slope exists at lower electric field stress because the charges from TAT can build up an internal electric field resulting in more injection. This eventually leads to a second slope.

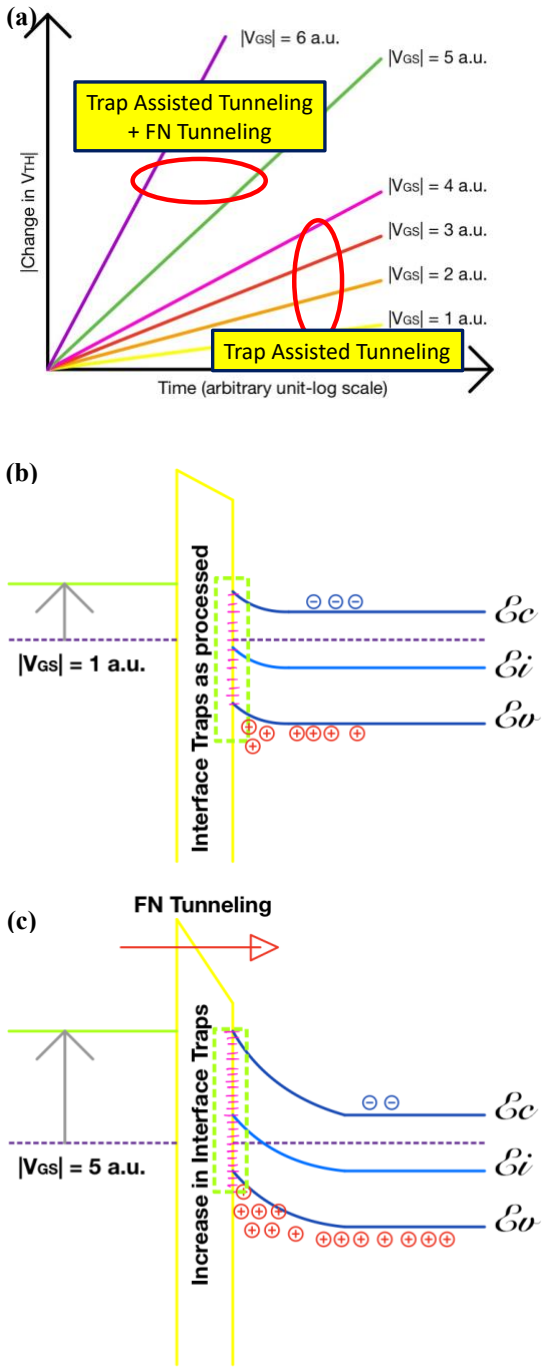

Figure 9. (a) the voltage stress is increasing by 1 arbitrary unit in magnitude. As the stress is applied, the change in threshold voltage increase linearly with time in log scale continuous injection through trap assisted tunneling. When the applied voltage stress increases to 5 a.u. the change in threshold voltage gets a higher slope as the trap assisted tunneling is reinforced with FN tunneling and creation of new traps. (b) The band diagram of n-type MOS structure as in p-

MOSFET. (c) *Change in band diagram* and increase in the number of traps *with increasing* negative *bias for p-type semiconductor MOS capacitor.*

Fig. 10 shows the NBTI on n-MOSFET and PBTI on p-MOSFET for the completion of CMOS reliability. The PBTI on p-MOSFET shows excellent stability; +0.169V and +0.083 shift in threshold voltage for Wafer 2 and Wafer 3 respectively after 100,000 seconds of 4.88MV/cm stress at 150˚C. On the other hand, NBTI on n-MOSFET shows -0.97V and -1.189V shift in threshold voltage for Wafer 2 and Wafer 3 respectively after 100,000 seconds of -3.21MV/cm stress at 150˚C. It is clearly observed that the NBTI has a high shift in threshold voltage compared to the PBTI regardless of n-channel or p-channel MOSFET. As a result, we conclude that the high shift is due to the lack of interface passivation near the valance band of the SiC substrate. At negative bias, holes are accumulated near the valence band while at positive bias, electrons are accumulated near the conduction band. N_2O and N_2 annealing performed during POA/PDA steps only passivate the traps near conduction band and the valence band passivation is incomplete. Thus, NBTI on both n- and p-MOSFET shows high shift in threshold voltage due to a high probability of interface traps assisted tunneling.

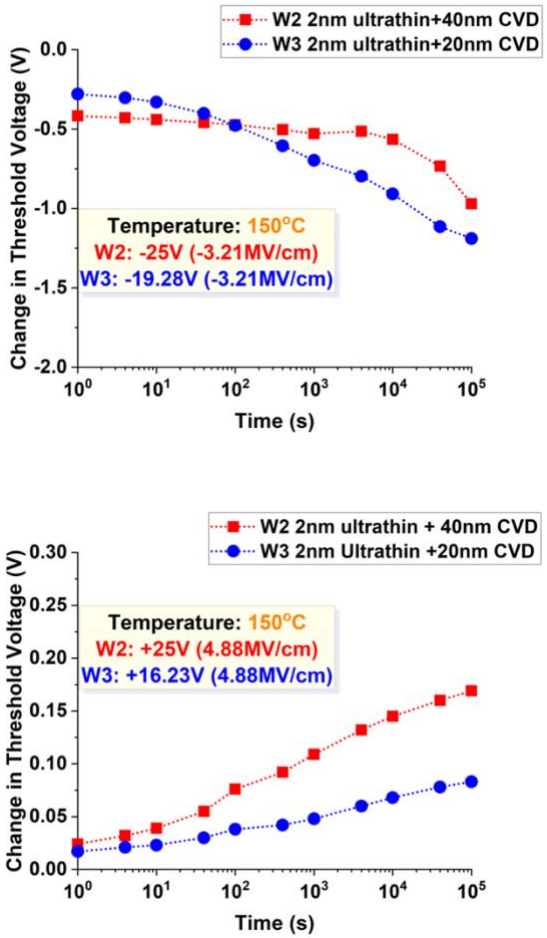

Figure 10. (a) NBTI on n-MOSFET. The large shift in threshold voltage (-0.97V for Wafer *2 and -1.189V for* Wafer *3) is due to lack of traps passivation such as oxygen vacancy. (b) PBTI on p-MOSFET. The curve shows excellent passivation of interface states near conduction band for p-MOSFET.*

V. Conclusion

This work illustrates the BTI characteristics for potential high-temperature SiC CMOS applications. Excellent PBTI on n- and p-channel MOSFETs for both thermal and ultrathin + CVD oxides has been demonstrated. PBTI on p-MOSFETs with deposited oxides are better even at higher electric field stress compared to n-MOSFETs due to less available carrier at the n-type substrate during positive applied stress. However, the NBTI characteristics suggest that the passivation of traps near the valence band is insufficient and separate post-oxidation annealing is needed. There is a significant decrease in traps near valence band of the pMOSFETs with ultrathin + CVD oxides as compared to thermal oxides as the NBTI shifts are lower for the deposited oxides.

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