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Critical Design Considerations for Static and Dynamic Performances on 6.5 kV 4H-SiC MOSFETs Fabricated in a 6-inch SiC Foundry

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***Abstract* — 6.5 kV-rated 4H-SiC MOSFETs have been successfully fabricated and demonstrated on 60 µm-thick, 1.2×10^{15} cm^{-3} doped N-type epi-layer on 6-inch, 4H-SiC N+ substrates. Devices were fabricated at the 6-inch SiC foundry, X-FAB, TX, USA. Active and edge termination areas of high voltage (>3.3 kV) SiC devices require critical design consideration due to implant straggles from the low background doping concentration. Despite the fabrication and design challenges, we have demonstrated $R_{on,sp}$ of 47 mΩ-cm^2 with a breakdown voltage of 7.9 kV with a very low leakage current using ring-based edge termination structure. Devices were then diced and packaged in a SUNY Poly's custom-made package to evaluate short circuit capabilities. Short circuit withstand time of 6.2 µs was recorded from the nominal device, along with 7 µs and 13 µs from the device with narrower JFET width and wider channel length, respectively.**

Keywords* — *Silicon Carbide, 4H-SiC, MOSFET, Breakdown Voltage, High Voltage, Edge Termination, Implant Straggle, Fabrication, 6-inch Foundry, Package, Short Circuit Capability

I. Introduction

Due to the high critical electric field and low intrinsic carrier density of 4H-Silicon Carbide (SiC), SiC has become a more prominent material to build high voltage devices than conventional silicon material. The merit of using 4H-SiC becomes more substantial when building a high voltage power device (>3.3 kV) due to the dominance of drift resistance contribution to total on-resistance of the high voltage power device, as the drift region must be made thicker and lighter doped [1]. The development of 6.5 kV SiC power devices is imperative in advancing and revolutionizing present and future high-power applications [2]. However, in-depth research and analysis in 6.5 kV power MOSFETs are lacking in previous literature [3-5].

Due to the low background doping concentration of a drift region in high voltage devices, implant straggles are more prominent than low voltage (~1.2 kV) power devices. As a result, active cell and edge termination require critical design considerations to avoid channel pinching in the JFET region and unwanted connection of P+ rings in the edge termination area [6, 7]. SiC MOSFETs with various cell designs and edge termination structures have been fabricated to 1) optimize the cell architecture overcoming the pinching issue and 2) demonstrate the dynamic/ruggedness performances of the fabricated 6.5 kV SiC MOSFETs.

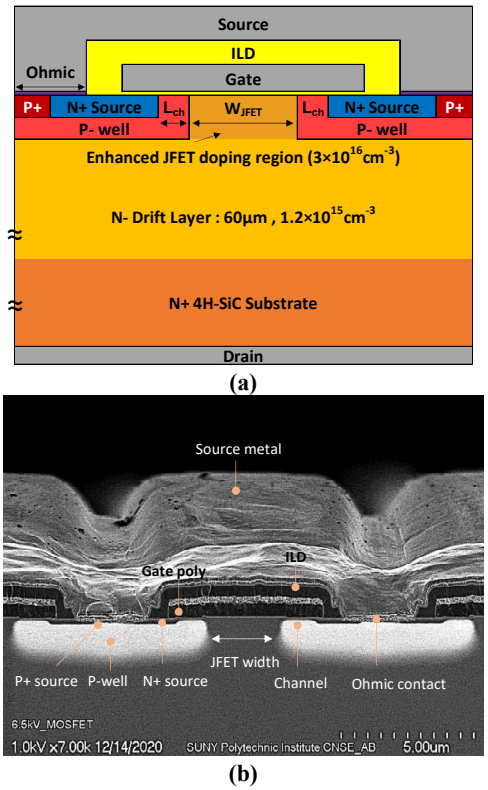

Fig. 1. (a) Schematic and (b) SEM cross-sectional view of the fabricated 6.5 kV 4H-SiC MOSFET.

II. Device Structure and Fabrication Technology

Fig. 1 shows a schematic cross-sectional view of the 6.5 kV SiC MOSFET. Critical design parameters are labeled in the

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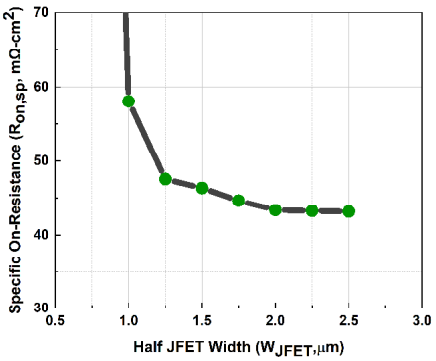
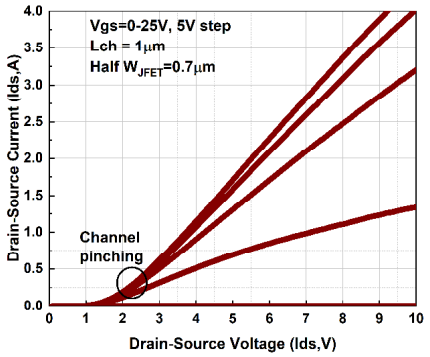


(a)



(b)

Fig. 2 (a) Extracted specfic on-resistane from small test MOSFET structures with various JFET width split. (b) Indication of the pinched channel in the JFET region due to the narrow JFET width. The half W_{JFET} is 0.7 μm in this design.

figures. The proposed MOSFETs were fabricated in a 6-inch wafer foundry company, X-FAB, TX, USA. A 60 μm thick drift layer with an N- epi doping concentration of about 1.2×10^{15} cm^{-3} on a 6-inch, N+ 4H-SiC substrate was used to fabrication 6.5 kV 4H-SiC MOSFETs. A detailed fabrication process flow can be found in [8]. Fig. 1 (b) shows a cross-sectional SEM image of the fabricated 6.5 kV SiC MOSFET.

III. High Voltage Device Design, Fabrication, and Experimental Results

A. Design Considerations For On-State Characteristics

Optimization of the active cell structure, especially JFET width (W_{JFET}) is critical for high voltage devices to ensure that the straggle from the P-well does not pinch the current path in the JFET region [6-7]. JFET widths were varied on small test MOSFET structures to find the optimum design for the 6.5 kV MOSFETs. Extracted specific on-resistance ($R_{on,sp}$) as a function of half W_{JFET} is shown in Fig. 2 (a). It is observed that half W_{JFET} needs to be at least 1 μm to have a reasonable $R_{on,sp}$ value. As shown in Fig. 2 (b), when the half W_{JFET} is 0.7 μm, the output characteristics of the fabricated 6.5 kV MOSFET supports that the channel in the JFET region is pinched due to narrow JFET width design. Conversely, a half W_{JFET} of 0.7 μm is a sufficient width to open the JFET region in the case of 1.2 kV MOSFET.

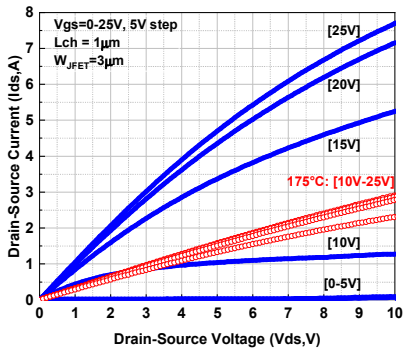


Fig. 3. SEM cross-sectional view of the fabricated 6.5 kV 4H-SiC MOSFET.

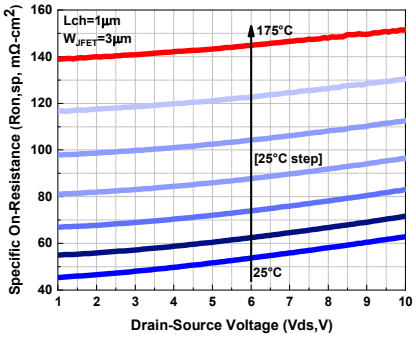


Fig. 4. Extracted specific on-resistance aa function of V_{ds} with varying temperatures at V_{gs} of 20 V.

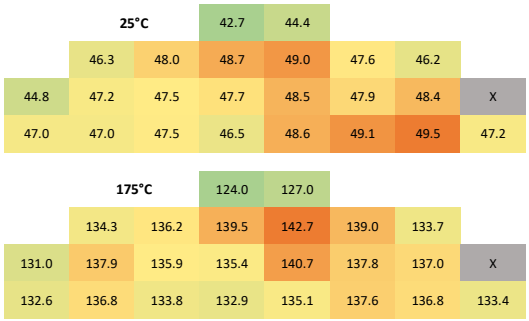


Fig. 5. Half wafer map of extracted $R_{on,sp}$ of 6.5 kV MOSFETs on a 6-inch wafer at 25 °C and 175 °C.

Table I. Edge Termination Design for 6.5 kV SiC MOSFETs

Design	Hyb65	Ra100	Hyb100	FFR100
S_o (μm)	2	1		0.8
S_i (μm)	1	0.75		0.03
W_{ring} (μm)	3			
# of ring	10	18		100
W_{JTE} (μm)	180	360		N/A
# of JTE zone	18	N/A	36	
alpha	1.04		1.02	
Total width (μm)	360	360	720	528

In order to ensure the opening of the JFET region in the high voltage devices, optimization of JFET width and doping concentration need to be carefully considered due to the low

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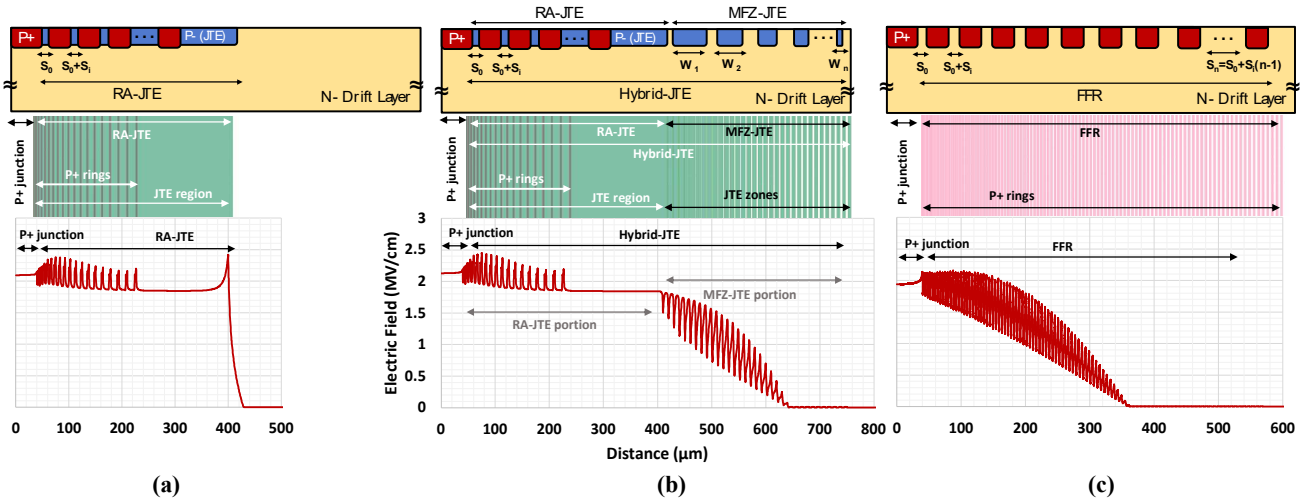

Fig. 6. Cross-sectional and topological layout image of the (a) RA-JTE, (b) Hybrid-JTE, and (c) FFR edge termination structures for 6.5 kV MOSFETs. Simulated electric field distributions are also shown at breakdown conditon.

background doping concentration of the drift region. The JFET doping concentration, along with W_{JFET} needs to be optimized to avoid the electric field crowding at the gate oxide below 3-4 MV/cm, where concentrated electric fields above 4 MV/cm can degrade the blocking behaviors. Detailed optimization of the JFET region can be found in [9]. In this study, the JFET doping concentration was designed to be 3×10^{16} cm^{-3}. As noted earlier, the half W_{JFET} needs to be at least 1 μm and a half W_{JFET} of 1.5 μm was chosen to be an optimum design.

The typical, on-wafer output characteristics of the fabricated 6.5 kV SiC MOSFETs measured at 25 ºC and 175 ºC are presented in Fig. 3. The demonstrated device has a full JFET width of 3 μm, a channel length of 1 μm, and a total cell pitch of 10.2 μm. The size of the active area is 4.5 mm^2. Fig. 4 shows extracted specific on-resistance ($R_{on,sp}$) at a gate-source voltage (V_{gs}) of 20 V as a function of drain-source voltage (V_{ds}) at elevated junction temperatures. As observed, $R_{on,sp}$ of the device increases with temperatures due to an increase of drift layer resistance. $R_{on,sp}$ variation across the wafer is also exhibited in Fig. 5. The average $R_{on,sp}$ at a gate-source voltage (V_{gs}) of 20 V from the half-wafer map at 25 °C and 175 °C are 47.2 mΩ-cm^2 and 132.2 mΩ-cm^2, respectively.

B. Design Considerations For Blocking-Mode of Operation

In order to warrant the use of 4H-SiC in high voltage-rating devices, the design of efficient edge termination structures is essential to manage the electric field crowding at the edge of the devices; thereby, achieving a specified breakdown voltage for a given drift layer design. Four edge terminations structures, Hybrid-JTE65 (nominal design), RA-JTE100 (slightly over-designed), Hybrid-JTE100 (slightly over-designed), and P+ floating field rings (FFR) were designed and fabricated [10]-[11]. The summary of 6.5 kV SiC edge termination technology is shown in Table I.

Cross-sectional views, topological layout views, and simulated electric field distributions are exhibited in Fig. 6. The optimization procedure of JTE and ring-based edge termination structures were previously discussed in [6, 10, 11].

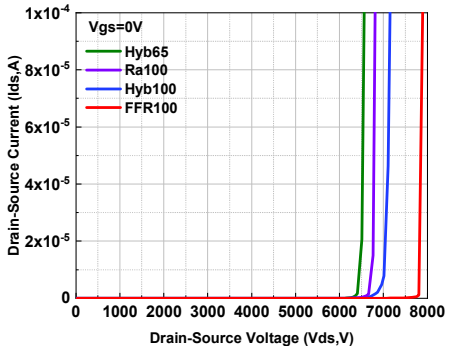

Fig. 7. Measured forward blocking characteristics of the 6.5 kV MOSFET. 7.9 kV was achieved with Hyb100.

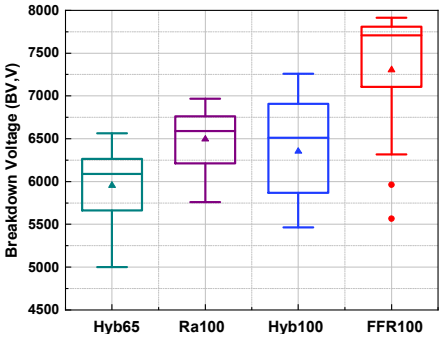

Fig. 8. Box-plot distribution of the measured breakdown voltage using various edge termination design. Breakdown voltages were extracted at I_{ds} of 100 μA.

Due to the low background doping concentration, straggles from P+ implant also need to be considered when designing edge termination structures to avoid unwanted connection of P+ rings, otherwise, the concentric rings will act as an extension of the P+ main junction [6, 12].

The breakdown voltage of 6.5 kV power devices was measured using SUNY Poly's custom-built ultra-high-voltage probe station that consists of >20 kV power supply, Keithley dual-channel Source Measuring Units (SMUs), and Signatone manual probe station. Devices were then submerged in a non-

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conductive dielectric liquid, Fluorinert FC-40, to prevent arcing during the high voltage measurement.

Measured forward blocking capabilities of the 6.5 kV SiC MOSFETs with different edge termination structures are shown in Fig. 7. All edge termination designs demonstrated extremely low leakage currents with blocking voltages of 6.6 kV (Hyb65), 7 kV (RA100), 7.2 kV (Hyb100), and 7.9 kV (FFR) at a drain-source (I_{ds}) current of 100 µA, respectively. A near-ideal breakdown voltage of 7.9 kV was achieved with an FFR edge termination design. It is presented that the JTE-based edge termination design shows a somewhat lower breakdown voltage than the FFR structure. This could be attributed to the unwanted connection of some P+rings, which results in altered spacing between rings in the JTE-based structure. On the other hand, the FFR structure has many P+ concentric rings to more evenly distribute the electric field, despite a couple of unwanted connection between some rings that merely serves as an extension of the main junction. Fig. 8 shows box-plot distributions of measured and extracted breakdown voltages across the whole 6-inch wafer. From the box-plot distribution, it is seen that the breakdown voltage varies significantly, which could be due to the non-uniform doping concentration that may cause more implant straggles of P+ concentric rings.

C. Design Variation and Short Circuit Capabilities

The MOSFETs with 1) a channel length of 2 µm (MOS2) and 2) JFET width of 2 µm (MOS3) were also fabricated in the same mask to evaluate short circuit capabilities of various 6.5 kV MOSFET designs. On-wafer, typical output characteristics of the fabricated MOS2 and MOS3 are shown in Fig. 9. Average $R_{on,sp}$ of the MOS2 and MOS3 are 55 mΩ-cm^2 and 57 mΩ-cm^2 (compared to 47 mΩ-cm^2 from MOS1). MOS2 has a 16% larger $R_{on,sp}$ due to increased channel length and thus cell pitch (10.2 µm vs 12.2 µm – MOS1:MOS2). MOS3 also shows 18% increased $R_{on,sp}$ when compared to MOS1, despite having a smaller cell pitch (10.2 µm vs 9.2 µm – MOS1:MOS3). This is due to slight pinching of JFET width that narrows the current path as discussed earlier. Box-plot distribution of $R_{on,sp}$ (extracted at Vgs = 20 V, 25 °C) with MOSFET design variations across the wafer are shown in Fig. 10. It is important to note that all devices have the same active area of 4.5 mm^2.

6.5 kV MOSFETs were diced and packaged in SUNY Poly's custom-made high-voltage packages to evaluate short circuit performances. Image and the details of the high-voltage custom package are shown in Fig. 11. Fig. 12 shows successfully measured short circuit capabilities of the packaged 6.5 kV MOSFETs. The short circuit withstands time on $L_{ch}1W_{JFET}3$ (MOS1), $L_{ch}2W_{JFET}3$ (MOS2), and $L_{ch}1W_{JFET}2$ (MOS3) MOSFETs are 6.2 µs, 13 µs, and 7 µs, respectively. The MOSFET with a channel length of 2 µm demonstrated the longest short circuit withstand time (approximately 2.2 times longer than MOS1) due to lower saturation current as shown in Fig. 12. On the other hand, MOS3 showed a slight improvement in short circuit time than MOS1, despite having higher on-resistance from the narrow JFET width. It is interesting to note that the current level in MOS3 (green) is higher than MOS1 (blue) although a significant difference in $R_{on,sp}$ was observed (see Fig. 10). This could be attributed to higher channel density in MOS3 due to the smaller cell pitch (10.2 µm vs 9.2 µm – MOS1:MOS3). Enhanced short circuit

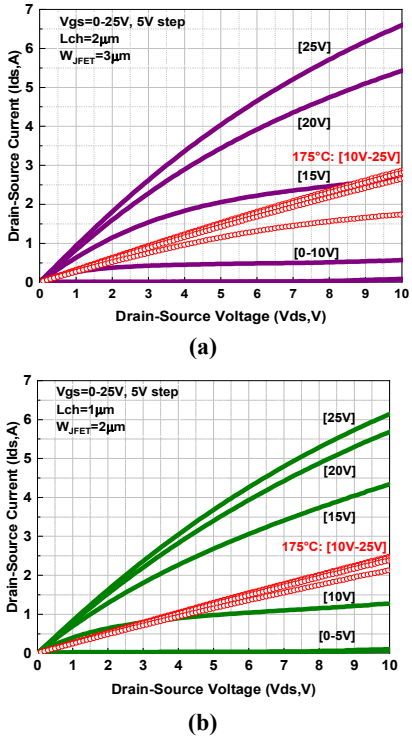

Fig. 9. Output characteristics of the 6.5 kV MOSFET with (a) a channel length of 2 µm and (b) JFET width (W_{JFET}) of 2 µm.

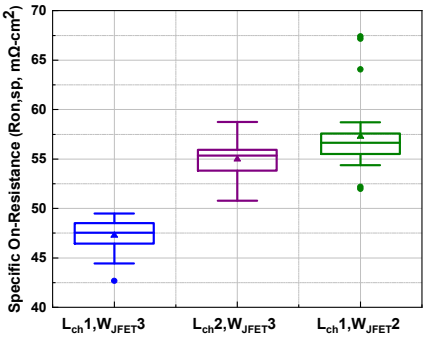

Fig. 10. Box plot distribution of $R_{on,sp}$ with MOSFET design variations. $R_{on,sp}$ extracted at V_{gs} of 20 V, room temperature.

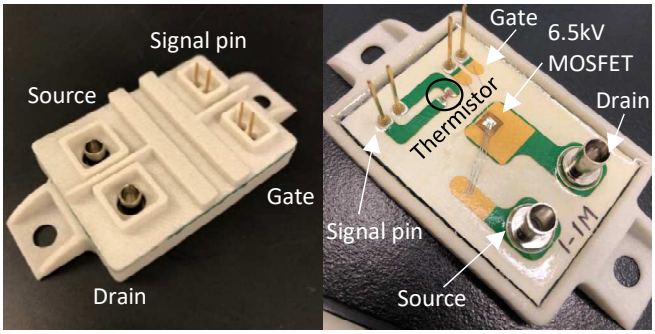

Fig. 11. Image of the fabricated 6.5 kV MOSFET in SUNY custom-made high-votlage package. Important parts are labelled.

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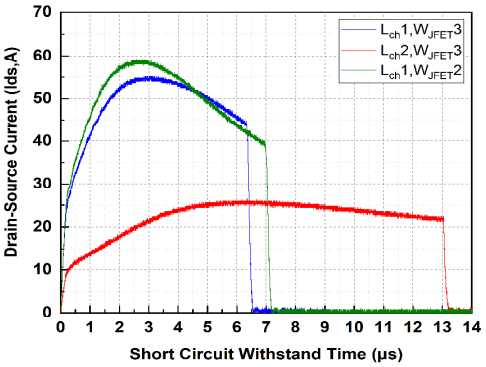

Fig. 12. Measured short circuit withstand time on 6.5 kV MOSFETs after packaging on SUNY in-house package. Short circuit withstand times of $L_{ch}1W_{JFET}3$ (MOS1), $L_{ch}2W_{JFET}3$ (MOS2), and $L_{ch}1W_{JFET}2$ (MOS3) MOSFETs are 6.2 µs, 13 µs, and 7 µs, respectively.

time from MOS3 is also due to enhanced shielding on gate oxide from the narrow JFET width [13].

CONCLUSION

4H-SiC 6.5 kV MOSFETs were successfully fabricated at a 6-inch SiC foundry, X-FAB, TX, USA. Design considerations for both forward and blocking characteristics were discussed to overcome potential issues when fabricating high voltage SiC MOSFETs. It is critical to take the straggle of P-type dopants into considerations when designing 6.5 kV power MOSFETs and their edge termination structure due to the low background doping concentration of the drift layer. Fabricated 6.5 kV MOSFETs successfully demonstrated both static (forward and blocking-mode) and dynamic characteristics.

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