Current Saturation Characteristics and Single-Pulse Short-Circuit Tests of Commercial SiC MOSFETs

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***Abstract*—This paper focuses on the short circuit (SC) tests of four commercial TO-247 packaged silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) with voltage ratings of 900 V and 1200 V at room temperature. The test results of the SiC devices are compared with that of super junction silicon (Si) MOSFETs which underwent identical test procedures. The current saturation characteristics were tested at over 50% of their rated voltages with 1-µs turn-on pulses. The test results show that the SiC MOSFETs can sustain much higher power density during short circuit conditions relative to their Si counterparts. However, there are several challenges in sustaining a 10-µs SC time without significant degradation or failure with the drain-to-source voltage set at half of the rated voltage and the gate set to the full rated voltage.**

Keywords—Silicon carbide (SiC), MOSFETs, short circuit, saturation current, failure mechanisms

I. INTRODUCTION

Silicon carbide (SiC) devices have great potential for high voltage, high power density and high frequency applications due to their higher bandgap energy, breakdown field, and thermal conductivity [1]. In recent years, SiC power MOSFETs have shown remarkable performance in a wide range of applications including modular multilevel converter (MMC) based high power motor drives [2], high efficiency photovoltaic harvesting systems [3], and high power density inverters for electric vehicles (EV) [4]. Since SiC MOSFETs are becoming increasingly available from several commercial venders, the reliability and ruggedness of these devices are becoming major considerations for market acceptance.

During normal operation, industry and transportation applications require switching devices to sustain over-current events at high drain-to-source voltages with full rated voltages applied to their gates for short periods. Certain applications such as automotive inverters for hybrid or electric vehicles demand longer sustaining times due to stall or frequent climb events. During over-currents caused by short circuit faults, conventional desaturation protection circuits for Si insulated-gate bipolar transistors (IGBTs) are able to protect them within 10 µs [5]. It is desirable for commercial SiC devices to have this 10-µs SC sustaining capability, similar to their silicon counterparts, should such a fault occur. Therefore, it is necessary to characterize the devices' SC withstand capability, their degradation, and any SC induced failure mechanisms.

This paper reports on saturation current measurements and SC test results of five commercial MOSFETs as shown in Table I. High saturation current density at high drain bias will result in reduction of the SC time due to increased heat dissipation. The heat generation on a per unit die area for SiC devices under SC conditions is much higher than for Si devices due to the smaller die area of SiC devices with similar on resistance. It should be noted that the SC condition for 10 µs to 15 µs is largely an adiabatic event where the heat is stored in the die, raising its temperature, and does not have adequate time to dissipate through the package and heatsink.

TABLE I. TESTED DEVICES

Device	Material	Voltage Rating	Current Rating	Approximate Die Size
A	Si	900 V	About 5 A	7.85 mm²
B	SiC	900 V	10-15 A	1.89 mm²
C	SiC	1200 V	10-15 A	3.85 mm²
D	SiC	1200 V	10-15 A	3.96 mm²
E	SiC	1200 V	About 30 A	8.48 mm²

Fig. 1 shows the circuit used for both the saturation current and short circuit tests. The power source is a 1500 V dc power supply. Three 100-µF film dc link capacitors are charged through the 5-kΩ current limiting resistor and discharged by the 66-kΩ bleeder resistor. A 2.5-µF decoupling capacitor with low equivalent serial inductance (ESL) and resistance (ESR) is placed near the device under test (DUT) to help support high transient energy. In order to measure the I_{ds}, a series of 30 MHz Rogowski coils with measurement ranges from 30 A to 600 A are used. V_{ds} is measured with a 1500-V differential probe and V_{gs} is measured with a high bandwidth passive probe. The gate driver outputs a 1-µs single gate pulse for the saturation current measurements, and up to a 10-µs single gate pulse for the short circuit tests. A 2-minutes interval between adjacent pulses is used in order to fully cool down the device.

II. TEST RESULTS AND DISCUSSION

A. Saturation Current Measurement Results

Fig. 2 shows the 1-µs pulse test waveforms for the 1200-V SiC MOSFET (E) and 900-V Si MOSFET (A). Due to high heat dissipation, the temperature of the die rises during the 1-µs pulse. Initially the device current increases due to the increase of inversion layer electron mobility with temperature [6], and then reduces due to the net reduction in inversion layer and

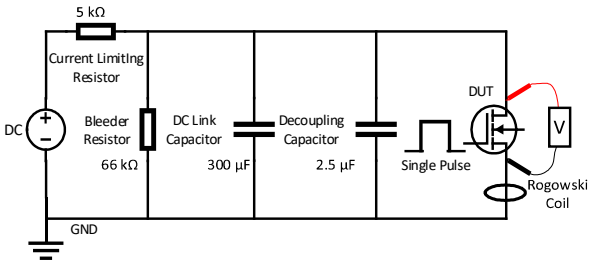


Fig. 1. Circuit for both saturation and short circuit tests.

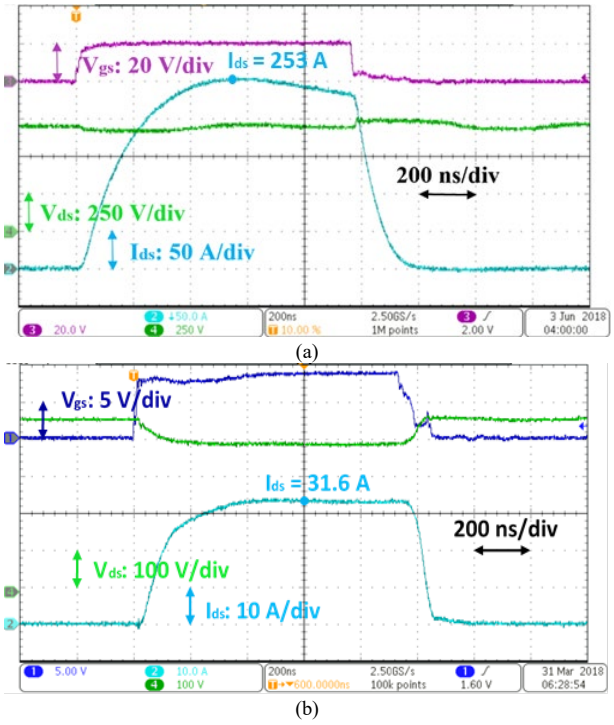


Fig. 2. The devices' switching waveforms with 1-µs gate voltage pulse at room temperature. (a) The 1200-V SiC MOSFET (E) with V_{gs} = 20 V and V_{ds} = 675 V. (b) The 900-V Si MOSFET (A) with V_{gs} = 9 V and V_{ds} = 400 V. Current limiting resistors are used for case (b).

bulk electron mobilities at higher temperatures. The saturation current value is extracted at the peak current point during the 1-µs turn-on period (as shown in Fig. 2(a)). A similar phenomenon is not observed in the 900-V Si super junction MOSFET (Fig. 2 (b)) since its electron mobility in the inversion layer, as well as in the bulk, reduces monotonically with temperature. Fig. 3 shows the first quadrant I-V curves measured with a 1-µs gate pulse for each of the five devices. The Si MOSFET shows a tendency for uncontrollable saturation current when V_{ds} is higher than 400 V as shown in Fig. 3 (a) for all three samples tested. The potential mechanism for this may be related to the parasitic npn bipolar junction transistor (BJT) in the Si MOSFET. The SiC MOSFETs tested do not display this phenomenon, possibly due to the fact that the implanted npn parasitic BJT in SiC has a current gain less than unity due to ion-implant damage caused by p and n implants [7]. Among the SiC devices, the C and D

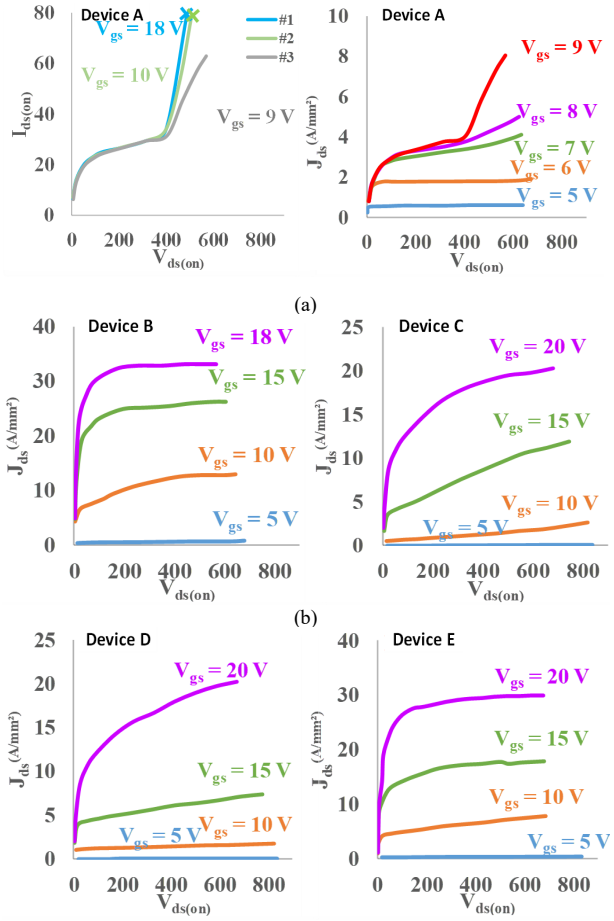


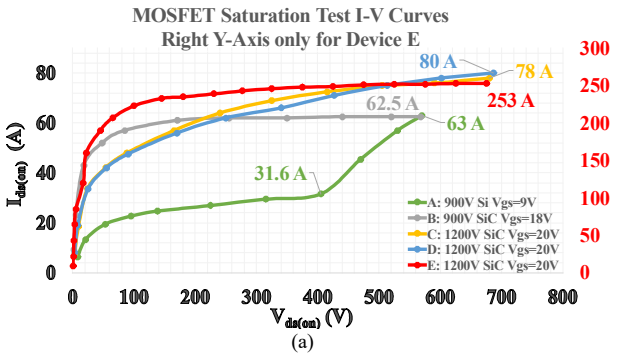
Fig. 3. 1st-quadrant output current density curves. (a) left: Si Device A with three test samples, which show the tendency of over current saturation events when V_{ds} > 400 V right: 900-V Si Device A; (b) left: 900-V Device B; right: 1200-V Device C. (c) left: 1200-V Device D; right: 1200-V Device E.

devices display the output conductance increasing with V_{ds} in the saturation region possibly due to their very short channel lengths. Device B was only measured up to V_{gs} = 18 V as recommended in its data sheet.

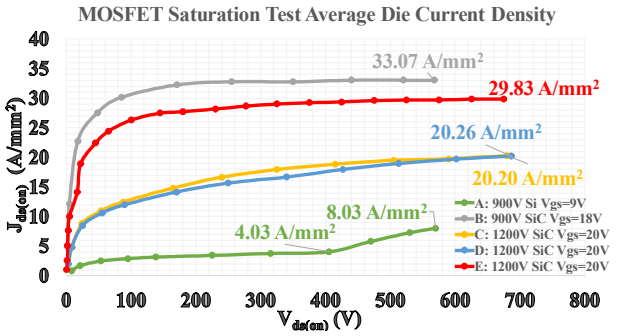
Fig. 4 (a) compares the I_{ds}-V_{ds} characteristics of all the devices when fully turned on. The results are also converted into current density vs. V_{ds}, as shown in Fig. 4 (b). Fig. 4 (b) indicates that the SiC MOSFETs display much higher current densities in the saturation region as compared to the Si MOSFET due to their much lower specific on-resistance. According to Fig. 4 (b), SiC devices B and E should have the highest heat dissipation per unit area under short-circuit conditions followed by devices C and D. The Si MOSFET should have the least amount of heat generated per unit area under a short-circuit and therefore should have the longest SC time.

B. *Short Circuit Test Results*

Fig. 5 shows the short circuit waveforms for the 1200-V SiC device D at V_{ds} = 600 V. The current rises as the temperature increases due to improvement of inversion layer electron



(a)



(b)

Fig. 4. 1st-quadrant I-V curves comparisons with full rated gate voltages: (a) Drain-to-source current vs. voltage (b) Drain-to-source die current density vs. voltage.

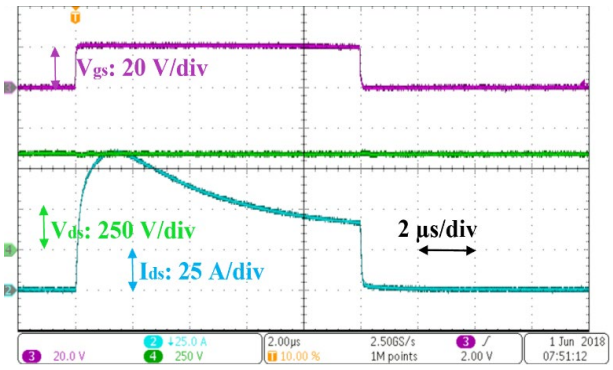
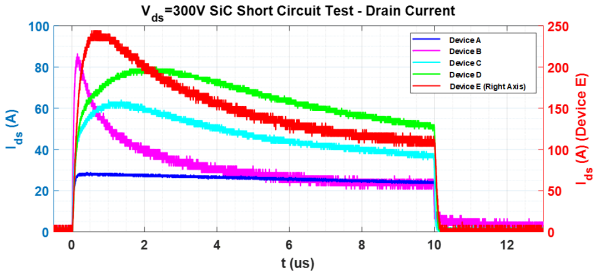
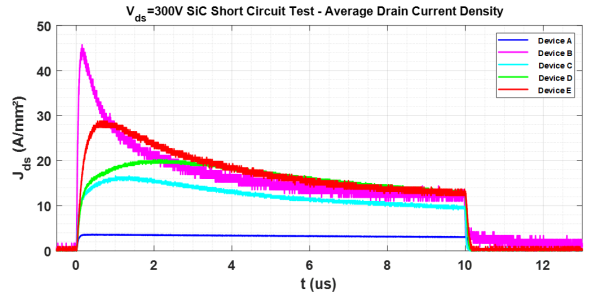


Fig. 5. 1200-V Device D: Short circuit test waveforms with 10-µs gate pulse at 600-V V_{ds} and 20-V V_{gs} at room temperature.

mobility and then reduces at higher temperatures due to the net reduction of the drift and inversion layers' electron mobilities. The integral of the product of V_{ds} and I_{ds} during the 10-µs gate pulse determines the total heat generated in the device. With increasing internal temperature, the device can ultimately be damaged due to melting of contacts, delamination of various layers or the detachment of the chip itself as well as various other destruction processes. Therefore, the short circuit time depends not only on the total heat generated and subsequent temperature rise but also on the processing of the chip and the choice of various metals and dielectrics. Fig. 6 compares drain currents and current densities during the transient short circuit period when V_{ds} is 300 V. Fig. 6 (b) contains information regarding the behavior of the inversion layer electron mobility



(a)



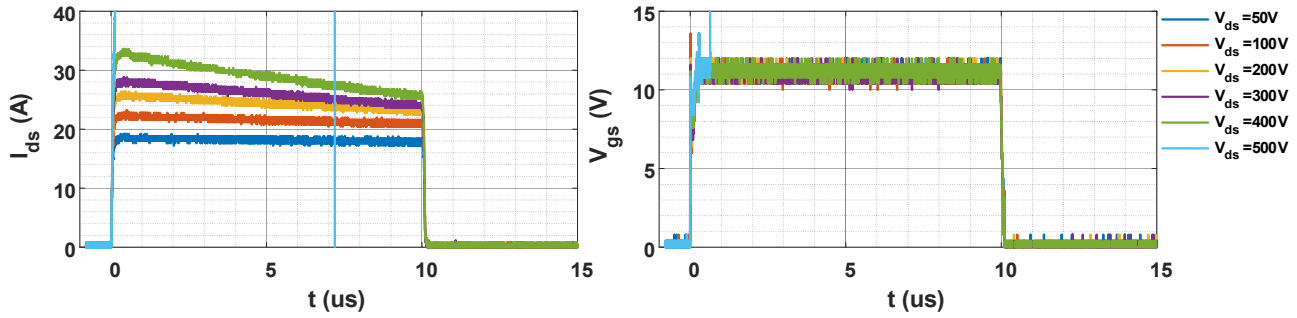
(b)

Fig. 6. Short circuit results comparisons at 300-V Vds. (a) Drain-to-source current during short circuit (b) Current density during short circuit.

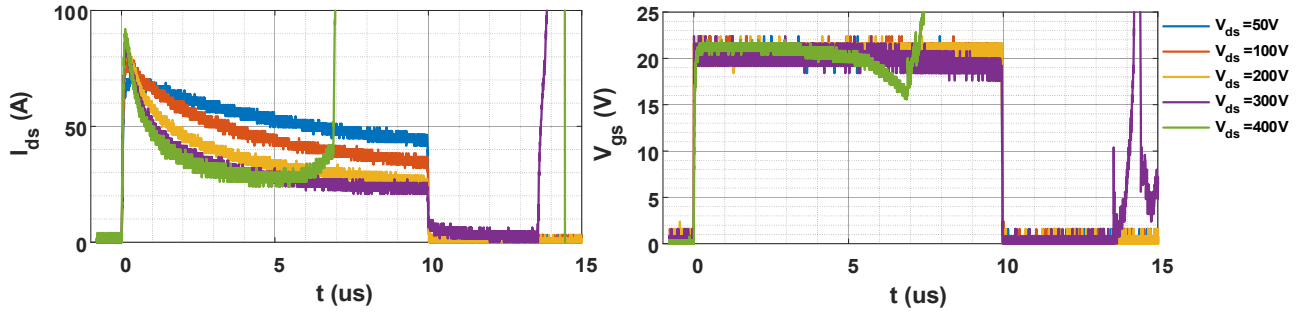
with temperature for each of the four SiC devices and the ratio of the channel resistance to the total resistance. The Si MOSFET does not display a current overshoot because the inversion mobility reduces monotonically with temperature and also due to the fact that the channel resistance is a much smaller part of the total resistance. Devices B and E seem to have the maximum heat dissipation integrated over 10 µs followed by devices D, C and A. However, as we will see, only device D survives up to 600 V.

Three of the five devices' drain current and gate voltage waveforms are plotted in Fig. 7. Measurements were done at different values of drain voltage, V_{ds}, while applying the full rated gate voltage, V_{gs}. The silicon device survived up to V_{ds} = 400 V and failed at 500 V possibly due to the turn-on of the parasitic npn BJT. Device B developed a gate-short at a high drain voltage as evidenced by a dip in the V_{gs} waveform. Device D was the only one to survive up to 10 µs at V_{ds} = 600 V. Table Ⅱ summaries the test results of the five devices. The second column shows the five devices' largest likely sustaining voltages without a failure with up to a 10-µs pulse. The third column shows the average die power density at 300 V V_{ds} during the 10-µs pulse. This was calculated by integrating curves in Fig. 6 (b) over 10 µs, dividing by 10 µs and then multiplying by 300 V. The average power density during the short-circuit measurements is between 3.71 to 5.30 kW/mm^2 (discounting the Si device) which is significantly higher than what is observed during nominal operation. This explains why the temperature rise is much higher in SiC devices compared to silicon during a short-circuit event. Assuming similar dielectrics and overlay metals are used in both Si and SiC devices, it is understandable that SiC devices would have much shorter SC times as compared to Si devices.

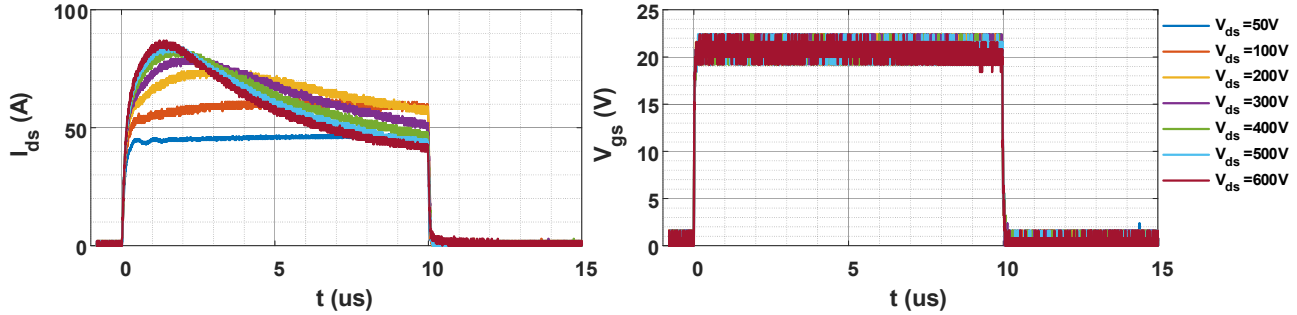
The 900-V SiC Device B and 1200-V SiC Device E show higher power dissipation in Fig. 6 (b). It is possible that the



(a) Device A: 900-V Si device short circuit test results (left: drain-to-source current, right: gate voltage)



(b) Device B: 900-V SiC device short circuit test results (left: drain-to-source current, right: gate voltage)



(c) Device D: 1200-V SiC device short circuit test results (left: drain-to-source current, right: gate voltage)

Fig.7 Short circuit tests results including I_{ds}, and V_{gs} waveforms with different drain-source voltages for device A, B, and D.

TABLE II. SHORT CIRCUIT TEST RESULTS

Device	Max 10-µs SC Sustaining Voltage	Average Die Power Density (kW/mm^2) at 300 V V_{ds} over 10 µs
A: 900 V Si	400 V to 500 V	0.99
B: 900 V SiC	Around 300 V	5.14
C: 1200 V SiC	Around 400 V	3.71
D: 1200 V SiC	Over 600 V	4.90
E: 1200 V SiC	500 V to 600 V	5.30

vender adopted thinner gate oxide and/or a lighter doped P well, which results in lower threshold voltages. The thinner gate oxide may lead to reduced gate reliability. According to Fig. 7 (b), the gate voltages dropped noticeably due to gate leakage current when the V_{ds} as well as die temperature were relatively high. This kind of gate degradation may weaken the device's short circuit reliability and can result in device failure [8].

Static measurements before and after the short circuit tests reveal degradation of the 1200-V SiC device D which are shown in Fig. 8. The threshold voltage increased and the output conductance decreased. The output current reduction could be caused by the rise of the threshold voltage possibly due to interface trap creation or electron injection into the gate oxide during the short circuit events. Moreover, the unclamped inductive switching (UIS) avalanche test result (Fig. 9) shows a very high effective drain-to-source breakdown voltage (about 2600 V). Therefore, it is highly possible that device D was designed with a thicker drift layer, which helps with the heat capacity during adiabatic events such as a short circuit.

III. CONCLUSION

The I-V curves with a 1-µs gate pulse were measured in the devices' saturation region for five target devices. Meanwhile, single-pulse short circuit ruggedness of each was evaluated. Based on the saturation current measurement results, it was found that the targeted commercial SiC MOSFETs did not show premature breakdown compared with the tested Si MOSFET even with five to eight times the Si device's die current density

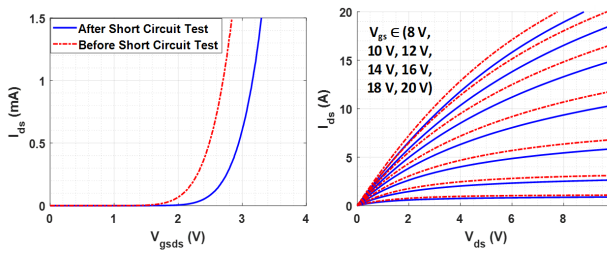


Fig. 8. 1200-V device D degradations (left: threshold voltage, right: 1st-quadrant I-V curves). The static characteristics were measured after 2 days of the short circuit test shown in Fig. 7 (c).

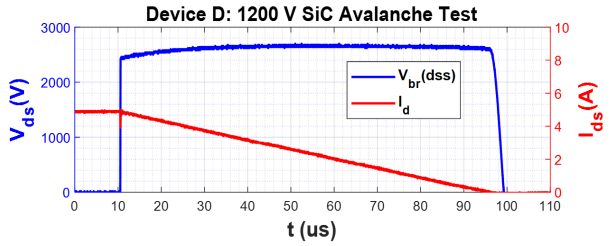


Fig. 9. Avalanche breakdown waveform of the 1200-V device D. The effective drain-source breakdown voltage is near 2600 V.

in the saturation region. This indicates that the parasitic npn BJT is effectively suppressed in SiC MOSFETs mainly due to implantation damage in the P-base layer [7].

For the 10-µs short circuit test, the results indicate that, the SiC devices did not show remarkable withstand capability compared with the super junction Si device. It can be inferred that none of the commercial SiC devices could sustain a 10-µs short circuit time at two thirds of the rated drain-source voltage without apparent degradation or failure. Clearly, redesign of those devices is needed to improve the short-circuit time if warranted by the applications.

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