Defects in 4H-SiC epilayers affecting device yield and reliability

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***Abstract*— Forty nine silicon carbide 150 mm wafers from three commercial vendors to be used for fabricating MOSFETs were examined by UVPL imaging to count their concentration of basal plane dislocations, inclusions, micropipes and trapezoids. The wafers were from three vendors, and wafers with 10 um, 30 um and 60 um epitaxial layers were evaluated. The wafers with 10 um and 30 um epilayers were virtually free of BPDs, while BPD concentrations of the wafers with 60 um were too high for commercial use. Concentrations of inclusions, micropipes and trapezoids were also evaluated. Most of the wafers had acceptable levels of these defects, but device yield would be improved by more consistently having low concentrations.**

Keywords—BPD, inclusion, trapezoid, micropipe, SiC

I. Introduction

There has been significant progress in improving materials and fabrication issues concerning SiC power devices that are driving their commercial success. These improvements combined with the superior intrinsic properties of SiC compared to silicon are responsible for the growing fraction of power electronics equipment that is based on SiC devices. One of the necessary factors has been the steady improvement of SiC substrates and epitaxial layers. There are a number of extended defects that can be present in the device drift layer that is within the epitaxial layer. When extended defects are present in the drift layer, many of them adversely affect the device yield, and/or reliability.

In this work we have examined the density of BPDs and other extended defects that degraded device yield and reliability using ultraviolet photoluminescence (UVPL) imaging. Forty-nine 150 mm wafers from three commercial suppliers were examined. This wafer set included epitaxial layer thicknesses of 10 µm, 30 µm and 60 µm to be used in the fabrication of 1.2 kV, 3.3 kV and 6.5 kV MOSFETs, respectively.

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Section II presents the defect counts in the epilayers for this set of wafers. The following sections go into more detail and discuss the origins of the defects and their expected effects on yield and reliability of MOSFETs fabricated on these wafers.

II. Summary of Results

Four sets of 150 mm wafers were purchased from vendors A, B and C, and they included wafers with epilayer thicknesses of 10, 30 and 60 µm. After imaging the defects in the epilayers with UVPL, the number of BPDs, inclusions and micropipes in each wafer were counted. The counts ignored defects within 5 mm of the wafer edge, and the results are shown in Tables I - III. While there is no table for trapezoids, they are discussed in Section VI.

TABLE I. BPD Counts Per Wafer

Vendor	BPDs per wafer				
	Epi thickness (µm)	*Number of wafers*	*Min.*	*Average*	*Max.*
A	30	14	0	0.5	2
A	10	21	0	0.9	5
B	30	8	0	0.5	3
C	60	6	> 1000		

BPDs that originate from the substrate and continue into the epitaxial drift layer for the 10 µm and 30 µm were negligible. Through a combination of reducing BPDs in the substrate and epitaxial growth processes that convert almost all of the BPD at the substrate/epilayer interface into threading edge dislocations (TEDs), this low count of BPDs has been achieved. Note that the above BPD counts for vendors A and B only include BPDs originating from the substrate. Clusters of BPDs can also originate from inclusions that are caused by fall downs during epitaxial growth [1]. They are discussed in Section IV.

TABLE II. INCLUSIONS PER WAFER

Vendor	Inclusions per wafer				
	Epi thickness (µm)	*Number of wafers*	*Min.*	*Average*	*Max.*
A	30	14	0	14.9	47
A	10	21	0	0.14	2
B	30	8	39	60	93
C	60	6	6	12.3	19

There was a distinct increase in the average number of inclusions as the epilayer thickness increased above 10 µm. This increase was consistent with the assumption that the major source of inclusions was due to SiC down-falls from the growth chamber. Assuming that the growth time is 3 times as long for the 30 µm versus the 10 µm epilayers there is more time for SiC to build up inside the growth chamber and to fall down onto the wafer. There was not an increase comparing 30 µm to 60 µm epilayers, which may be due to different types of growth chambers or different growth conditions.

TABLE III. MICROPIPES PER WAFER

Vendor	Micropipes per wafer				
	Epi thickness (µm)	*Number of wafers*	*Min.*	*Average*	*Max.*
A	30	14	0	1.0	6
A	10	21	0	0.8	4
B	30	8	0	2.1	9

In UVPL images micropipes are not seen directly. Instead, small tight clusters of BPDs are observed that surround a micropipe. The BPDs are a result of the stress field around a micropipe. This local stress just outside a micropipe is equivalent to the stress of several threading screw dislocations clustered together. This stress field is large enough that the SiC crystal can lower its energy by creating a micron sized hole. The stress field is also sufficient to generate BPDs. Note that the stress from a single 1c threading screw dislocation is not sufficient to generate a BPD cluster.

III. BPDS

The adverse effects of BPDs on power devices were first reported by researchers working with ABB to develop 4.5 kV SiC PiN diodes two decades ago [2,3]. They found that the forward voltage drop of SiC PiNs increased during forward voltage operation and identified the faulting of BPDs in the epitaxial drift layer as the source of the increasing voltage drop. An example of BPD faulting to form a Shockley stacking fault (SSF) is shown in Fig. 1. After epitaxial growth, BPDs that continue into the epilayer are not faulted [4]. In this example, 1(a) shows a 3D schematic image of a BPD from the substrate that continues through the epilayer to the top of the epilayer. During electron-hole recombination, such as in a forward biased PiN diode, BPDs fault and create expanding SSFs as shown in Fig. 1(b), which shows a partially expanded SSF. Figure 1(c) is a cross-sectional view of the 3D image of both 1(a) and 1(b). Note that both the original BPD and the SSF are in the same basal plane.

The Shockley stacking faults (SSFs) that are formed from the BPD have the same local stacking order as 3C-SiC. The bandgap of 3C-SiC is 0.9 eV smaller than the bandgap of 4H-SiC. While the SSF is only a couple of atomic layers thick, it locally creates a discontinuity in the bandgap that primarily affects the conduction band edge as shown in Fig. 2 [5]. As the area of the SSF increases it captures more electrons and is a strong electron-hole recombination site. Within the area of a SSF, the carrier lifetime is suppressed, which reduces the local concentration of electrons and holes, resulting in a higher forward-voltage of a PiN diode or other bipolar device.

A second degradation mechanism was later identified that affected majority carrier mobility such as the on-state of a n-type MOSFETs [6,7]. As the local dip in the conduction band due to the stacking fault collects electrons, the conduction band on both sides move upward to maintain charge neutrality and the electron density is suppressed on both sides of the stacking fault.

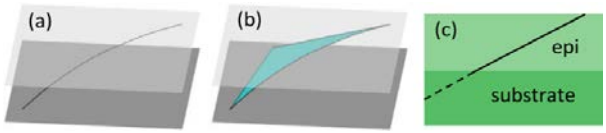

Fig. 1. Schematic example showing the development of a SSF from a BPD; (a) and (b) are 3D views before and during faulting with the darker gray at the substrate/epi interface and the lighter gray at the top of the epilayer, (c) is a cross-sectional view that stays the same as the SSF expands.

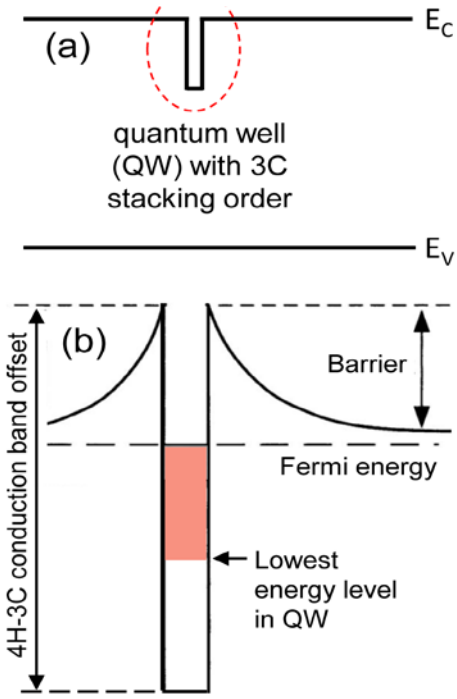

Fig. 2. The effect of a Shockley stacking fault (SSF) in 4H-SiC: (a) the local decrease of the conduction band edge (E_C) caused by the SSF, (b)for the Fermi level near E_C, electrons fill the QW and locally raises E_C , which depletes electrons near the SSF and forms a conduction barrier.

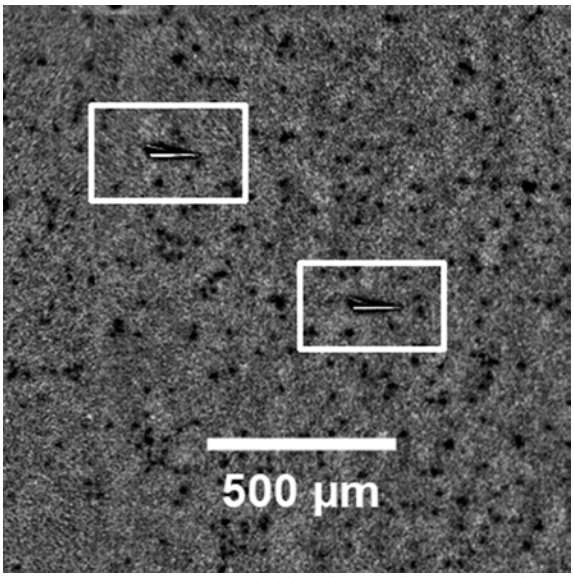

Fig. 3. Two BPDs in 10 µm thick epilayer. These BPDs originate from the substrate.

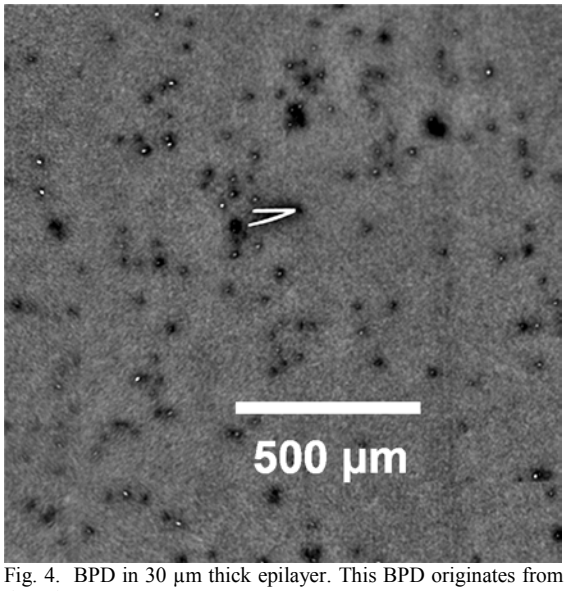

Fig. 4. BPD in 30 µm thick epilayer. This BPD originates from the substrate.

The suppressed conductivity in the area of the stacking fault increases the overall on-resistance of the MOSFET. This effect was been subsequently observed experimentally [7].

For higher current densities than normally encountered in MOSFETs, it is also possible to form stacking faults in the drift layer from faulting of BPDs in the n^+ buffer below the drift layer and from BPDs on the substrate side of the substrate/epilayer interface [8,9].

In power applications using MOSFETs, the body diode of the MOSFET is often conducting during switching, as well as during fault conditions. These conditions cause faulting of BPDs in the drift layer. Thus, BPDs in the epilayers of wafers to be used in the fabrication of MOSFETs must be minimized to have reliable MOSFETs. The wafers from vendors A and B satisfy the low-BPD requirement. An examples of the rare BPDs found in a wafer with 10 µm epilayer is shown in Fig. 3, and an example in a wafer with 30 µm epi is shown in Fig. 4.

Due to their high BPD density, MOSFETs fabricated on wafers from vendor C, 60 µm epilayer, will probably have low yield, and many of the MOSFETs that pass initial testing are likely to have low reliability. Figure 3 shows a UVPL image of one of the wafers. While it is not possible to distinguish individual BPDs, the brighter vertical streaks near the center are due to many vertical bands of BPDs. The shape and overall structure of these BPDs indicate they sid not originate from the substrate. Examination of this central section at full magnification suggests that these BPDs originated from the epilayer surface as the epilayer was being grown.

Figures 6-8 are of the regions marked by the squares in Fig. 5: 6 is the center region; 7 is to the left and 8 is to the right.

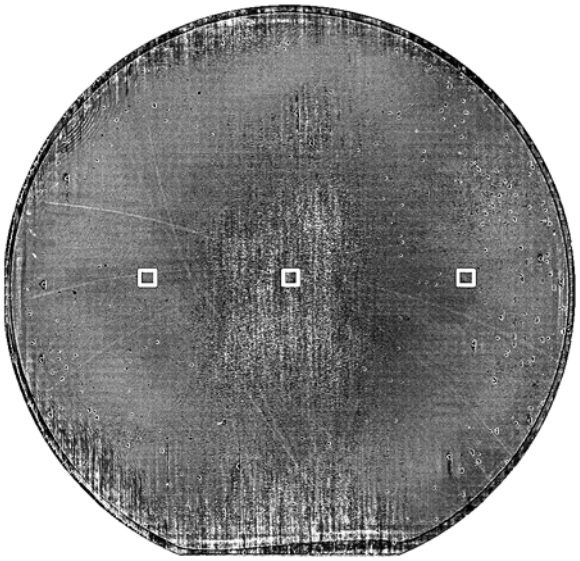

Fig. 5. UVPL image of one of the wafers with a 60 µm thick epilayer. The left, center and right box areas are shown in Figs. 4, 5 and 6.

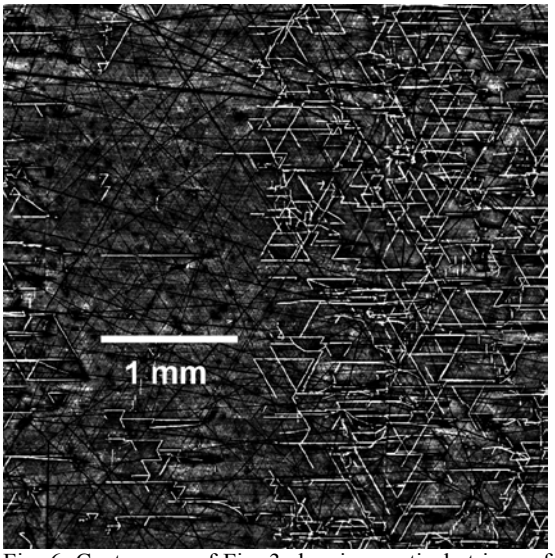

Fig. 6. Center area of Fig. 3 showing vertical strings of BPDs that extend many mm. These BPDs appear to be introduced during epi growth and do not originate in the substrate.

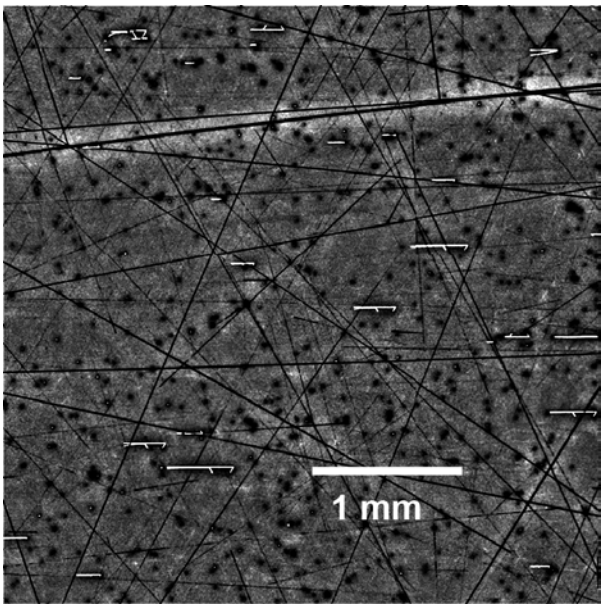

Fig. 7. Left area of Fig. 3 showing BPDs that originate from the substrate. The BPDs have different lengths because many of them convert to threading dislocations during epi growth.

Figures 7 and 8 show individual BPDs that did originate from the substrate. The density is approximately 200/cm^2 in Fig. 5, and 250/cm^2 in Fig. 6. Both of these densities are too high for useful MOSFETs.

In Figs. 3-8, the dark dots show the location of threading dislocations, which are primarily threading edge dislocations. A small fraction is screw type. Their contribution to leakage is negligible [10].

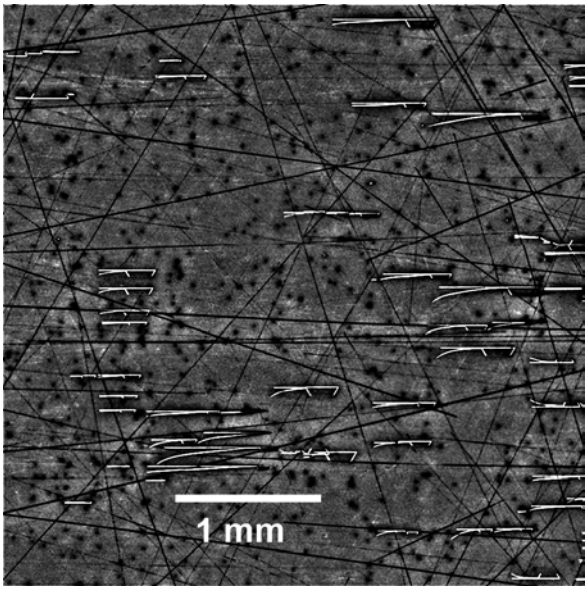

Fig. 8. . Right area of Fig. 3 showing BPDs that originate from the substrate. The BPDs have different lengths because many of them convert to threading dislocations during epi growth.

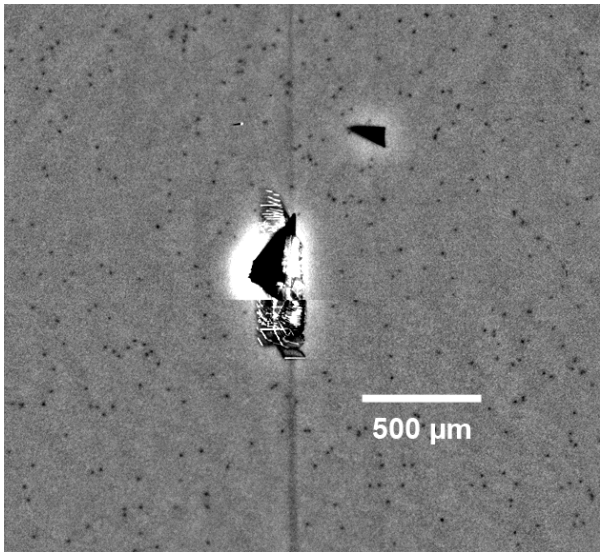

Fig. 9. Inclusion in in 10 µm thick epi due to a fall-down during epitaxial growth. This is the only inclusion in the 21 wafers examined.

IV. Inclusions

Inclusions are due to SiC down-falls from the growth chamber that distort the local growth where they land. Investigation of inclusions by high-resolution x-ray topography, micro-Raman imaging, and UVPL imaging has shown that that inclusions are a mixture of 3C and misoriented 4H polytypes. They strain the local area sufficiently to generate clusters of BPDs around them. They also distort the surface morphology [1].

Inclusions disrupt the operation and reliability of MOSFETs in two ways: the distorted surface morphology can degrade the gate oxide above it, and the BPDs they create can form stacking faults that can extend centimeters away from the inclusion site.

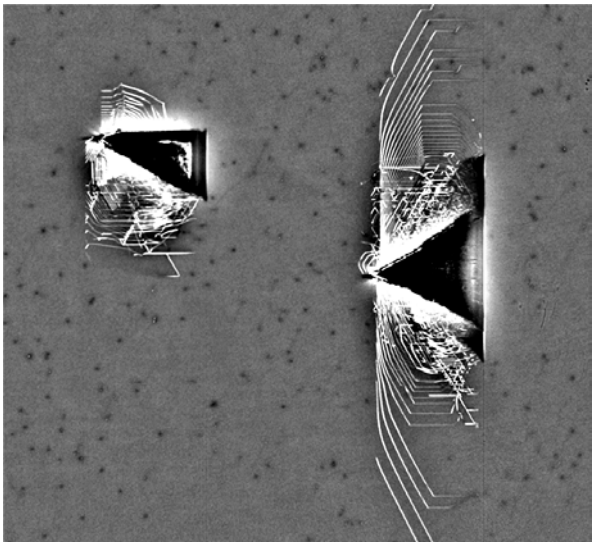

Fig. 10. Inclusions in 30 µm thick epi due to fall-downs during epitaxial growth. The average is 31/wafer and the BPDs glide farther from the inclusion.

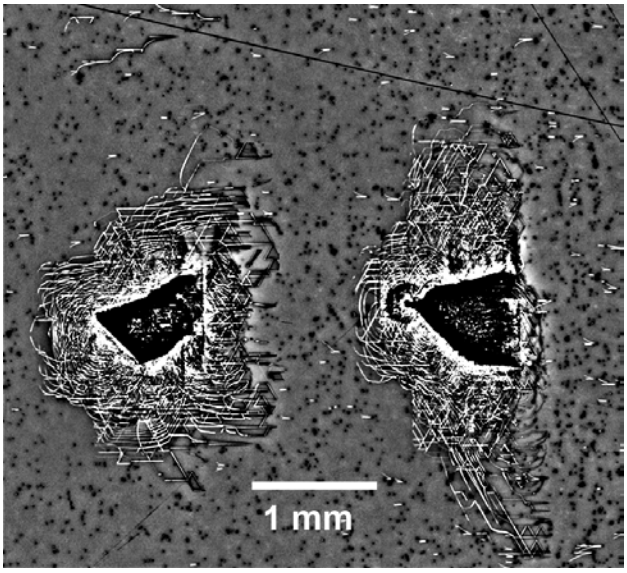

Fig. 11. Inclusions in 60 µm epi due to fall-downs during epitaxial growth. The average is 12 per wafer and the BPDs glide farther than for the 10 or 30 µm epi;avers.

V. MICROPIPES

The number of micropipes in a wafer is determined by the substrate, so it is not surprising that the minimum, maximum and average number of micropipes for the wafers with 10 µm and 30 µm epilayers are comparable for vendor A. The numbers are also similar for vendor B. For vendor C, with a 60 µm epilayer, too much of the area is obscured by BPDs from other sources to observe these BPD clusters. Figure 12 shows an example of the tight cluster of BPDs that is the signature for a micropipe. All of the micropipes observed had a similar cluster.

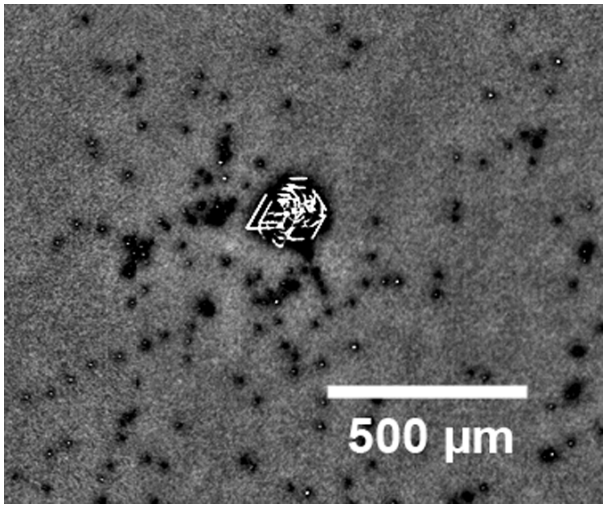

Fig. 12. Example of a BPD cluster that is produced by the stress around a micropipe.

VI. TRAPEZOIDS

The trapezoids are another defect that originates in the substrate. They propagate into the epilayer and through the full thickness of the epilayer. High resolution TEM has found that it contains Frank stacking faults [9]. UVPL imaging during extended UV exposure shows that some of the fault boundaries within a trapeziod move. This suggests that each trapezoid consists of multiple closely spaced faults, and that both Shockley and Frank stacking faults are present. This defect is likely to have similar effects on MOSFET operation as the stacking faults that originate from BPDs. This includes increasing the on-state resistance by decreasing the active area of the MOSFET that conducts current well.

The trapezoids vary in length, and their UVPL images indicate each trapezoid consists of multiple overlapping stacking faults. They often are present in clusters, but also can be isolated. These characteristics are illustrated in Fig. 13. Due to this behavior, their concentration is not easy to quantify and no table of concentrations is included.

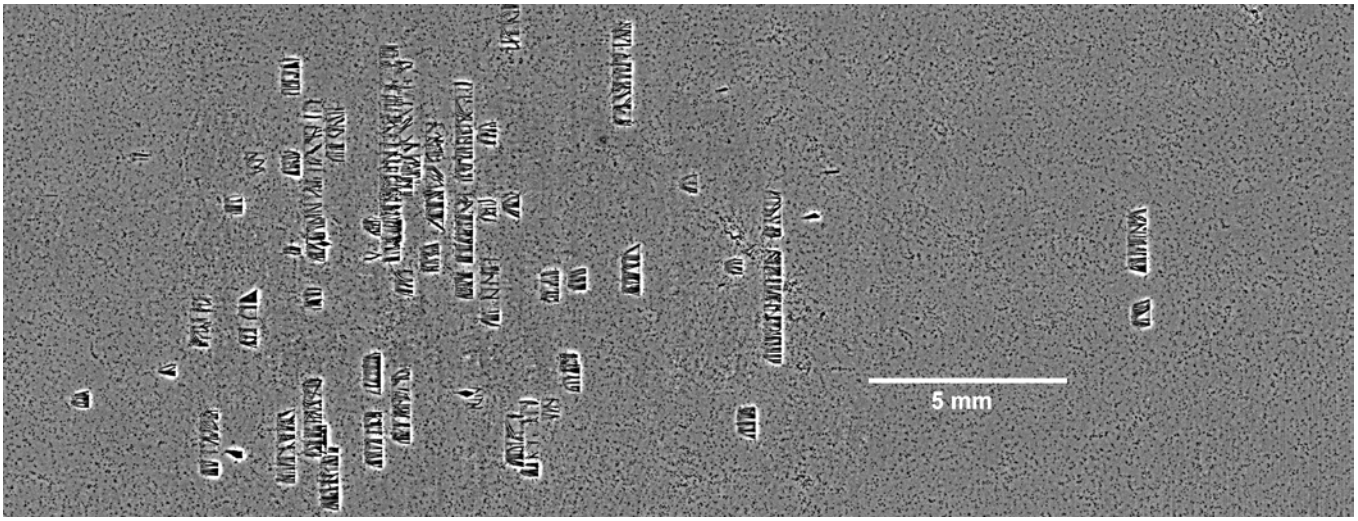

Fig. 13. Examples of trapezoid defects that originate in the substrate and propagate through the epitaxial layer (30 µm thick in this example). The variation of their density, which is typical, is illustrated.

VII. SUMMARY

Using UVPL imaging, the concentrations of BPDs as well as inclusions, micropipes, and trapezoids has been evaluated for 49 150 mm SiC wafers that will be used for MOSFET fabrication. The wafers came from three vendors and included wafers with 10 µm, 30 µm and 60 µm epi layers. The first two thicknesses had negligible BPDs; the worst wafer had 5 BPDs in the whole wafer and many of them had no BPDs in the epilayer. The wafers with 60 µm epilayers had > 1000 BPD/cm^2 over a majority of the wafer area, and accurate counts were not possible. The wafers with 10 µm had negligible inclusions, while the count in all of the other wafers could be improved. The average number of micropipes per wafer for all of the wafers was about one which is not significant. Trapezoid density could be improved.

The next steps for these wafers are to fabricate MOSFETs, and to examine the correlations between the various extended defects and the yield and reliability of the MOSFETs.

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