# Developing 13-kV 4H-SiC MOSFETs: Significance of Implant Straggle, Channel Design, and MOS Process on Static Performance

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***Abstract*— 13-kV 4H-SiC MOSFETs were successfully fabricated on a 125-$\mu$m-thick epitaxial layer on 6-in, N+ SiC substrates. Both lateral and longitudinal straggles from the P-well implant were investigated to optimize the JFET width and thus to avoid channel pinching in the JFET region. Channel lengths and channel mobilities were varied to investigate the effect of channel portions in determining the ON-state resistance of the 13-kV MOSFETs. It was discovered that the low channel mobility limits the transconductance, such that the MOSFETs cannot offer full current at reasonable gate voltages ($V_{gs} = \sim 20$ V). Even in high voltage MOSFETs, it is essential to have a reasonably high channel mobility to reduce ON-state power loss. Therefore, channel design and process are also important aspects of high voltage devices. A superior blocking capability of 13.2 kV was demonstrated using a ring-based edge termination structure. It is important to note that the straggling effect due to ion implantations should also be taken into account when designing an edge termination structure. Static electrical characteristics, scanning electron microscope (SEM) imaging, secondary ion mass spectrometry (SIMS) analysis, and 2-D simulation of the 13-kV MOSFETs were employed to support this reasoning.**

***Index Terms*— 4H-SiC, breakdown voltage, channel mobility, design consideration, edge termination, gate oxide, lateral straggle, longitudinal straggle, MOSFET, silicon carbide 4H-SiC, specific ON-resistance, transconductance, ultrahigh voltage.**

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## I. Introduction

THE breakdown voltage of power devices depends on the thickness and doping concentration of the drift region as the majority of voltage is supported by the depletion region formed within the drift region. The drift layer design must be optimized to target the specified breakdown voltage so that the power dissipation of the device is reduced. Due to the high critical electric field and low intrinsic carrier density of 4H-SiC, SiC has become a prominent material compared to silicon for fabricating energy-efficient power devices [1].

Ultrahigh voltage devices require a very thick drift layer for sufficient blocking capability, which, in turn, makes them difficult to manufacture due to the warpage and bow of the wafer. Despite the manufacturing challenges, 13-kV 4H-SiC MOSFETs were successfully fabricated at a 6-in, Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA.

It is important to take implant straggles into account when designing cell area and edge termination structures, especially for high voltage (>6.5 kV) devices in SiC. The low background doping level ($\sim<10^{15}$ cm$^{-3}$) in the N-drift layer results in substantial longitudinal and lateral straggles during the P-type implantations [2]–[5]. In addition, for 13-kV 4H-SiC MOSFETs, although drift layer resistance contributes the most to the total ON-resistance, it was discovered that channel mobility plays a significant role in determining the current level and, thus, the ON-resistance. These are critical aspects to consider in developing high voltage 4H-SiC MOSFETs, which is lacking in the previous literature [6], [7].

This article presents the analysis of the straggling effect of P-type implants in 13-kV MOSFETs using scanning electron microscope (SEM) images, secondary ion mass spectrometry (SIMS) analysis, and electrical characteristics. The optimization of both MOSFET and edge termination structures is also discussed. Different gate oxide recipes impacting channel mobility were utilized with different channel designs to analyze the significance of the channel portion on 13-kV 4H-SiC MOSFET's static performance.

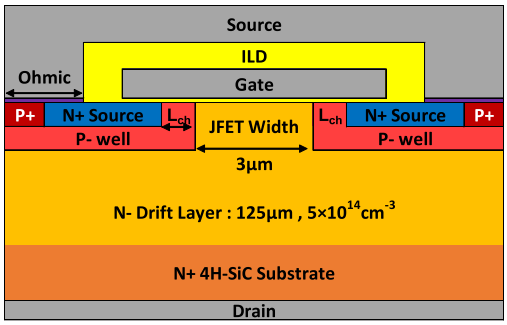



Fig. 1. Schematic cross-sectional view of the fabricated 13-kV 4H-SiC MOSFET. Important design parameters are labeled.

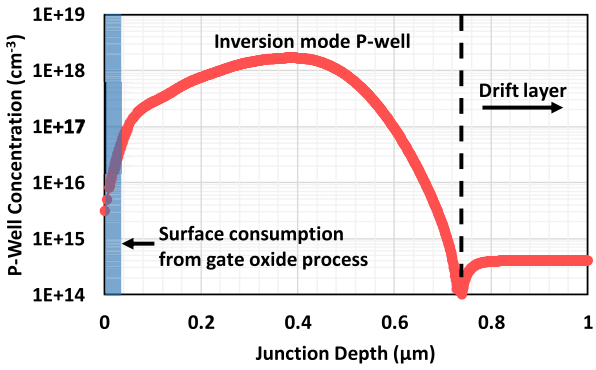



Fig. 2. Simulated 2-D stopping and range of ions in matter (SRIM) implant profiles to make inversion mode channel.

## II. High Voltage Device Design, Fabrication, and Experimental Results

### A. Device Architecture and Fabrication Process

Fig. 1 shows a schematic cross-sectional view of the 13-kV 4H-SiC MOSFET. Important design parameters are also labeled. The N-type doping concentration of $5 \times 10^{14}$ cm$^{-3}$ with a drift layer thickness of 125 $\mu$m on 6-in, N+ 4H-SiC substrates was used to fabricate 13-kV MOSFETs. High-temperature ion implantations using aluminum and nitrogen were used to form P-well, P+ body, junction–termination–extension (JTE), and N+ source, respectively. P-well profile was designed to create an inversion mode channel as shown in Fig. 2 [8]. Implant processes for P+ body and N+ source contacts for the MOSFET were also employed to make P+ floating field rings (FFRs) and channel stop regions at the periphery. After the implantation steps, wafers were activated at 1650 °C for 10 min with a carbon cap. A 50-nm-thick gate oxide was formed by 1) 1200 °C thermal oxidation in an $N_2O$ ambient for one wafer and 2) 800 °C ultrathin thermal oxide (2 nm) with 48 nm of deposited oxide, followed by a postoxidation anneal in $N_2O$ ambient for the other wafer for the channel mobility split. After, gate polysilicon was deposited and patterned. Then, an interlayer dielectric (ILD) was deposited and etched to open for ohmic contact regions. Nickel (Ni) metal was deposited on the front side and annealed for the self-silicidation process. Unsilicided Ni metals were removed, followed by 2 min of a rapid thermal anneal (RTA) at >900 °C. Backside metal contact was also formed by Ni deposition with the same RTA process. A 4-$\mu$m-thick aluminum (Al)-based metal was used for the source metal and the gate pad. The front side was passivated by nitride and polyimide. Finally, a solderable metal stack was deposited on the backside. Fig. 3 shows the cross-sectional SEM image of the fabricated 13-kV 4H-SiC MOSFET.

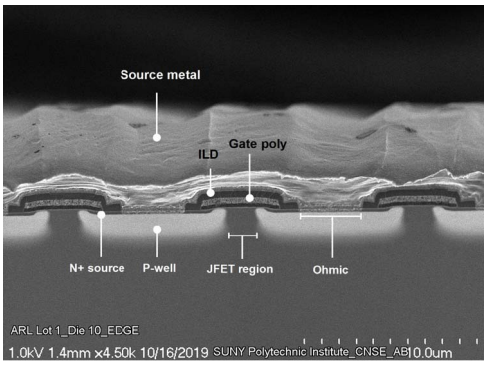



Fig. 3. Cross-sectional SEM image of the fabricated 13-kV 4H-SiC MOSFET.

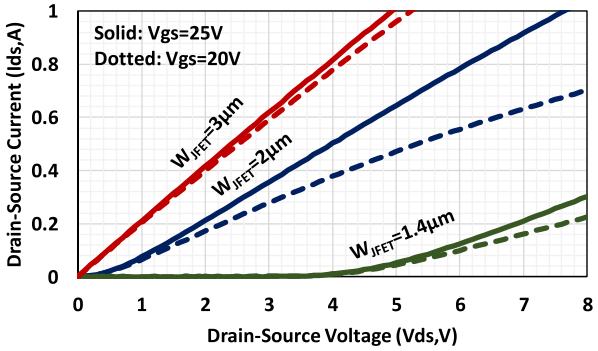
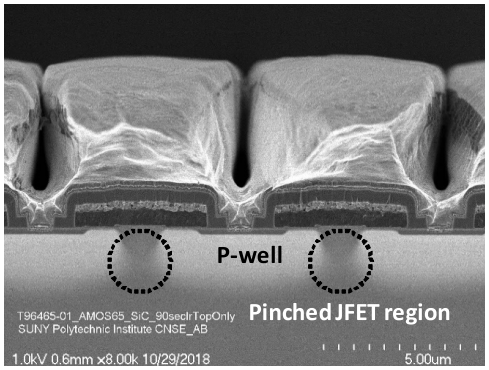



Fig. 4. Measured output characteristics of the fabricated 13-kV MOSFETs with JFET width ($W_{JFET}$) of 1.4, 2, and 3 $\mu$m. The abnormal pinching effects are observed when $W_{JFET}$ is 1.4 and 2 $\mu$m.

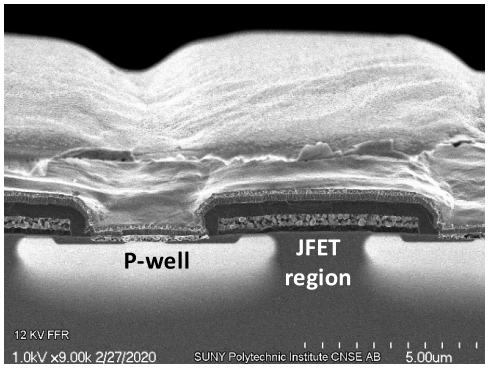
### B. Design Consideration for High Voltage MOSFETs: Effect of Lateral Straggle From P-Well Into JFET Region

When designing 13-kV MOSFETs, it is critical to design the JFET width ($W_{JFET}$) in a way that the lateral straggle of P-well implants does not pinch the current path in the JFET region [5]. Fig. 4 shows the measured output characteristics of the 13-kV MOSFETs with $W_{JFET}$ of 1.4, 2, and 3 $\mu$m, respectively. All other dimensions are kept the same for a fair comparison. The doping concentration in the JFET region was enhanced to $3 \times 10^{16}$ cm$^{-3}$ for this study. The abnormal pinching (knee) behaviors are observed when $W_{JFET}$ is 1.4 and 2 $\mu$m. However, the normal MOSFET operation is exhibited when the $W_{JFET}$ was designed to be 3 $\mu$m. Therefore, $W_{JFET}$ needs to be wider than at least 2.5 $\mu$m to avoid high ON-resistance from the channel pinching effect in the JFET region.

The cross-sectional SEM images of the MOSFETs with $W_{JFET}$ of 1.4 and 3 $\mu$m are shown in Fig. 5, respectively. The SEM images support that the channel path in JFET regions is pinched due to the lateral straggle from the P-well implants. For comparison, it is important to note that for low voltage (<1.2 kV) power MOSFETs, $W_{JFET}$ of even 1.4 $\mu$m is a sufficient width to secure a current path in the JFET region [9]. As shown in Fig. 6(a), a significant difference in junction




(a)




(b)

Fig. 5. Cross-sectional SEM images of the fabricated 13-kV MOSFETs with JFET width ($W_{JFET}$) of (a) 1.4 $\mu$m and (b) 3 $\mu$m, respectively. The channel path in JFET regions is pinched when the $W_{JFET}$ is 1.4 $\mu$m. This phenomenon is not observed when $W_{JFET}$ is 3 $\mu$m.

depth for simulated and measured SIMS P-well is observed. The SIMS profile exhibits the extension of the aluminum tail after a junction depth of 0.6 $\mu$m, which could not be estimated by the SRIM simulation. Due to the limitation of the SIMS tool, the tail of the P-well was estimated and drawn based on the analyzed SIMS data. The "expected" tail was extended up to 2 $\mu$m, which is also confirmed by SEM images in Fig 6(b). Although the JFET region was enhanced to $3 \times 10^{16}$ cm$^{-3}$ with a depth of about 1 $\mu$m, it was not enough to confine the aluminum tail caused by the longitudinal and lateral straggles. In the case of 1.2-kV MOSFET, the depth of P-well is about 0.7 $\mu$m based on the SEM image in Fig. 6(b). The P-well depth matches accordingly with the SRIM simulation. This can be attributed to higher background doping concentration in 1.2-kV MOSFET, which can confine the depth of aluminum tails at $8 \times 10^{15}$ cm$^{-3}$. However, for the case of 13-kV MOSFET, the junction depth of the P-well is deeper due to the extension of aluminum tails up to the low background concentration of $5 \times 10^{14}$ cm$^{-3}$. The cause of substantial straggles in ultrahigh-voltage power devices thus originates from the low N-type background doping concentration, unlike in low voltage (<1.2 kV) power devices.

## III. Importance of Channel Mobility in High Voltage MOSFETs

### A. On-Wafer, Static Electrical Characteristics

Fig. 7 shows the extracted field effect channel mobilities ($\mu_{ch}$) of two different gate oxide processes at 25 °C and 175 °C fat field-effect transistor (FATFETs) with a channel length of 200 $\mu$m. The difference in the $\mu_{ch}$ is attributed to the interface traps from different gate oxide recipes [10]. Gate-to-source (gate oxide) breakdown in Fig. 8 supports that both recipes exhibit a good quality gate oxide. The room temperature, typical on-wafer output characteristics of the fabricated 13-kV 4H-SiC MOSFETs with two different gate oxide splits; channel mobility of 3 cm$^2$/Vs for $N_2O$ grown oxide and 7.5 cm$^2$/Vs for deposited oxide are shown in Fig. 9, respectively. The measured MOSFETs have channel lengths ($L_{ch}$) of 1 $\mu$m and JFET width ($W_{JFET}$) of 3 $\mu$m.

Fig. 10(a) shows the optical image of the fabricated wafer (red dotted lines indicate the measured dies), along with extracted specific ON-resistance ($R_{ON,sp}$) of 13-kV MOSFETs at a gate–source voltage ($V_{gs}$) of 20 V. As shown in the wafer map, the MOSFETs with $\mu_{ch}$ of 7.5 cm$^2$/Vs provide lower $R_{ON,sp}$ than $\mu_{ch}$ of 3 cm$^2$/Vs. The box plot in Fig. 10(b) also shows the difference in $R_{ON,sp}$ with different $\mu_{ch}$, and about 13% (240 versus 208 m$\Omega$-cm$^2$) of $R_{ON,sp}$ improvement is seen when $\mu_{ch}$ is enhanced. This first hints that channel mobility plays an important role in determining $R_{ON,sp}$ of the ultrahigh voltage devices despite the drift layer resistance being the most prominent contributing portion of the total ON-resistance.

Extracted $R_{ON,sp}$ as a function drain–source voltage ($V_{ds}$) with varying temperatures at a $V_{gs}$ of 20 V are shown in Fig. 11. At 25 °C, it is observed that $R_{ON,sp}$ is constantly increasing with $V_{ds}$ for $\mu_{ch}$ of 3 cm$^2$/Vs because the current cannot be fully extracted at $V_{gs}$ of 20 V with low channel mobility. However, the same phenomenon is not seen for the MOSFET with $\mu_{ch}$ of 7.5 cm$^2$/Vs. This implies that high channel mobility is also essential for the operation of 13-kV MOSFETs at reasonable $V_{gs}$. At high-temperature operation, the increase of resistance with $V_{ds}$ is not observed even for the case of $\mu_{ch}$ of 3 cm$^2$/Vs due to the enhancement of channel mobility at high temperature as shown in Fig. 7. Even at 175 °C operation, the MOSFET with high channel mobility exhibits lower $R_{ON,sp}$. The impact of channel mobility on 13-kV MOSFETs was observable because the $\mu_{ch}$ of 3 cm$^2$/Vs is too low to be used compared to the $\mu_{ch}$ of 7.5 cm$^2$/Vs. This secondly elucidates that the effect of channel mobility in high voltage 13-kV power devices is also significant.

The 13-kV MOSFETs with a channel length of 2 and 4 $\mu$m were also fabricated to investigate the impact of channel components in high voltage devices. Measured on-wafer output characteristics are shown in Fig. 12(a) and (b). Similar to the MOSFETs with $L_{ch}$ of 1 $\mu$m, differences in current–voltage ($I - V$) behaviors for $L_{ch}$ of 2 and 4 $\mu$m are observed with different channel mobilities. However, a significant distinction in the $I - V$ characteristics can be found in the case of the wider $L_{ch}$ (4 $\mu$m). Fig. 12(c) shows an average $R_{ON,sp}$ for MOSFETs with $L_{ch}$ of 2 and 4 $\mu$m. A reduction in ON-resistance for MOSFETs with $L_{ch}$ of 2 and 4 $\mu$m is 22% (292 versus 228 m$\Omega$-cm$^2$) and 40% (472 versus 283 m$\Omega$-cm$^2$) when comparing MOSFETs with $\mu_{ch}$ of 3 and 7.5 cm$^2$/Vs, respectively. A significant change is observed for the MOSFETs with longer channel lengths, and this indicates that channel mobility and, therefore, the channel component plays

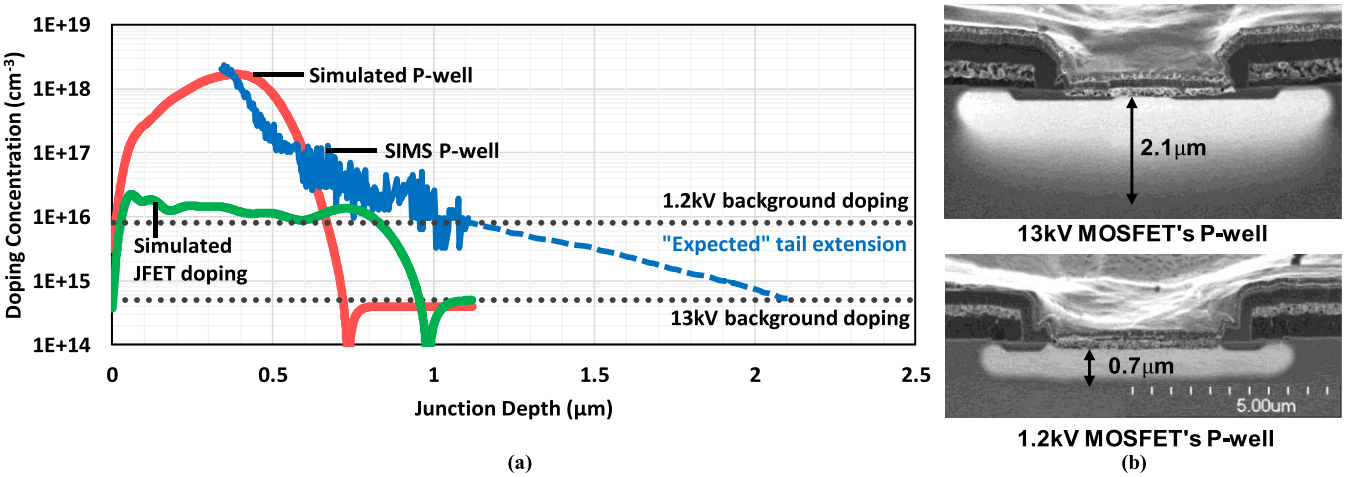



Fig. 6. (a) Doping profiles for simulated P-well and JFET and measured SIMS profiles for P-well to illustrate the cause of substantial straggle. "Expected" tail was estimated and drawn based on the analyzed SIMS P-well profile. As shown in (b), cross-sectional SEM images show the difference in depth of P-well for 13- and 1.2-kV MOSFET from the background doping concentration. The same implantation conditions (dose and energy) were used.

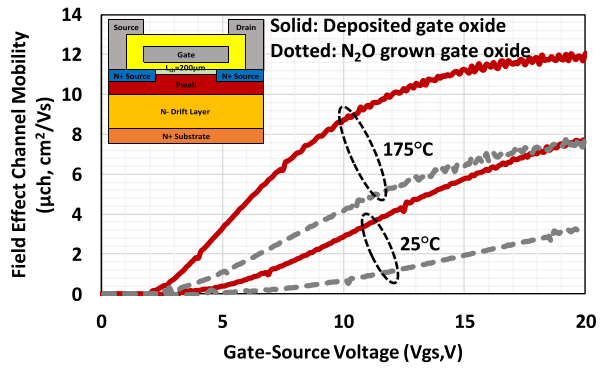



Fig. 7. Extracted field effect channel mobilities at 25 °C and 175 °C from the lateral test MOSFET structures (FATFETs) with a channel length of 200 $\mu$m. Inset shows a schematic cross-sectional view of the FATFET structure.

a critical role in determining the total ON-state resistance of the 13-kV 4H-SiC MOSFETs.

### *B. Transfer Characteristics and Transconductance: In-Depth View of Channel Mobilities in 13-kV 4H-SiC MOSFETs*

To further address the importance and impact of channel mobility in 13-kV MOSFETs, transfer characteristics and transconductance ($G_m$) of the MOSFETs were analyzed at 25 °C and 175 °C, as shown in Fig. 13. In the case of MOSFETs with $\mu_{ch}$ of 3 cm$^2$/Vs at 25 °C [see Fig. 13(a)], the peak $G_m$ occurs at $V_{gs}$ of 12 V and does not get to zero even at $V_{gs}$ of 20 V. However, when the $\mu_{ch}$ is 7.5 cm$^2$/Vs, a strong $G_m$ peak is observed at low $V_{gs}$ of 8 V and then gradually decreases to zero. This indicates that all the current in the MOSFET cannot be completely extracted at reasonable $V_{gs}$ due to the poor $G_m$ behavior with low channel mobility (3 cm$^2$/Vs). It is important to note that a high $G_m$ with a peak at low $V_{gs}$ is preferable for high current handling capability at reasonable $V_{gs}$ of $< 20$ V. Although higher $V_{gs}$ could be used to further reduce the ON-resistance, it is preferable

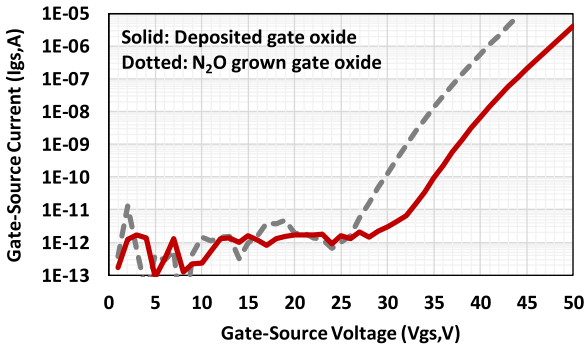



Fig. 8. Measured gate-to-source (gate oxide) breakdown voltage of two different gate oxide recipes.

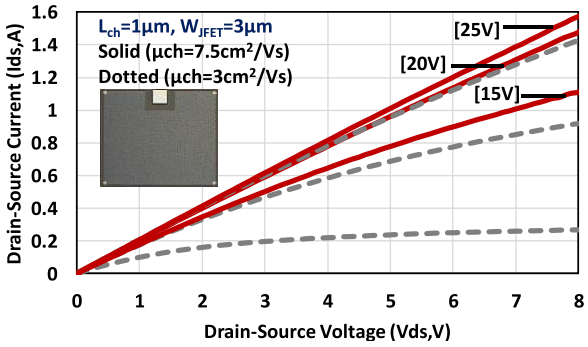



Fig. 9. On-wafer output characteristic of the fabricated 13-kV SiC MOSFET, measured at 25 °C. Inset shows the optical image of the MOSFET. (Active area = 4.5 mm$^2$, $L_{ch}$ = 1 $\mu$m, and $W_{JFET}$ = 3 $\mu$m.)

to operate the MOSFET at lower gate biases to avoid any gate oxide related reliability issues. At 175 °C operation [see Fig. 13(b)], the peak $G_m$ for both MOSFETs shifts toward smaller $V_{gs}$ and reaches zero at about 10 V, thanks to the enhancement of channel mobility at high temperature (see Fig. 7). A correlation between the threshold voltage ($V_{TH}$) and channel mobility with varying junction temperatures is shown in Fig. 14. As expected, $V_{TH}$ decreases with higher channel mobility.

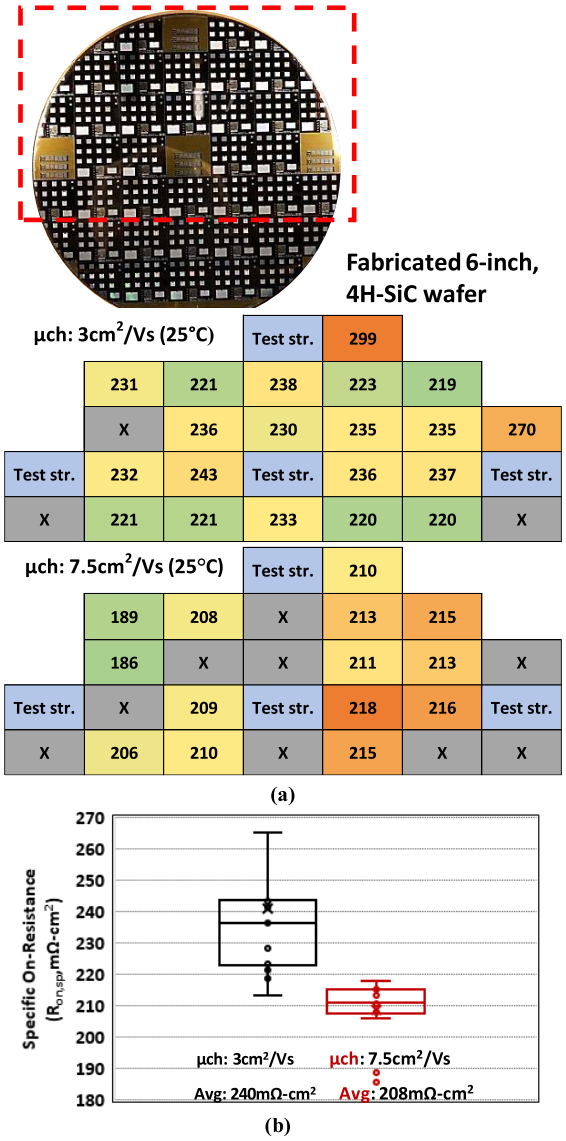



Fig. 10. (a) Optical image of the fabricated 13 kV SiC MOSFETs on 6 in, 4H-SiC wafer, followed by a wafer-map of extracted specific ON-resistance from the MOSFETs with a channel length of 1 $\mu$m and different channel mobilities. "X" represents nonworking devices. (b) Box plot distribution of $R_{ON,sp}$ with different channel mobilities. A 13% improvement is observed.

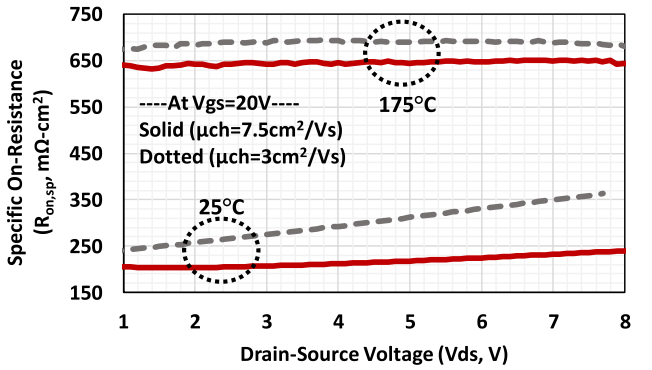



Fig. 11. Extracted specific ON-resistance as a function of drain–source voltage with varying temperatures at gate–source voltage of 20 V.

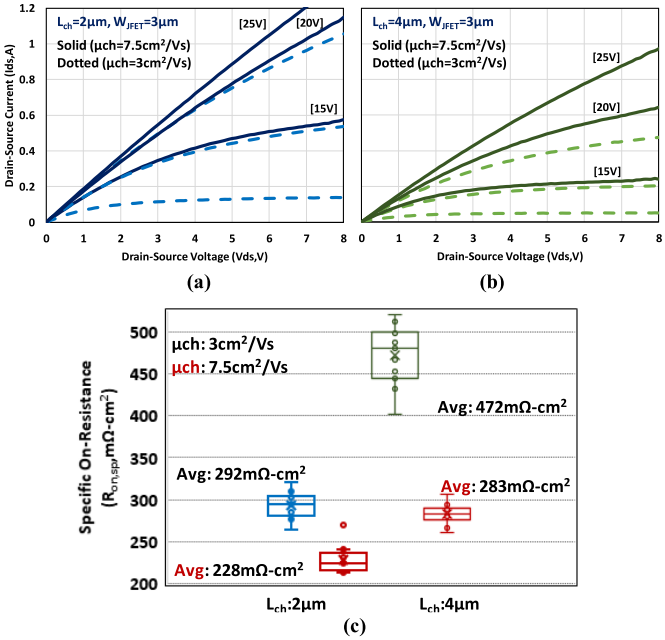



Fig. 12. On-wafer output characteristic of the fabricated 13-kV MOSFETs with a channel length of (a) 2 $\mu$m and (b) 4 $\mu$m, measured at 25 °C. (c) Box plot distribution of $R_{ON,sp}$ with different channel lengths and channel mobilities.

In addition, the correlation between channel mobility and transfer characteristics of 13-kV MOSFETs was further analyzed for MOSFETs with wider channel lengths ($L_{ch}$ = 2 and 4 $\mu$m), as shown in Fig. 15. It is observed that the peak and zero $G_m$ values vary with different $L_{ch}$, where poor $G_m$ is attributed to the low channel mobility. As expected, $\mu_{ch}$ of 3 cm$^2$/Vs is too low to be used in 13-kV MOSFETs with long channel lengths as peak and zero $G_m$ does not occur at reasonable gate voltages. This implies that these MOSFETs ($L_{ch}$ = 2 and 4 $\mu$m) cannot be operated at a reasonable $V_{gs}$ (20 to 25 V) due to weak gate control at lower $V_{gs}$ and that channel mobility is an important factor in determining the ON-state operation of the 13-kV SiC MOSFETs.

Fig. 16 shows the impact of channel component (channel mobility and channel length) to the total ON-resistance of the 13-kV SiC MOSFET. It is observed that channel resistance ($R_{ch}$) of the MOSFET, especially with larger $L_{ch}$ (4 $\mu$m), is significant when $\mu_{ch}$ is low (3 cm$^2$/Vs). When $\mu_{ch}$ is enhanced to 7.5 cm$^2$/Vs, the $R_{ch}$ significantly reduces, but the contribution of $R_{ch}$ is still high. If $\mu_{ch}$ was high enough (~20 cm$^2$/Vs), $R_{ch}$ would not be dependent on the $L_{ch}$ with $\mu_{ch}$ as it is shown in Fig. 16. This suggests that there is still a room for further improvement by adopting a better gate oxide recipe in conjunction with the accumulation-mode channel, and the channel mobility can be increased as high as 20 cm$^2$/Vs. The impact of channel component in the high voltage (13 kV) MOSFET could be minimized as shown in the blue lines of Fig. 16. Therefore, although drift layer resistance is the dominating portion of the total specific ON-resistance in 13-kV SiC MOSFETs, a sufficient channel mobility is necessary for different channel lengths because $G_m$ determines the drain current control. As a result, it is also essential

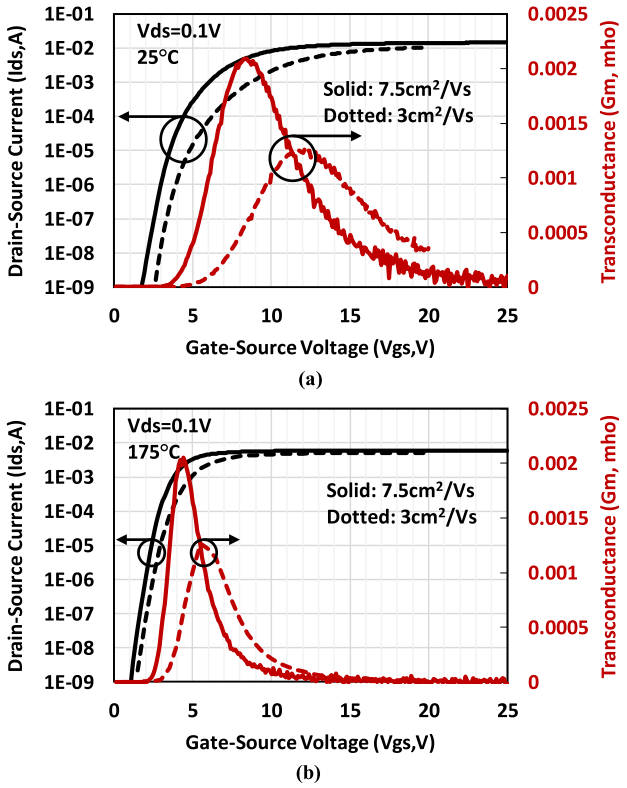



Fig. 13. Transfer characteristics and transconductance of the fabricated 13-kV MOSFETs with a channel length of 1 $\mu$m, measured at (a) 25 °C and (b) 175 °C.

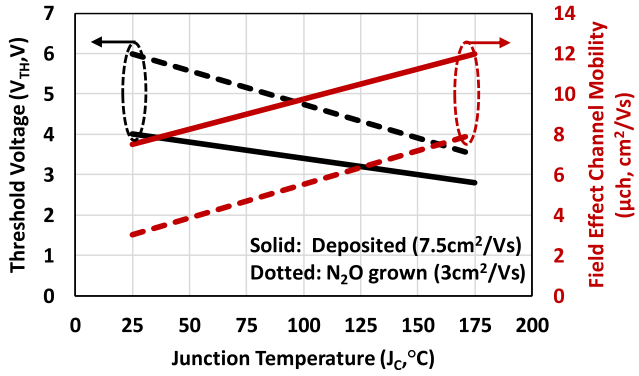



Fig. 14. Tradeoff curve between threshold voltage ($V_{TH}$) and channel mobility ($\mu_{ch}$) with temperatures. $V_{TH}$ was extracted at $I_{ds}$ of 100 $\mu$A, at $V_{ds}$ of 1 V.

for high voltage MOSFETs to have reasonably high channel mobility to achieve low power loss.

## IV. High Voltage Edge Termination Design

It is critical to design an efficient edge termination structure, especially in ultrahigh voltage power devices. In order to achieve the targeted breakdown voltage with given drift design, P+ FFR edge termination structure was designed. The schematic cross-sectional view of the FFR structure is shown in Fig. 17(a). The placement of the concentrated rings in the periphery regions was defined in a manner by the formula $S_n = S_0 + S_i(n-1)$, where $S_n$ is $n$th spacing, $S_0$ is spacing between the first ring and the main junction, $S_i$ is incremental

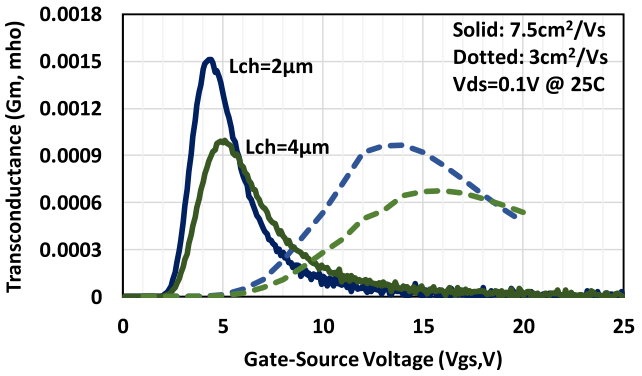



Fig. 15. Measured transconductance of the fabricated 13-kV MOSFETs with a channel length of 2 and 4 $\mu$m, measured at 25 °C.

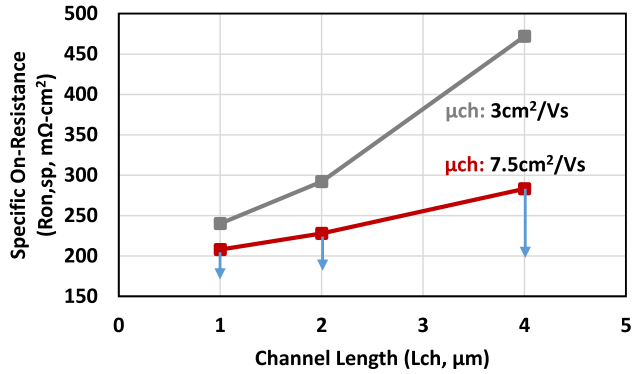



Fig. 16. Extracted specific ON-resistance as a function of channel lengths at different channel mobility. Blue lines represent further improvement by adopting a better gate oxide recipe in conjunction with the accumulation-mode channel.

spacing, and $n$ is the number of the rings [11]. The FFR structure is optimized when $S_0$ is 0.8 $\mu$m, $S_i$ is 0.08 $\mu$m, and the ring width is 5 $\mu$m with a total of 100 concentrated rings.

In the FFR structure, $S_0$ is a critical parameter as a premature breakdown at the main junction can occur if the spacing between the first and main junctions is not optimized. As mentioned in Section II-B, the lateral straggle should also be considered when designing the FFR edge termination structure as straggle can disrupt the optimized P+ ring spacing [12]. Fig. 17(b) and (c) shows the schematic cross-sectional view and SEM images of the FFR structure with the lateral straggle, respectively. As shown in the SEM images, the straggles are severe near the main junction area due to less spacing between P+ concentrated rings. This signifies that a couple of the rings that are near the main junction will not be effective in alleviating the electric fields properly. P+ rings with straggles become equivalent to the extended main junction as confirmed by the SEM image.

Two-dimensional TCAD simulation was carried out to further investigate the effect of the FFR edge termination structures with and without P+ straggles, as shown in Fig. 18. When the FFR structure is incorporated with the straggling effect [see Fig. 18(b)], the formation of the depletion region in the drift layer is different, and most of the electric field is crowded at the last ring, as shown in Fig. 18(c). It is

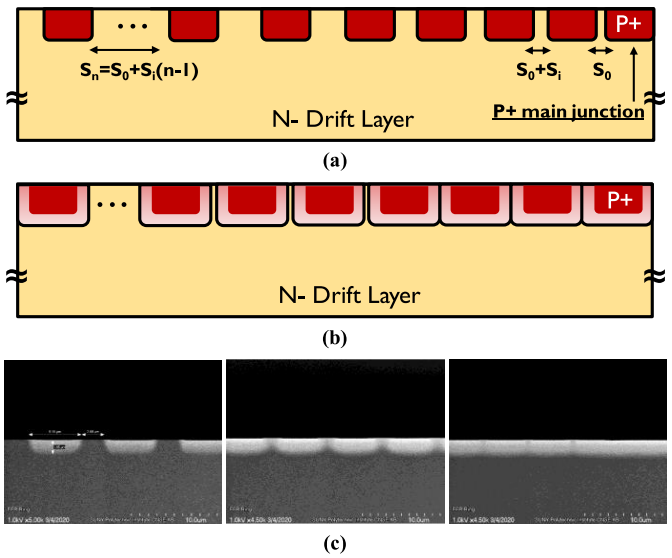



Fig. 17. Schematic cross-sectional view of the P+ FFR edge termination (a) without and (b) with straggles. (c) SEM images of FFR structure. A straggling effect is observed from the P+ rings.

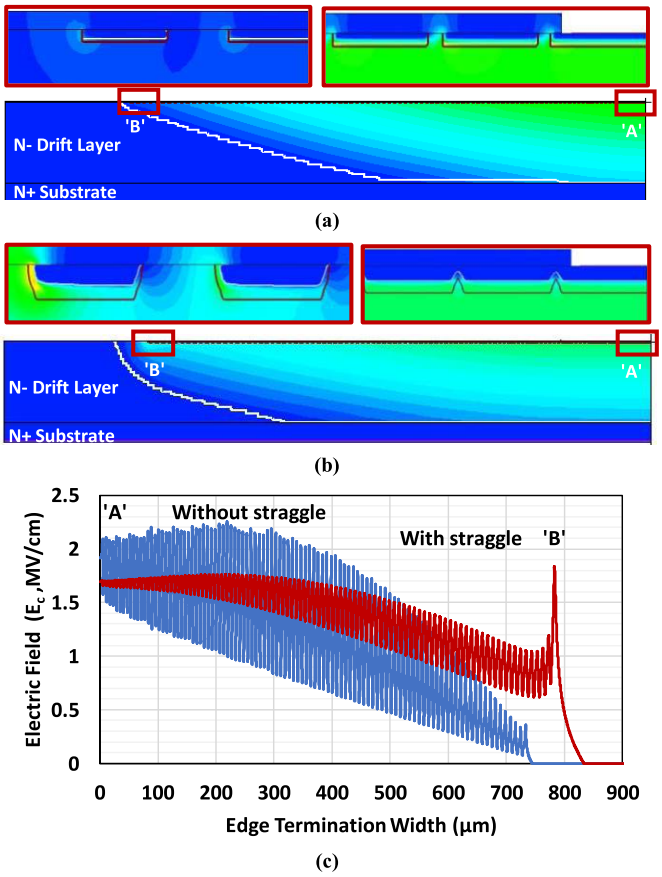



Fig. 18. Simulated P+ FFR edge termination structure (a) without, (b) with straggles, and (c) electric field distribution at breakdown condition.

observed that electric fields are not distributed properly. This is attributed to the connection of P+ rings near the main junction and smaller spacing between rings due to the implant straggle. Without the implant straggles taken into consideration, as is the case in 1.2-kV power devices, the electric fields are well distributed across the concentrated rings. The simulated breakdown voltages with and without straggles are 13.6 and 14.4 kV, respectively. Therefore, it is important to take straggle into account when simulating and designing edge termination structures for high voltage devices.

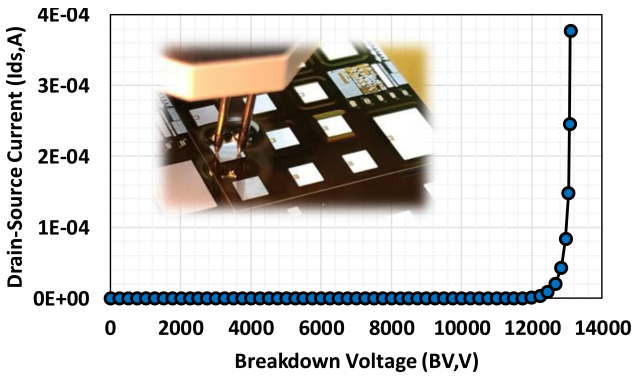



Fig. 19. Measured forward blocking behaviors of the fabricated 13-kV MOSFET using FFR edge termination structure. The breakdown voltage of 13.2 kV with very low leakage current was demonstrated. Inset shows an optical image of the 13-kV wafer in Fluorinert FC-40 to avoid arcing during the high voltage measurement.

Fig. 19 shows the measured forward blocking capability of the fabricated 4H-SiC MOSFETs. A breakdown voltage of 13.2-kV at drain–source current ($I_{ds}$) of 100 $\mu$A with very low leakage current was successfully demonstrated. Inset shows the optical image of the submerged 6-in, 13-kV wafer in Fluorinert FC-40 to avoid arcing during the high voltage measurement. The breakdown voltage could be even higher when considering the aforementioned issues. The ideal simulated breakdown voltage is 15.4 kV.

## V. Conclusion

The 13-kV 4H-SiC MOSFETs were successfully fabricated and demonstrated on 6-in, N+ substrates. Ultrahigh voltage power MOSFETs with low background doping concentrations for the drift layer ($\sim 5 \times 10^{14}$ cm$^{-3}$) and edge termination structures require the consideration of the straggle of P-type dopants (aluminum). SEM imaging and SIMS analysis were employed for the investigation of the straggling effect. The 13-kV SiC MOSFETs with different channel lengths and gate oxides (i.e., channel mobilities) were fabricated to elucidate the significant impact of channel components on total ON-resistance in the high voltage MOSFETs by analyzing the static electrical characteristics. Although drift layer resistance is the most dominant portion in determining total ON-resistance of the 13-kV SiC MOSFETs, it is essential to have reasonably high channel mobility to operate the MOSFETs at reasonable gate–source voltage.

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