Gate Leakage Current and Time-Dependent Dielectric Breakdown Measurements of Commercial 1.2 kV 4H-SiC Power MOSFETs

Tianshi Liu, Shengnan Zhu, Susanna Yu, Diang Xing, Arash Salemi, Minseok Kang, Kristen Booth, Marvin H. White and Anant K. Agarwal
The Ohio State University
Columbus, Ohio, USA
liu.2876@osu.edu

***Abstract*—Gate leakage current and constant-voltage time-dependent dielectric breakdown (TDDB) measurements at room temperature and elevated temperatures of commercially available large-area 1.2 kV 4H-SiC power MOSFETs are performed to investigate their gate oxide reliability and better understand their failure modes. It is shown that Fowler-Nordheim (F-N) tunneling current is the dominant mechanism contributing to the gate leakage current. Despite anomalous gate leakage current behaviors that could be caused by interface states densities (D_{it}) and near interface oxide traps, leakage currents at normal operating condition (V_G = 20 V at 28°C) are less than 100 pA for all vendors. Extrapolation from TDDB measurements shows that the predicted lifetimes when V_G = 20 V at both 28°C and 175°C are far longer than the targeted 10 years.**

***Index Terms*—Silicon Carbide (SiC), MOSFETs, oxide reliability, Folwer-Nordheim, TDDB, failure time**

I. Introduction

There has been considerable interests in the investigation of the gate oxide reliability for small-area SiC MOS capacitors and DMOSFETs during the past 20 years [1], [2]. A recent study published by CREE presented the gate oxide reliability measurements for on-wafer large-area SiC MOS capacitors [3]. It described the extrapolated gate oxide lifetime at gate voltage of 15 V being larger than 10^8 hours at 175°C. Ion implantation followed by high temperature anneal is normally utilized in SiC power MOSFETs fabrication. The ion implantation process creates damage in the SiC crystal [4] and consequently affect the gate oxide reliability and ruggedness. Therefore, for large-area SiC power MOSFETs that are now becoming commercially available, a comprehensive study of the gate oxide reliability is needed for the next growth markets such as electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs).

Table I shows the general information of the tested commercial power MOSFETs in this work. Gate leakage current and constant-voltage stress TDDB measurements were conducted in these commercial devices at both room and elevated temperatures.

TABLE I
TESTED 1.2 KV COMMERCIAL DEVICES

Vendors	Type	Current Rating	Typical V_{th}	Typical $R_{DS,on}$
C	DMOSFET	12 A	9.5 V	600 $m\Omega$
D	T-MOSFET	17 A	5.5 V	200 $m\Omega$
E'	DMOSFET	10 A	4 V	380 $m\Omega$

II. Experimental Method

A. Gate Leakage Current Measurements

Fig. 1 shows the diagram of the proposed setup for gate leakage current measurement. A packaged commercial MOSFET was placed into the test fixture (N1295A) with its source and drain shorted to ground. A positive gate voltage sweep was applied through the high power SMU of curve tracer (B1505A) to the gate electrode at 28°C, 175°C and 280°C and the gate leakage current was measured until the gate oxide breaks down. When measuring at higher temperatures, the packaged devices were placed on top of a hot plate with an insulating pad.

Fig. 2 (a) shows the gate leakage measurement for vendor E' at different temperatures. The gate voltage is swept from 0 V to breakdown voltage, and the gate leakage current compliance is set at 100 mA to protect the curve tracer. For 28°C and 175°C, the measurement results of less than 30 V are not actual leakage current but the noise floor of the measurement setup. Also, it is suspected that the leakage current increase at 280°C is due to shunt paths through the plastic package. The packages of all these commercial devices are only rated at 175°C. Therefore, it is reasonable to assume that increasing leakage current at low gate oxide electric field is due to package degradation at 280°C.

It has been previously reported that at high gate oxide electric field, Fowler-Nordheim (F-N) tunneling mechanism is the dominant contribution to gate leakage current [1]. F-N tunneling can be expressed as:

$$J_{FN}(T) = A(T)E_{ox}^2 \exp\left(\frac{-B(T)}{E_{ox}}\right) \quad (1)$$

978-1-7281-3761-2/19/$31.00 ©2019 IEEE

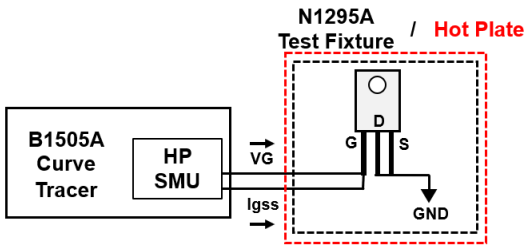

Fig. 1. Illustration of the experimental setup for measuring Fowler-Nordheim tunneling current.

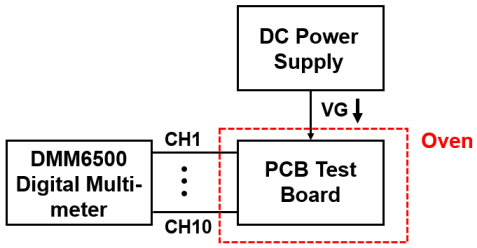

Fig. 3. Illustration of experimental setup for Time-Dependent Dielectric Breakdown (TDDB).

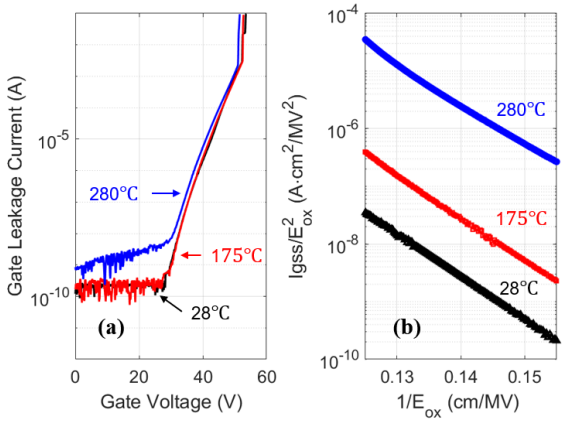

Fig. 2. (a) Gate current-voltage characteristics for Vendor E' at 28°C, 175°C and 280°C and (b) F-N tunneling plots for Vendor E' at 28°C, 175°C and 280°C.

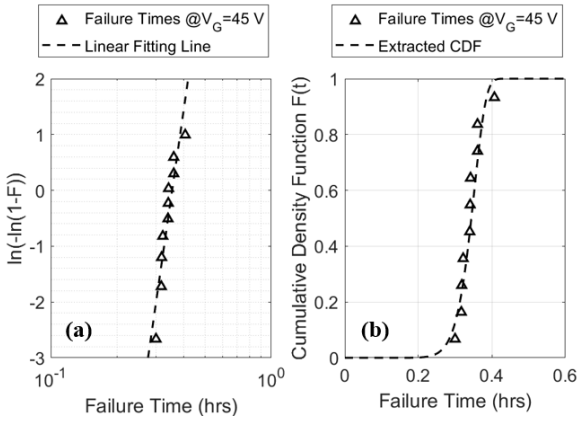

Fig. 4. Example of extracting $t_{63\%}$ failure time with vendor E' TDDB measurement at V_G=45 V.

where $J_{FN}(T)$ is the tunneling current density, E_{ox} is the gate oxide electric field, $A(T)$ and $B(T)$ are temperature dependent coefficients. Equation (1) can be rearranged into a linear form as:

$$ln(J_{FN}(T)/E_{ox}^2) = -B(T)/E_{ox} + ln(A(T)). \quad (2)$$

This is often referred as F-N plot. F-N plots at three temperatures for vendor E' are shown in Fig. 2 (b) assuming that the oxide thickness is 50 nm. It demonstrates linear relationships for over four decades of changes for all three temperatures. It shows that F-N tunneling is the dominant mechanism contributing to gate leakage under all three temperatures.

B. TDDB Measurements

Fig. 3 illustrates the proposed TDDB measurement setup. To investigate TDDB, 10 devices were tested at each gate oxide voltage to obtain an accurate prediction of the failure times due to the statistical nature of dielectric breakdown. During the measurement, 10 devices were placed in parallel on a PCB test board while all their source and drain electrodes were connected to ground. A constant gate voltage was applied to all 10 gate electrodes. A fuse and a resistor were placed in series with each MOSFET to limit the current flow during breakdown. A 10-channel digital multi-meter (DMM6500) was used to monitor the voltage drop across the resistors. When a MOSFET broke down, multi-meter displayed sudden voltage change across the resistor and the time was recorded as the failure time of that MOSFET.

Studies have shown that Weibull distribution can be used to successfully fit TDDB experimental data [2],[3]. The cumulative density function (CDF) of a two parameter Weibull distribution has the form of:

$$F(t) = 1 - \exp(-(\frac{t}{\eta})^{\beta}) \quad (3)$$

This can be rearranged into:

$$ln(-ln(1 - F(t))) = \beta ln(t) - \beta ln(\eta) \quad (4)$$

where, β and η are the slope parameter and characteristic lifetime of the Weibull distribution. A plot of $ln(-ln(1 - F(t)))$ as a function of time in log scale is often referred as Weibull plot. β can be extracted from the slope of the Weibull plot. When $t = \eta$, the cumulative percentage of failure $F(t) = 1 - \exp(-(\frac{\eta}{\eta})^{\beta}) = 1 - 1/e = 63.2\%$, and the y-axis of Weibull plot $ln(-ln(1 - F(t))) = \beta ln(\eta) - \beta ln(\eta) = 0$. Therefore, η is the time at which 63% of the devices will fail and it equals to the time when the y-axis is zero on the Weibull plot.

Fig. 4 (a) shows the Weibull plot of ten measured TDDB failure times of vendor E'. The ten measured failure times are sorted with increasing order and the cumulative percentage of the these failure times are calculated using the median-

rank method as shown in eq. (5) to minimize systematic error caused by limited sample size [5], [6],

$$F(i) = \frac{i + 0.3}{n - 0.4} \tag{5}$$

where i is the ith sorted failure time and n is the sample size. From Fig. 4 (a) at $V_G = 45V$, $\beta = 12$ and $\eta = 0.35$ hours can be extracted. With these two parameters, the CDF at any given time can be constructed as shown by the dashed line in Fig. 4 (b). The constructed CDF agrees well with the ten measured failure times.

III. Results and Discussion

A. Gate Leakage Measurement Results

Figs. 6-8 show the gate leakage current measurements at 28°C, 175°C and 280°C for all three vendors. It can be observed in Fig. 6 that for vendor E', the leakage current maintained the same level from 28°C to 175°C and then increased from 175°C to 280°C. The breakdown voltage decreases as temperature is increased. These can be explained by reduction of effective barrier height and re-emission of electrons that are trapped at the interface at elevated temperatures as shown by process B in Fig. 5. Due to electron emission from the interface, threshold of the device under test (DUT) will decrease. Therefore, for a constant gate bias, the voltage drop across the gate oxide will increase and enhance F-N tunneling. Assuming that the critical electric field for dielectric breakdown stays constant at different temperatures, reduced gate voltage is needed to reach dielectric breakdown. Therefore, the breakdown voltage reduced from 28°C to 280°C.

Vendors C and D exhibit different gate leakage current behaviors as shown in Figs. 7 and 8. When the gate bias approached a certain voltage (crossover point), the leakage current at higher temperature decreased and became less than the leakage current at lower temperature. The behavior before the crossover point are similar to vendor E'. So the reduction of effective barrier height and electron re-emission from the interface traps are still taking place. However, with the presence of near interface oxide traps, more electrons can be injected into these oxide traps at elevated temperatures as shown by process C in Fig. 5. It can be shown from Gauss's Law that this process can relax the oxide electric field near the interface thus increase the barrier width and suppress F-N tunneling [7]. Furthermore, with the injected electrons into the oxide traps, the threshold voltages of the DUTs will increase. Therefore, in contrast to vendor E', the breakdown voltages of vendors C and D increased with elevated temperatures. These measurements show that the leakage current behavior at elevated temperatures is strongly related to interface traps and near interface oxide traps and it can be used as an indication of the quality of gate oxide.

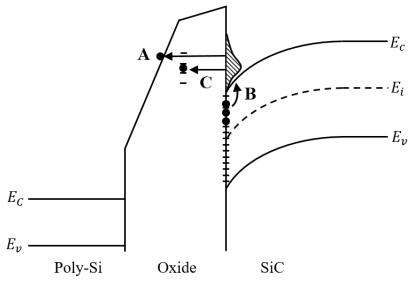

Fig. 5. Energy band diagram of a SiC MOSFET showing F-N tunneling (A), re-emission of electron from interface traps (B) and electron injection into the near interface oxide traps (C).

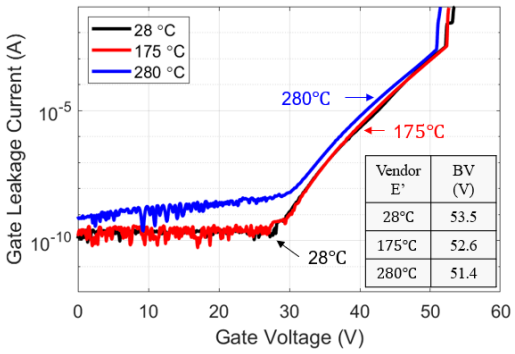

Fig. 6. Current-voltage characteristics for Vendor E' at three different temperatures (28°C, 175°C and 280°C)

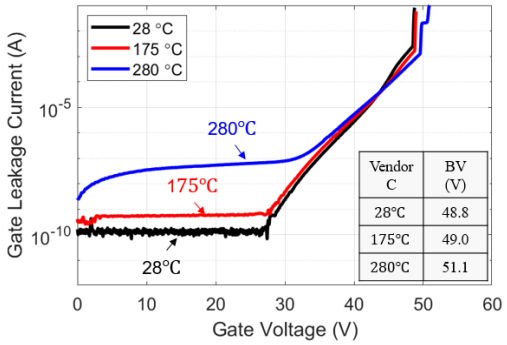

Fig. 7. Current-voltage characteristics for Vendor C at three different temperatures (28°C, 175°C and 280°C)

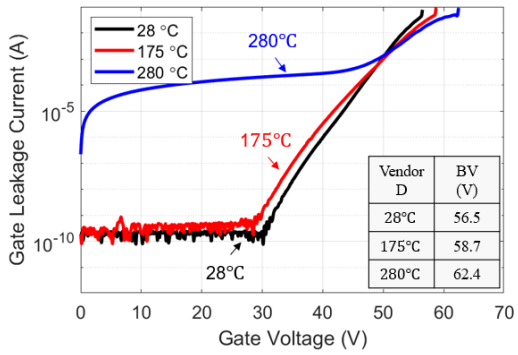

Fig. 8. Current-voltage characteristics for Vendor D at three different temperatures (28°C, 175°C and 280°C)

B. TDDB Measurement Results

A total of 80 commercial devices from vendor E' were characterized with constant-voltage TDDB measurements at 28°C and 175°C. At each temperature, four different gate voltages were applied. These gate voltages were selected so that the failure times are of the order of 10 minutes, 1 hour, 10 hours and 100 hours, respectively at 28°C. The Weibull distributions for both temperatures are shown in Figs. 9 and 10. When approximating the linear regression lines for the Weibull distribution, data points that fall significantly outside of the rest of the distribution were ignored. Despite the effort, variations of the slope parameter β can still be observed for both 28°C and 175°C. According to the percolation theory of dielectric breakdown, the slope parameter β is proportional to the oxide thickness and inverse of active area [8]. Therefore, the mismatch of oxide thickness might contribute to the variations of β. Percolation theory assumes that there is no pre-existing gate oxide defects. In practice, gate oxide defects exist before the stress is applied. These defects can introduce different failure modes and modify β values. Another potential cause for β variation is the threshold voltage difference for the commercial devices. For a given gate bias, with different threshold voltages, the gate oxide electric field will vary thus resulting in different failure times. Threshold voltage variations also indicate potentially different interface states and oxide defects distributions. This might cause the failure mode to change between devices and thus creating variations of the β values.

From the two distributions presented in Figs. 9 and 10, the 63% failure times ($t_{63\%}$) and slope parameter β at different gate voltages can be extracted. $t_{63\%}$ as a function of applied gate voltages at both 28°C and 175°C are plotted in Fig. 11. Assume that $log(t_{63\%})$ is linearly proportional to V_G as predicted by thermal-chemical E-model [9], the failure time at V_G = 20 V can be extracted by extrapolating back to the normal condition with a linear regression line. Once β and $t_{63\%}$ are extracted, the failure time at any given cumulative percentage of failure can be derived from Eq. (4) and it is given by:

$$t_{F\%} = t_{63\%} exp\Big\{\frac{1}{\beta} ln(-ln(1-F))\Big\}. \quad (6)$$

Failure times for other cumulative percentage of failures such as 1ppm (t_{1ppm}) are often used in automotive industry. t_{1ppm} at 175°C as a function of applied gate bias are also calculated and shown by the blue up-word triangles in Fig. 11. Extrapolation back to V_G = 20 V predicts t_{1ppm} at 175°C to be larger than 10^6 hours.

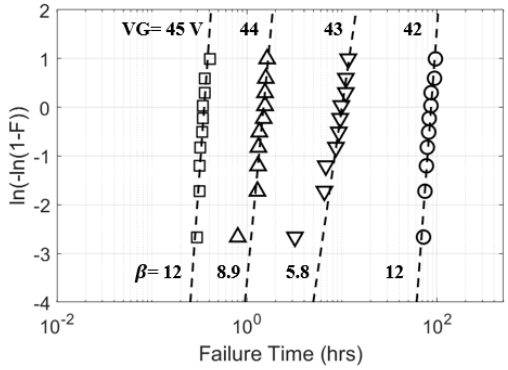

Fig. 9. Weibull distribution of vendor E' for four different gate voltages at 28°C.

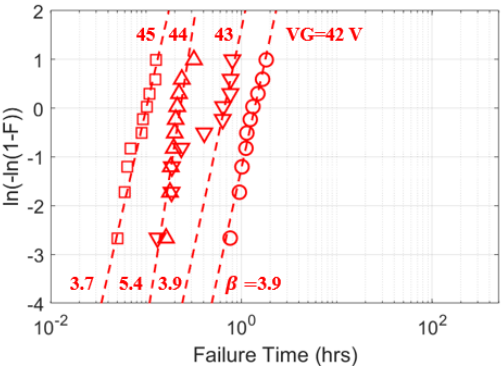

Fig. 10. Weibull distribution of vendor E' for four different gate voltages at 175°C.

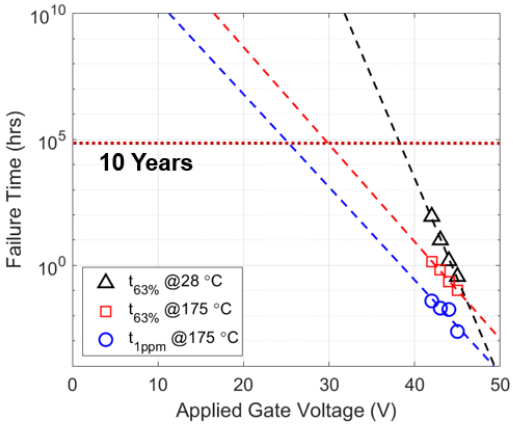

Fig. 11. Failure times, $t_{63\%}$ and t_{1ppm}, as a function of applied gate bias for vendor E' at 28°C and 175°C.

IV. Conclusion

Gate leakage current and time-dependent dielectric breakdown measurements were performed on commercial 1.2 kV 4H-SiC Power MOSFETs from several vendors. Gate leakage currents at normal operating condition (28°C and 20 V gate bias) showed values less than the noise floor (100 pA) for all three vendors. Anomalous gate leakage current behaviors that might be caused by high interface state density and near interface oxide trap were observed for vendors C and D. Therefore, the community should keep working on improving the oxide quality. TDDB measurement for vendor E' demonstrated that the predicted lifetime through extrapolation assuming a linear field-dependent model for 1ppm (t_{1ppm}) at 175°C is still larger than 10^6 hours.

Acknowledgments

This research is supported in part by the US Department of Energy (DOE) Vehicle Technologies Office (VTO) under the Electric Drive Train Consortium and the block gift grant from the II-VI Foundation. The authors would also like to thank the Power Electronics Teams at Ford Motor Company's Research and Innovation Center as well as at Sandia National Laboratories, for the helpful discussions.

References

[1] A. K. Agarwal, S. Seshadri, and L. B. Rowland, "Temperature dependence of Fowler-Nordheim current in 6H- and 4H-SiC MOS capacitors," *IEEE Electron Device Letters*, vol. 18, no. 12, pp. 592–594, 1997.

[2] K. Matocha, G. Dunne, S. Soloviev, and R. Beaupre, "Time-Dependent Dielectric Breakdown of 4H-SiC MOS Capacitors and DMOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1830–1834, 2008.

[3] D. J. Lichtenwalner, S. Sabri, E. V. Brunt, B. Hull, S. Ganguly, D. A. Gajewski, S. Allen, and J. W. Palmour, "Gate Oxide Reliability of SiC MOSFETs and Capacitors Fabricated on 150mm Wafers," *Materials Science Forum*, vol. 963, pp. 745–748, 2019.

[4] E. Wendler, A. Heft, and W. Wesch, "Ion-beam induced damage and annealing behaviour in SiC," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 141, no. 1-4, pp. 105–117, 1998.

[5] J. Fothergill, "Estimating the cumulative probability of failure data points to be plotted on Weibull and other probability paper," *IEEE Transactions on Electrical Insulation*, vol. 25, no. 3, pp. 489–492, 1990.

[6] J. Mcpherson, "Reliability Physics and Engineering," *New York: Springer*, 2010.

[7] S. J. Oh, Y. T. Yeow, "Voltage shifts of Fowler-Nordheim tunneling J-V plots in thin gate oxide MOS structures due to trapped charges," *Microelectronics Reliability*, vol. 30, no. 3, p. 626, 1990.

[8] J. H. Stathis, 1999, Percolation models for gate oxide breakdown, Journal of applied physics, 86(10), pp.5757-5766.

[9] J. W. McPherson, H. C. Mogul, 1998, Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO 2 thin films, Journal of Applied Physics 84, no. 3 (1998): 1513-1523.