Gate Oxide Reliability Studies of Commercial 1.2 kV 4H-SiC Power MOSFETs

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***Abstract*—This work examines the gate oxide ruggedness and underlying failure mechanisms of commercially available large-area 1.2 kV 4H-SiC power MOSFETs from multiple vendors. Both gate leakage current and time-dependent dielectric breakdown (TDDB) measurements are performed at various voltage stresses with temperatures between 28℃ and 175℃. While some vendors show promising gate oxide reliability results such as low gate leakage current (~100pA) and >10^6 hours lifetime at 175℃ with V_G=20 V, anomalous gate leakage current behaviors and TDDB characteristics are observed for other vendors. The anomalous gate oxide reliability measurement results are related to the pre-existing gate oxide defects and interface traps. Gate leakage current measurements at different temperatures reveal insights into the oxide quality. The authors also observe that constant-voltage TDDB measurement can greatly overestimate the oxide lifetime when a significant amount of extrinsic oxide defects exist before the measurements.**

***Index Terms*--Folwer-Nordheim (F-N) tunneling, Silicon Carbide (SiC) MOSFETs, oxide reliability, oxide defects, time-dependent dielectric breakdown (TDDB)**

I. INTRODUCTION

Due to superior properties such as wide bandgap, high breakdown electric field and high thermal conductivity [1], SiC MOSFETs are expected to be adopted soon in markets such as electric vehicles (EVs) and plug-in hybrid electric vehicles (PHEVs). For automotive applications, long term reliability is critical since device operational lifetimes are required to be longer than 10 to 20 years. Therefore, the ruggedness of 4H-SiC power MOSFETs has been extensively examined in recent years. Among the reliability concerns for SiC power MOSFETs [2]-[9], gate oxide reliability is the most critical issue [2]-[5].

Recently published gate oxide reliability results from CREE [2] shows extrapolated gate oxide lifetime at a gate voltage of 15 V is larger than 3x10^8 hours at 150℃ for their 1200 V 75$m\Omega$ Gen3 MOSFET (C3M0075120D). Monolith/Littlefuse also demonstrates more than 100 years of lifetime at normal operating conditions at 175℃ and 225℃ for their 1200 V 80$m\Omega$ planar MOSFETs in [3]. Comparing to the early gate oxide reliability studies in [10]-[12], significant advancement has been made over the last two decades in enhancing the gate oxide reliability. In this work, the current gate oxide reliability status of packaged commercial 1.2 kV SiC power MOSFETs is investigated for multiple vendors.

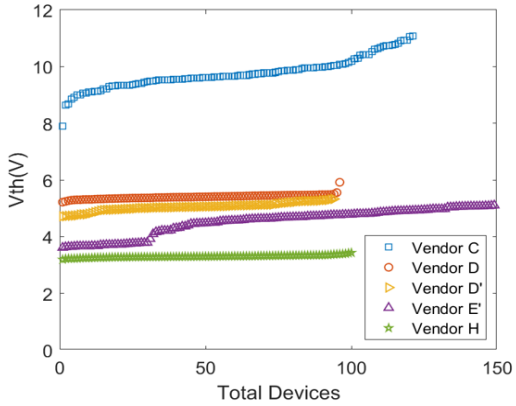

Figure 1. Threshold pretest results for all vendors.

II. EXPERIMENTAL METHODS

Table I shows the general information of all the tested commercial power MOSFETs in this work. All purchased commercial MOSFETs were divided into groups of ten devices to capture the statistical behaviors of gate leakage currents and dielectric breakdowns. Before any gate oxide reliability measurements, the threshold voltages of all devices were pretested with a linear extrapolation method at $V_{DS} = 0.1$ V [13]. These devices were then carefully selected to ensure the threshold voltage variation among each group was less than 0.1 V. This procedure minimizes the variations of the voltages across the gate oxide when the same gate bias is applied to all devices under test (DUTs). Sorted threshold values for all vendors are shown in Fig. 1. A significant amount of threshold voltage variation is observed for vendor C.

TABLE I GENERAL INFORMATION FOR TESTED COMMERCIAL SIC DEVICES.

Vendors	*Type of MOSFET*	*Current Ratings*	*Typical Vth*	*Typical $R_{ds,on}$*	*Estimated T_{ox}*
C	Planar	12 A	9.5 V	680 mΩ	50 nm
D	Trench	17 A	5.5 V	150 mΩ	50 nm
D'	Planar	10 A	5 V	410 mΩ	50 nm
E'	Planar	10 A	4.5 V	380 mΩ	45 nm
H	Planar	20 A	3.5 V	60 mΩ	40 nm

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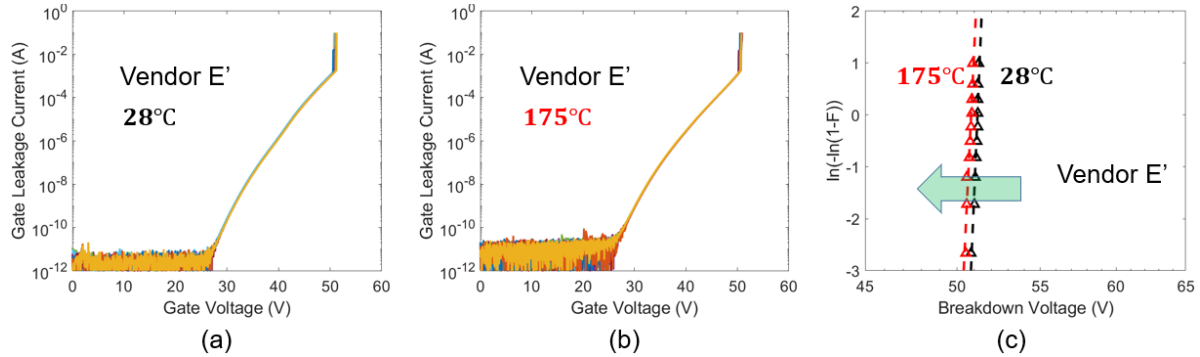

Figure 2. Gate leakage current of 10 vendor E' devices (a) at 28℃, (b) at 175℃, and (c) comparison of the breakdown distributions at two temperatures.

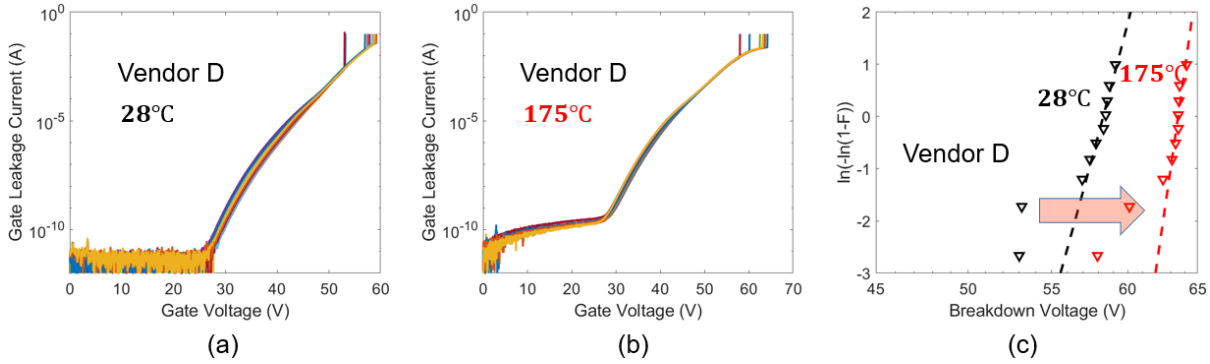

Figure 3. Gate leakage current of 10 vendor D devices (a) at 28℃, (b) at 175℃, and (c) comparison of the breakdown distributions at two temperatures.

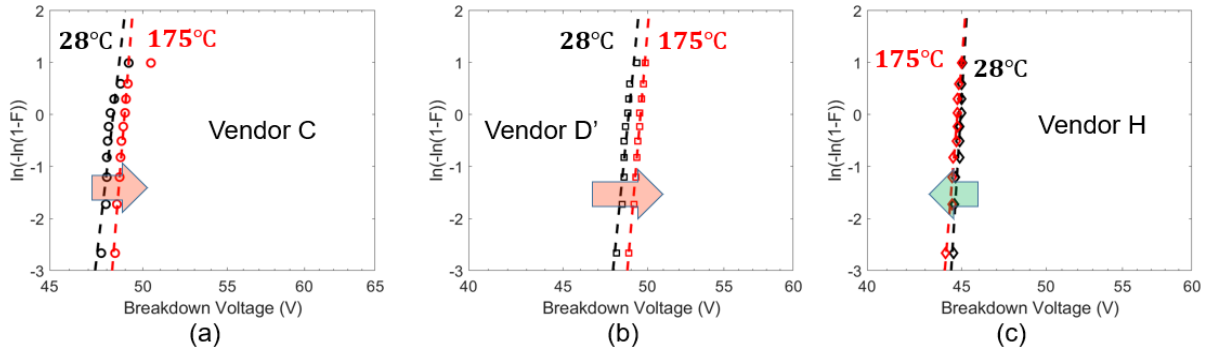

Figure 4. Comparisons of breakdown distributions between 28℃ and 175℃ for (a) vendor C, (b) vendor D', and (c) vendor H.

This variation of threshold values within each vendor can be caused by non-uniform distributions of oxide charges and trapped interface charges which indicate different gate oxide qualities. The unexpectedly large threshold values for vendor C also suggest high interface trap densities.

A packaged commercial MOSFET was placed into an oven with its source and drain electrodes shorted to the ground during the gate leakage current measurement. A gate voltage sweep was applied through a curve tracer (B1505A) to the gate electrode of the device, and the gate leakage current was measured until dielectric breakdown. Constant-voltage TDDB measurements were performed at temperatures between 28°C and 175°C and gate voltage biases between 40 V to 55 V. During TDDB experiments, a constant gate voltage was applied to all 10 gate electrodes of DUTs with their source and drain electrodes connected to the ground. The failure times were measured with a 10-channel digital multi-meter (DMM 6500) then analyzed with Weibull statistics [14].

III. Gate Leakage Current Measurement

Gate leakage current measurements at both 28°C and 175°C for vendor E' and D are shown in Figs. 2 and 3, respectively. The breakdown voltages are extracted and fitted with Weibull distribution. Comparing between two vendors, vendor E' shows fewer variations at both 28°C and 175°C. Uniformity of vendor E' leakage results, especially in the F-N tunneling regime, is an indication of uniform distribution of oxide thickness across all DUTs. It also suggests that F-N tunneling is dominant and other processes such as Trap-Assisted Tunneling (TAT) are negligible. This reflects mature and reliable process control for

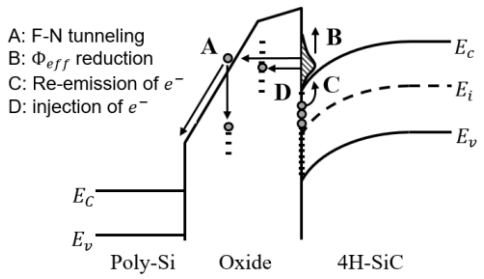

Figure 5. Energy band diagram illustrating four possible mechanisms during the gate leakage current measurements: F-N tunneling and potential subsequent trapping of electrons into deep oxide traps (process A), effective barrier height reduction at elevated temperature (process B), re-emission of trapped electrons at elevated temperature (process C), and injection of electrons into near interface oxide traps (process D).

vendor E'. The breakdown voltage distribution for vendor E' decreases at a higher temperature. This can be explained with additional processes besides F-N tunneling (process A) that can happen during the measurement as illustrated by the energy band diagram in Fig. 5.

Reduction of effective barrier height at elevated temperature (process B) can increase the gate leakage current with the same gate voltage bias. Consequently, the breakdown voltage decreases because less gate voltage is needed to accumulate the critical amount of charge for dielectric breakdown [15]. Electrons that are trapped at the interface re-emits at a higher temperature (process C). Due to process C, the threshold voltage of the DUT decreases. Therefore, for a constant gate bias, the voltage drop across the gate oxide will increase and enhance the oxide electric field. If the critical electric field for dielectric breakdown stays constant at different temperatures, a reduced gate voltage is enough to reach the dielectric breakdown. Thus, both processes B and C reduce the breakdown voltage. Opposite to process C, electron injections into the near interface oxide traps (process D) increase the threshold of the DUTs and relax the electric field near the SiC/SiO2 interface [16]. With increased threshold voltage and relaxed oxide electric field, a higher gate voltage needs to be applied to reach a given breakdown electric field. Hence, process D increases the breakdown voltage. For vendor E', processes B and C are dominant over D so that the breakdown voltage decreases at a higher temperature.

Noticeable variations of the F-N tunneling characteristics and spread-out breakdown voltage distributions on the Weibull plot is observed for vendor D in Fig. 3 (c). This indicates that vendor D deviates more from the intrinsic gate oxide quality comparing to vendor E'. This can be confirmed with the breakdown voltage increase at a high temperature because it is evidence of significant electron injections into the near oxide interface traps. Therefore, the gate leakage current behavior at a high temperature can be used as an indication of gate oxide quality.

Breakdown distribution changes from 28℃ to 175℃ for vendors C, D', and H are summarized in Fig. 4. Gate leakage current results are not included for these vendors. However, the uniformity of their gate leakage current results is reflected in the tight breakdown voltage distributions on the Weibull plot. Vendor H shows a similar breakdown voltage decrease as vendor E' suggesting comparable gate oxide quality. The breakdown voltages increase at a higher temperature for vendor C and D'. It is worth noting that vendor D devices demonstrate a larger shift and more variations of breakdown voltages on the Weibull plot comparing to vendors C and D'. This suggests that trench MOSFETs tend to have more pre-existing gate oxide defects than planar MOSFETs. Measured high threshold values for vendor C devices in Fig. 1 implies significant interface traps. Therefore, the relatively small breakdown voltage increase for vendor C can be caused by large numbers of re-emissions of trapped electrons from the interface at elevated temperature (process C) which considerably cancels the injection of electrons (process D).

IV. Time-Dependent Dielectric Breakdown Measurement

The failure times of TDDB measurements are analyzed with Weibull distribution which is described by:

$$F(t) = 1 - \exp\left(-\left(\frac{t}{t_{63\%}}\right)^{\beta}\right) \quad (1)$$

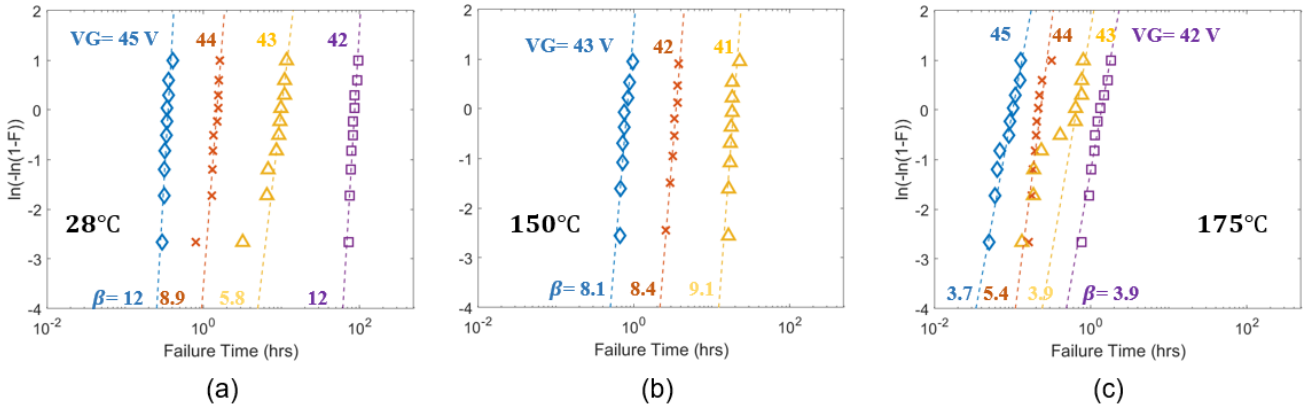

Figure 6. Weibull distributions for vendor E' (a) at 28℃ with gate biases of 42, 43, 44, and 45 V, (b) at 150℃ with gate biases of 41, 42, and 43 V, and (c) at 175℃ with gate biases of 42, 43, 44, and 45 V.

where F(t) is the cumulative percentage of failures at a given stress time, $t_{63\%}$ is the characteristic lifetime (the time that 63% of the population will fail) and β is the slope parameter for Weibull distribution. β is an indication of the gate oxide quality. Less variation of the failure times produce a larger β value and suggests fewer degradations from the intrinsic gate oxide quality [12]. Therefore, a tighter distribution of failure times on the Weibull plot implies better gate oxide quality.

A total of 110 vendor E' devices are divided into 11 groups of 10 devices and the complete TDDB results between 28℃ and 175 ℃ are shown in Fig. 6. Obvious extrinsic failures are ignored when extracting the slope parameter β. It can be observed that at higher temperatures, failure times at all gate biases are shorten as expected. From the Weibull distributions, $t_{63\%}$ for different gate biases at different temperatures are extracted and plotted in Fig. 7. Prediction of the lifetime under normal operating conditions ($V_G = 20\ V$ at 150℃) is made by extrapolating linearly from the much-accelerated experimental conditions. This method is based on a conservative dielectric breakdown model called thermal-chemical E-model [17], [18]. Extrapolating back to V_G=20 V at 150℃, the predicted lifetime without considering the extrinsic failures is much higher than the targeted 10-20 years that is typically used as a standard for the automotive industry.

TDDB results for vendor C at 28℃ with three different gate biases are shown in Fig. 8. Compared with the results for vendor E', vendor C demonstrates notably wider variations of failure times for given gate biases. For all three gate biases, the results

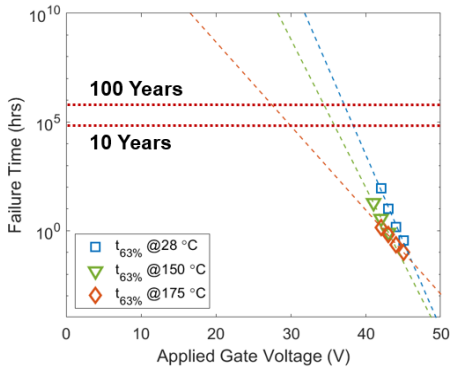

Figure 7. Failure times as a function of applied gate voltage for vendor E' at 28℃, 150℃, and 175℃.

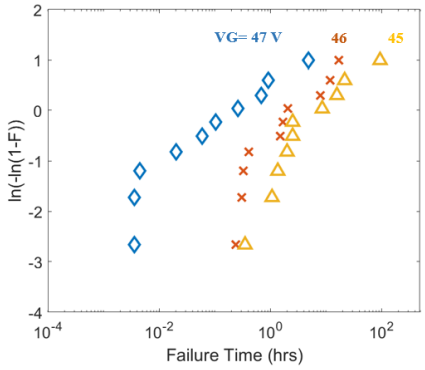

Figure 8. Weibull distributions for vendor C at 28℃ with gate biases of 45, 46, and 47 V.

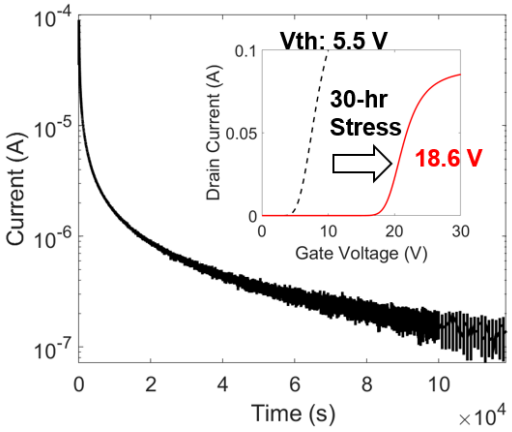

Figure 9. Gate leakage current as a function of time (up up to 30 hours) with a constant voltage stress of 53 V for one vendor D device at room temperature. Inset shows the threshold voltage change before and after the long-term stress.

do not show any intrinsic region and seem to suggest different failure modes for each gate bias. This notable amount of variations of the measured lifetime makes it impossible to predict the lifetime under a normal operating condition with any reasonable uncertainty level. Lifetime variations for vendor C link to its threshold voltage variations since both are caused by non-uniform distribution of the high amount of interface traps and oxide defects.

During the TDDB measurement for vendor D, it was observed that even with an applied gate voltage close to the breakdown voltage, the DUTs still survived after a surprisingly long amount of stress time. To investigate this phenomenon, vendor D devices were stressed with a gate bias of 53 V (~2 V below its mean breakdown voltage) for 30 hours, and the gate leakage current a function of time for one vendor D device was plotted in Fig. 9. The leakage current rapidly reduced right after the stress was applied and continued to gradually decrease throughout the stress. This leakage current decrease strongly suggests that a significant number of electrons were injected into the near interface oxide traps and into the conduction band of oxide then subsequently captured by traps distributed deeper into the gate oxide. These are the same mechanisms as the previously discussed processes D and A (with subsequent capture). They can relax the gate oxide field and increase the threshold of the DUT. The inset of Fig. 9 shows around 13 V threshold voltage shift after the stress which agrees with the assumption. Similar threshold voltage shifts after applied gate voltage stress for several commercial SiC MOSFETs are also published in [19]. Degradation of carrier mobility at higher gate voltage bias can be also observed from the collapsed drain current versus gate voltage curve after stress. This indicates increased surface scattering due to both trappings at the interface and electron injection into near interface oxide traps. Therefore, TDDB lifetime can be noticeably prolonged when the gate leakage current is reduced by the significant amount of injection of electrons into the near interface oxide traps as mentioned by K. Okada, et al. in [4]. ***For devices with a higher amount of gate oxide traps like vendor D devices, extrapolation of TDBD results will overestimate the lifetime prediction at normal operating conditions.***

V. CONCLUSION

Both gate leakage current and time-dependent dielectric breakdown measurements are performed on commercial 1.2 kV 4H-SiC Power MOSFETs from several vendors. Gate leakage currents are found to be less than 1 nA at 175℃ with V_G=20 V for all vendors. TDDB measurement for vendor E' predicts that the $t_{63\%}$ lifetime at 150℃ with V_G=20 V is significantly higher than 10^6 hours if extrinsic failures are neglected. Besides the encouraging oxide reliability results, anomalous gate leakage current results and TDDB characteristics are observed for multiple vendors. The breakdown voltage increase at elevated temperature is associated with the dominance of electron injections into near interface oxide traps. Therefore, breakdown voltage behavior at high temperatures can be used as an indication of oxide defects near the interface. Anomalous TDDB measurements were observed for vendor C and D. Variation of the measured lifetimes for vendor C makes it unreliable to predict the lifetime under normal condition through extrapolation. Lifetimes for vendor D devices were prolonged due to the threshold voltage increase and oxide electric field relaxation caused by electron injections into oxide traps. Thus, lifetime predicted through constant-voltage TDDB can be greatly overestimated if a substantial number of traps exist in the gate oxide. Consequently, the community should keep working on improving the gate oxide quality.

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