Impacts of Area-Dependent Defects on the Yield and Gate Oxide Reliability of SiC Power MOSFETs

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***Abstract*—Large area SiC power metal-oxide-semiconductor field-effect- transistors (MOSFETs) with a $150\,\mathrm{A}$-$200\,\mathrm{A}$ or higher current rating are desired by the fast-growing electric vehicles (EVs) market. However, the reliability and yield of large area MOSFETs are limited by the crystal defects in the epitaxial layers. Yield analyses are applied to defect maps of 6-inch commercial SiC n-type wafers. The results show that the defect density needs to be reduced to lower than $0.2\,\mathrm{cm}^{-2}$ to obtain more than 80% yield for the $200\,\mathrm{A}$ SiC power MOSFETs. Defects with significant surface morphology also affect the long-term oxide reliability of the devices. Therefore, time-dependent dielectric breakdown (TDDB) measurements are conducted on commercially available SiC power MOSFETs with different current ratings (different chip areas). Degradation of oxide lifetime prediction and more spread-out oxide failure times are observed for the larger commercial power MOSFETs.**

***Index Terms*—Silicon carbide (SiC), power MOSFET, area-dependent defects, oxide reliability, yield, time-dependent dielectric breakdown (TDDB).**

I. Introduction

Silicon carbide (SiC) power devices such as Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect-transistors (MOSFETs) have been receiving increasing attention in high-power and high-voltage applications [1]. In particular, SiC power MOSFETs are being utilized in the fast-growing electric vehicles (EVs) market. A midsize electric sedan requires approximately $100\,\mathrm{kW}$ peak power from the traction inverter to drive the electric motor. A $400\,\mathrm{V}$ bus voltage silicon-based EV inverter module typically consists of three $750\,\mathrm{V}$, $150\,\mathrm{A}$ insulated-gate bipolar transistors (IGBTs) [2]. These power devices with higher current ratings (larger device sizes) are desired since they reduce the number of parallel devices inside the module, lower system cost, and improve system reliability. Therefore, SiC power MOSFETs with $150\,\mathrm{A}$ to $200\,\mathrm{A}$ currents are desired to better compete with silicon IGBTs.

A $200\,\mathrm{A}$ SiC power MOSFET requires an active area of $1\,\mathrm{cm}^2$ (estimated with a current density of $200\,\mathrm{A\,cm}^{-2}$). However, the reliability and yield of such MOSFETs are limited by the crystal defects in the epitaxial layers that originate from the substrate during the epitaxial growth, or added during the device processing steps [3]. During the past decades, extensive studies have been conducted to understand the impact of major SiC defects [1], [4]–[6]. Defects such as micropipes, particle and polytype inclusions, and large surface morphological defects are considered to be device-killing defects or killer defects since they kill or severely damage the electrical properties of the devices. Other non-killer defects such as basal plane dislocations (BPD) and threading edge dislocations (TED) might not kill the electrical properties of the devices but can cause performance degradation and excessive leakage current [7], [8]. Defects with significant surface morphology also alter the uniform distribution of the oxide electric field and create local peak electric field, affect the long-term oxide reliability of the devices, and cause premature failure [3], [9]. These defects are area-dependent. Therefore, SiC power MOSFETs with larger device areas are more susceptible to the influences of these defects.

This work studies how the yield and oxide reliability of large area SiC power MOSFETs are affected by the area-dependent defects. Defect maps containing three major killer defects for multiple 6-inch commercial SiC wafers are investigated. The relationship between yield and chip area is presented under different defect densities. Time-dependent dielectric breakdown (TDDB) measurements of commercially available SiC power MOSFETs with different current ratings (different chip areas) are conducted to investigate if the gate oxide reliability degrades with larger chip area.

II. Experimental

Essential information of the tested commercial SiC power MOSFETs are listed in Table. I. The transfer, output, and gate oxide breakdown characteristics of all the commercial devices are characterized by a semiconductor parameter analyzer (B1505A, Keysight, Inc). The threshold voltages of the MOSFETs are extracted with the linear extrapolation method at $\mathrm{V_{DS}} = 0.1\,\mathrm{V}$ at room temperature. The oxide thicknesses are estimated from the extracted oxide breakdown voltages at 150°C, assuming a critical oxide breakdown electric field of $11\,\mathrm{MV\,cm}^{-1}$ [10], [11]. The TDDB measurement are conducted with the experimental method detailed in [10], [12], [13].

TABLE I
Tested Commercial 1200 V 4H-SiC Power MOSFETs

MOSFETs	Type	Typical ON-resistance	Oxide Thickness	Typical Threshold
E-300	Planar	300 $m\Omega$	46 nm	4.5 V
E-25	Planar	25 $m\Omega$	46 nm	4.7 V

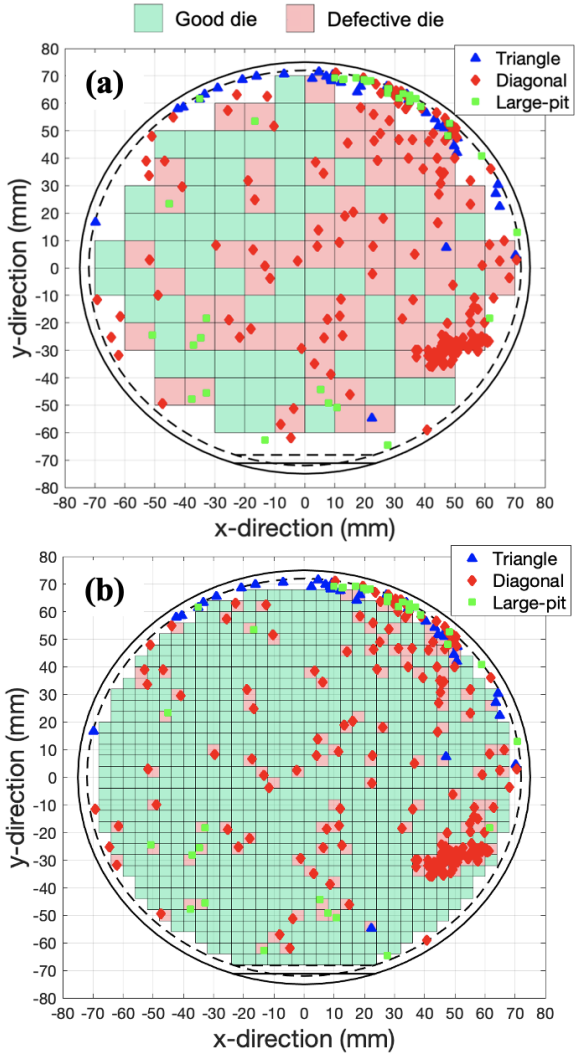

Fig. 1. Simulated wafer maps with die areas of (a) $10\,\mathrm{mm} \times 10\,\mathrm{mm}$ and (b) $4\,\mathrm{mm} \times 4\,\mathrm{mm}$. The total defect density for this wafer is $1.69\,\mathrm{cm}^{-2}$. The simulated yields are 49% and 87%, respectively.

III. Results and Discussions

This section discusses how the yield of large area SiC power MOSFET is affected by the densities of SiC defects on the epitaxial wafers. In addition, TDDB measurements are conducted for commercial SiC power MOSFETs with different current ratings to investigate if the gate oxide reliability deteriorates with a large device size.

A. Defects and Yield

Sixteen defect maps for 6-inch commercial n-type SiC epitaxial wafers are obtained with the Lasertec SICA platform that is capable of both surface and photoluminescence (PL) inspections. Three device-killing surface defects (triangle defect, diagonal defect, and large pit) are identified. The total defect densities vary from $0.1\,\mathrm{cm}^{-2}$ to $1.69\,\mathrm{cm}^{-2}$ across all wafers. The authors developed a MATLAB script to simulate and extract the die yield with arbitrary die size for all defect maps. The MATLAB script treats a die as defective if one or more defects are inside the die since these defects are all killer

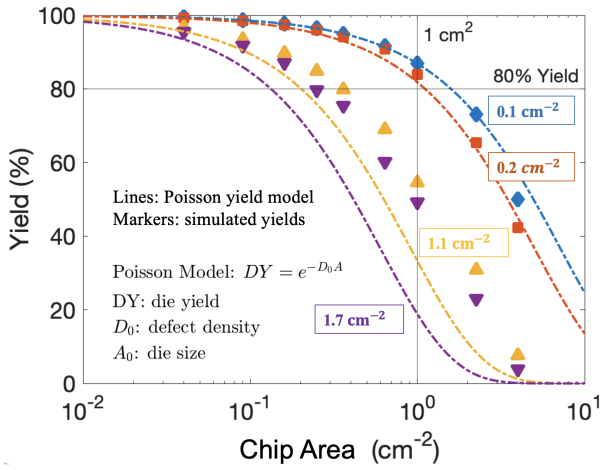

Fig. 2. Simulated yields (markers) and die yield vs. die area curves based on Poison yield model (lines) with different defect densities.

defects. Fig. 1 shows the simulated wafer maps with die areas of $10\,\mathrm{mm} \times 10\,\mathrm{mm}$ and $4\,\mathrm{mm} \times 4\,\mathrm{mm}$. The extracted yields are 49% and 87%, respectively, for the two different die sizes.

The Poisson yield model is the most commonly used yield model, and it is described as

$$DY = e^{-D_0 A}, \tag{1}$$

where DY is the die yield, D_0 is the number of defects per unit area, and A is the die area. The MATLAB script is applied to all wafer maps with various die areas, and the simulated yields for four selected wafers are plotted in Fig. 2 (markers). The yields predicted by the Poisson yield model are also calculated at the respective defect densities and included in the same figure (lines in Fig. 2). The Poisson yield model underestimates the yield with large defect densities and large die sizes due to the clustering of the defects inside the wafers and near the edge. The development of a more accurate yield model that considers the clustering of defects is outside the scope of this work. However, the Poisson yield model fits well with the wafer maps that have smaller defect densities ($0.1\,\mathrm{cm}^{-2}$ and $0.2\,\mathrm{cm}^{-2}$ in Fig. 2). According to the results, the defect density needs to be lower than $0.2\,\mathrm{cm}^{-2}$ to have more than 80% yield for the desired 200 A (chip area=$1\,\mathrm{cm}^2$) SiC power MOSFETs. It is important to note that this yield is estimated with only three types of defects. The actual yield of the 200 A SiC power MOSFETs could be lower due to additional defects and other yield losses during device fabrication.

The authors are also doing in-depth structural analyses to investigate the surface morphology of major SiC defects. The surface morphology results and their impacts on the long-term oxide reliability of SiC power MOSFETs will be published in a future communication.

B. TDDB with Different Active Areas

TDDB measurements have been conducted on two types of vendor E MOSFETs with over ten times difference in ON-resistance to check if the gate oxide reliability degrades with

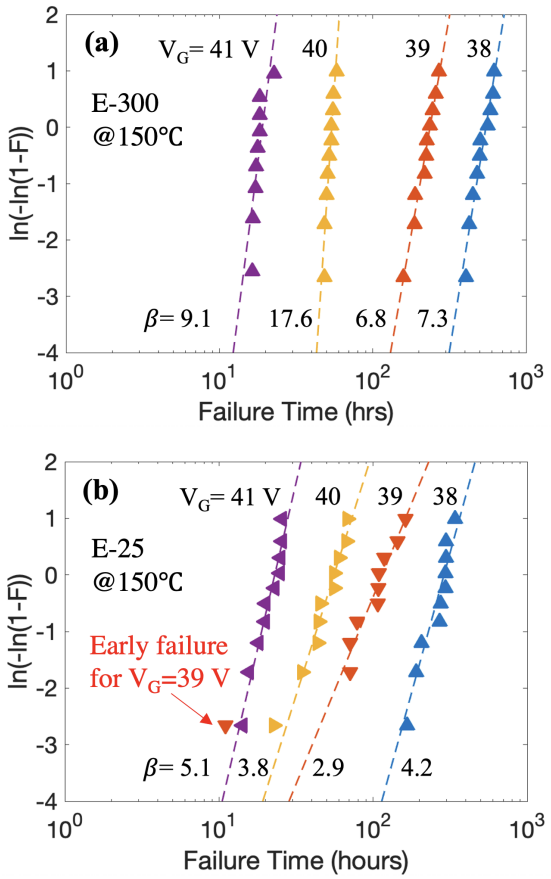

Fig. 3. Weibull distributions of measured lifetimes ($t_{63\%}$) at 150°C with different gate voltage stresses for (a) E-300 and (b) E-25.

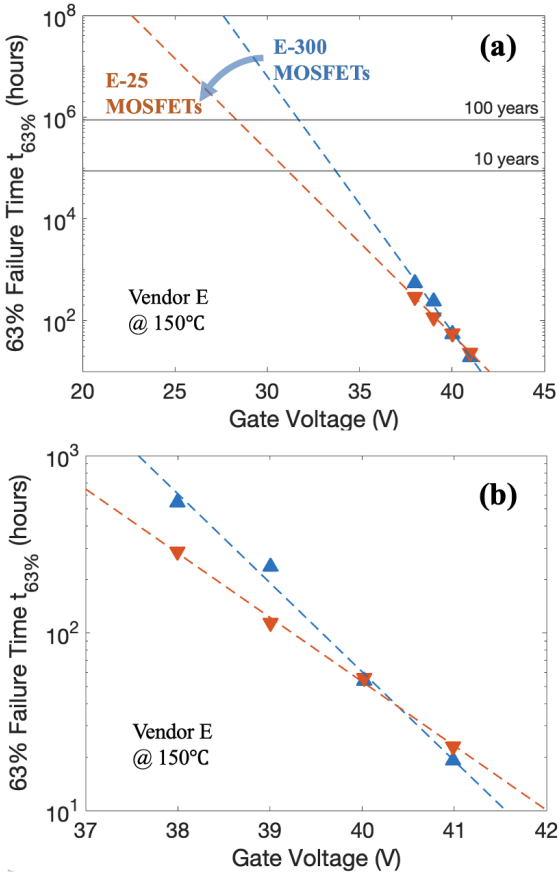

Fig. 4. (a) $t_{63\%}$ vs. gate voltage at 150°C for the two types of vendor E MOSFETs. (b) Enhanced view of the measured failure times.

large MOSFETs. Our previous study [10] shows that TDDB measurements need to be performed at lower oxide electric fields to avoid inaccurate lifetime prediction caused by impact ionization at high oxide electric fields. Therefore, the TDDB measurements in this study are all done at oxide electric fields lower than $9\,\mathrm{MV\,cm^{-1}}$ to ensure accurate lifetime predictions. Since these are commercial devices, it is assumed that a gate oxide screen has already been performed by the manufacture to screen out majority of the devices with extrinsic defects. However, some of the extrinsic defects may have not been screened out.

The measured oxide failure times are analyzed with Weibull distribution and shown in Fig. 3. Weibull distribution is expressed as

$$F(t) = 1 - e^{-(t/t_{63\%})^{\beta}}, \tag{2}$$

where $F(t)$ is the cumulative percentage of failures, $t_{63\%}$ is the time that 63.2% of the sample population fails, and β is the Weibull slope parameter. Less variation in the failure times produces larger β and suggests better gate oxide uniformity. Therefore, for a given set of failure times, a larger β and a larger $t_{63\%}$ are desirable. The β of the two types of MOSFETs are extracted and annotated in Fig. 3. The β of E-25 MOSFETs are much smaller than the E-300 MOSFETs, reflecting more variations of the oxide failure times for the larger MOSFETs. The area-dependent β indicates that oxide reliability degrades with larger MOSFETs since the percolation model predicts that the β of an intrinsic oxide is independent of oxide area [14].

The oxide lifetime ($t_{63\%}$) versus gate voltage results are plotted in Fig. 4. Although the predicted lifetimes for both types of MOSFETs at 20 V gate voltage are above 100 years, degradation of lifetime prediction is observed for E-25 MOSFETs. The authors are studying the underlying reasons for the lifetime degradation and also conducting TDDB measurements with even larger MOSFETs from the same vendor to check if the degradation trend continues with higher current ratings.

It is also important to point out that failure times for much lower cumulative percentage of failures such as 100 ppm (t_{100ppm}) are often the criteria for the automotive industry. The failure time at any given cumulative percentage of failure can be calculated with

$$t_{F\%} = t_{63\%} exp\Big\{\frac{1}{\beta} ln(-ln(1-F))\Big\}, \tag{3}$$

where $t_{F\%}$ is the failure time at any given cumulative percentage of failure. With an average β of 4 for the E-25 MOSFETs, the 100 ppm failure time is expected to be one order of magnitude lower than the $t_{63\%}$. Therefore, the lifetime prediction can be further reduced if the criteria for the percentage of failure is lowered.

IV. Conclusion

Analyses on the wafer maps also show that the yield of large area SiC power MOSFETs is strongly limited by the density of the device-killing defects. The surface defect densities need to be reduced to lower than $0.2\,\mathrm{cm}^{-2}$ to have at least 80% yield for the desired $200\,\mathrm{A}$ SiC MOSFETs. TDDB measurements have been conducted on commercial SiC power MOSFETs with different current ratings. Degradation of the oxide lifetime prediction and more spread-out oxide failure times are observed for the MOSFETs with a larger current rating (E-25).

Acknowledgments

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