Investigation of Gate Leakage Current Behavior for Commercial 1.2 kV 4H-SiC Power MOSFETs

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2021 IEEE International Reliability Physics Symposium (IRPS) | 978-1-7281-6893-7/21/$31.00 ©2021 IEEE | DOI: 10.1109/IRPS46558.2021.9405230

***Abstract*—The commercialization of silicon carbide (SiC) power metal-oxide-semiconductor field-effect-transistors (MOSFETs) has expanded during the last decade. The gate oxide reliability is the primary issue for SiC power MOSFETs since it determines the device's operational lifetime. In this work, we investigate the gate leakage currents under different gate voltages on commercial 1.2 kV SiC power MOSFETs. The impact ionization and/or anode hole injection (AHI) triggered by high oxide electric fields results in hole trapping that enhances the gate leakage current and reduces device's threshold voltage. The electron injection and trapping due to Fowler-Nordheim (F-N) tunneling tend to reduce the gate leakage current and increases threshold voltage. Constant-voltage time-dependent dielectric breakdown (TDDB) measurements are also conducted on the commercial MOSFETs. The results on gate leakage current suggest that the change of the field acceleration factor is due to enhanced gate current/hole trapping under high gate oxide fields. Therefore, it is suggested that TDDB measurements should be conducted under low gate voltages to avoid overestimation of lifetime under normal operating gate voltage.**

***Index Terms*—SiC MOSFET, gate leakage current, hole and electron trapping, impact ionization, TDDB.**

I. Introduction

Due to the excellent material properties of silicon carbide (SiC), SiC power devices have been widely developed during the past decades to replace silicon (Si) power devices in high voltage and high power applications [1]. Reliability issues, such as gate-oxide reliability [2]–[5], threshold-voltage instability [6]–[8], short-circuit ruggedness [9]–[11] and body-diode degradation [12], [13], of SiC power metal-oxide-semiconductor field-effect-transistors (MOSFETs) have been investigated for the past few years. Among these reliability issues, the gate oxide reliability of SiC power MOSFETs is a primary concern since the gate oxide quality determines the operational lifetime of the SiC power MOSFETs.

The SiO_2 layer grown on SiC has abundant extrinsic defects [14], [15], which may accelerate the degradation of the gate oxide and cause early failure [4]. Chbili et al. propose a lucky defect model to explain the extrinsic failures of SiC/SiO_2 gate oxide. The lucky defect model for oxide time-to-breakdown is closely associated with the gate current flowing through the oxide during constant electric field stress. The measured gate leakage current under oxide electric field of 9 MV/cm at 150°C exhibits three phases [16]. In phase I, the current increases due to impact ionization induced hole trapping. Then, in phase II, the current decreases because of the negative charge trapping. In phase III, the current increases rapidly and the device breaks down. The same gate leakage current behavior is observed by Moens et al. [5]. The increase and decrease of gate current are explained by positive and negative charge build-up. The difference is that Moens et al. attribute the positive charges to anode hole injection (AHI) [17], [18] and the negative charge build-up to thermally assisted tunneling (TAT). Based on the analysis, a charge-to-breakdown approach is developed to extract the SiC/SiO_2 dielectric lifetime [5].

Constant-voltage time-dependent dielectric breakdown (TDDB) measurements [3], [19]–[22] are commonly applied to examine the oxide lifetime for SiC power MOSFETs. TDDB results in [19], [22] display an abrupt change of the failure acceleration factor under different gate voltages that leads to the overestimation of the device normal operating lifetime. The higher failure acceleration factor under higher gate voltages implies an enhanced oxide degradation rate. With increased gate leakage current, the wear-out of gate oxide is accelerated. Consequently, the lifetime of the gate oxide is shorter [4], [16].

In this paper, we monitor the gate leakage currents and threshold voltage variations under different gate voltages for commercial 1.2 kV 4H-SiC power MOSFETs. The gate leakage current behaviors reveal that the trapping of holes introduced by impact ionization and/or AHI and trapping of electrons injected by Fowler-Nordheim (F-N) injection happen simultaneously under various gate oxide electric fields. The analysis of gate leakage currents reveals insights into different failure mechanisms under different oxide electric fields and provides support to the statement that constant voltage TDDB measurements should be conducted under lower gate oxide electrical fields.

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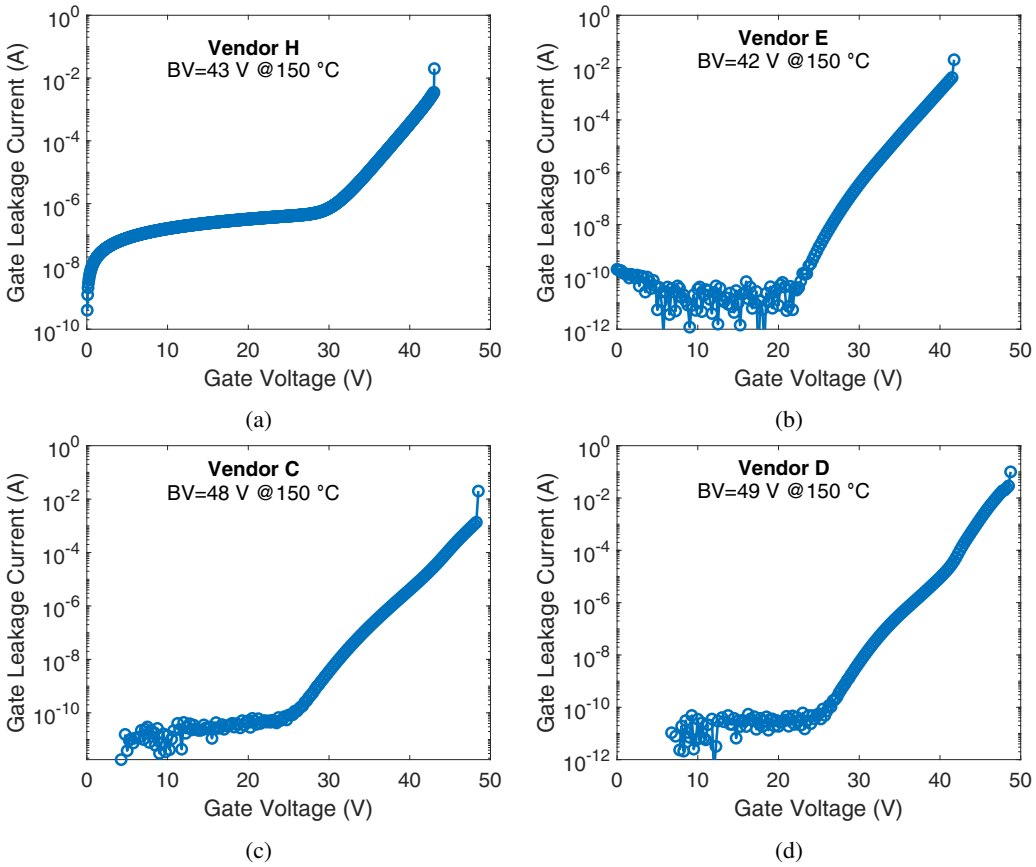


Fig. 1: Ramped-voltage breakdown measurement results for commercial SiC power MOSFETs from (a) vendor H, (b) vendor E, (c) vendor C, and (d) vendor D.

II. Experimental Method

The commercial 1.2 kV 4H-SiC power MOSFETs (packaged in TO-247) from four vendors are tested in this work. The general characteristics of the devices are listed in Table I. The threshold voltages for those devices are extrapolated using the linear extrapolation method [23], [24] at $V_{DS} = 100\,\mathrm{mV}$.

The ramped-voltage breakdown measurements are conducted on devices from vendors H, E, C, and D using the method described in [22], [25]. The results are shown in Fig. 1. The gate oxide breakdown voltage for vendor H [Fig. 1(a)] is extracted to be 43 V at 150°C. This being a commercial device, the gate oxide thickness is unknown. Assuming the dielectric breakdown field is 10 MV/cm to 11.5 MV/cm, the oxide thickness for vendor H ranges from 37 nm to 43 nm.

TABLE I: Information for Tested Commercial SiC MOSFETs

Vendor	Voltage Ratings	Current Ratings	Vth Voltage Range	Oxide Breakdown Voltage	Estimated Oxide Thickness
H	1200 V	40 A	4.62∼4.77 V	43 V	40 nm
E	1200 V	30 A	4.96∼5.02 V	42 V	39 nm
C	1200 V	12 A	11.3∼12.2 V	48 V	45 nm
D	1200 V	10 A	6.00∼6.05 V	49 V	46 nm

Thus, the average value (40 nm) of the oxide thickness is used to estimate the oxide field for the commercial SiC MOSFET from vendor H. This assumption will subject our electric field estimates in the dielectric by a maximum error of +/- 7.5%. Similarly, for vendor E [Fig. 1(b)], vendor C [Fig. 1(c)] and vendor D [Fig. 1(d)], the gate oxide breakdown voltage and thickness are evaluated and listed in Table I.

The gate leakage currents for the packaged (TO-247) commercial SiC power MOSFETs are examined by applying various constant voltages to the gate terminals while the drain and source terminals are grounded. The gate voltages are chosen based on the gate oxide breakdown voltages so that the oxide electric fields range from around $10\,\mathrm{MV/cm}$ to around $8\,\mathrm{MV/cm}$. A source/measurement unit (Keysight B2901A) is used to apply the gate voltage for up to 24 hours and simultaneously monitor the gate leakage current. The device under test (DUT) is put in an oven with the temperature set at 150°C. The threshold voltage variation of the DUT during the stress is measured by interrupting the stress and extracting the threshold voltage of the DUT rapidly (in less than 10 seconds).

III. Results And Discussion

In this section, the gate leakage current behaviors for different vendors and the threshold voltage variations for vendor H under different gate voltages are displayed. The mechanisms

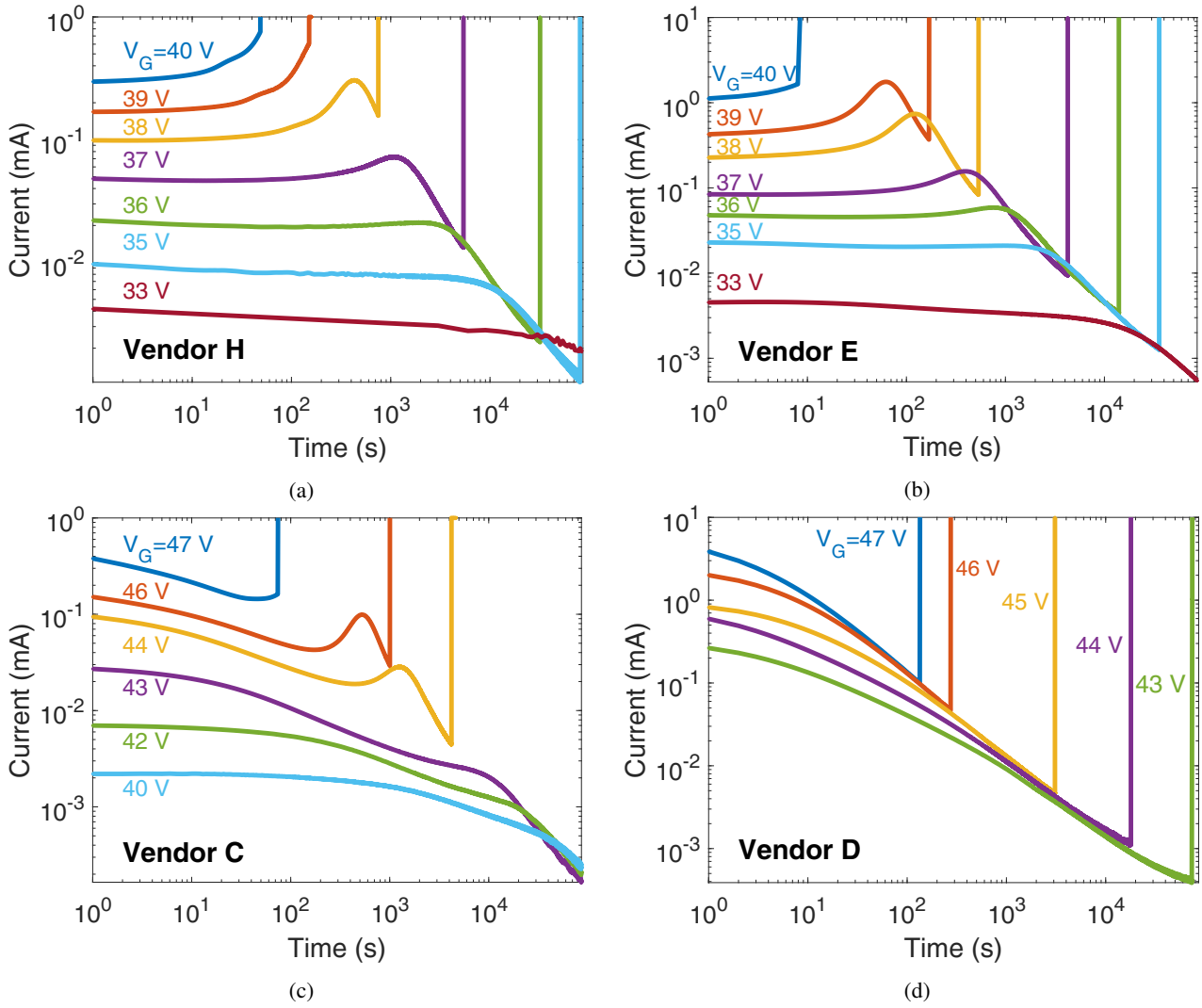


Fig. 2: Gate leakage currents for commercial SiC power MOSFETs at 150°C for (a) vendor H with gate voltages from 33 V to 40 V, (b) vendor E with gate voltages from 33 V to 40 V, (c) vendor C with gate voltages from 40 V to 47 V, and (d) vendor D with gate voltages from 43 V to 47 V.

of hole and electron trapping under different oxide electric fields are addressed to explain the distinct gate leakage current behaviors and corresponding threshold voltage variations.

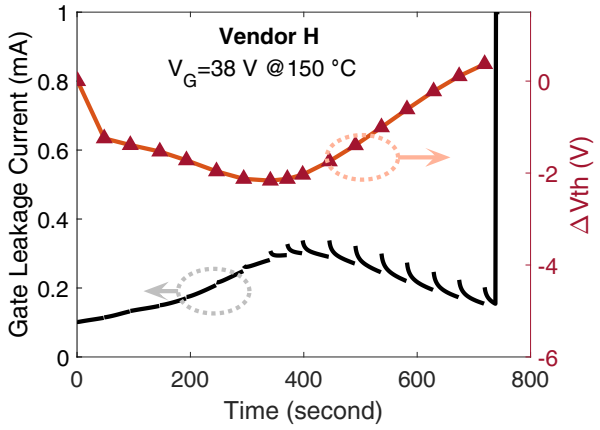
A. Gate leakage currents under different oxide electric fields

The gate leakage currents are monitored with multiple stress voltages for devices from different vendors. The gate leakage current results are shown in Fig. 2. For vendor H [Fig. 2(a)], the applied gate voltages vary from 33 V to 40 V (electric fields ranging from 8.25 MV/cm to 10 MV/cm). The currents display distinct behaviors under different stress voltages. These behaviors can be categorized into three groups: (1) at high gate voltages of 40 V, and 39 V, the gate leakage currents keep increasing until DUTs breakdown; (2) at reduced stress voltages (V_G=38 V, 37 V, and 36 V), the gate leakage currents increase initially and then decrease until breakdown; (3) with further reduced gate stress (V_G=35 V, and 33 V), the gate leakage currents of the DUTs decrease throughout the 24-hour measurement period but eventually breakdown.

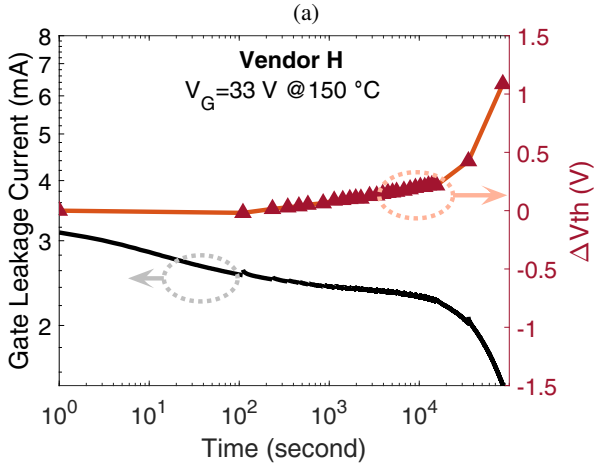
The gate leakage current results for vendor E [Fig. 2(b)] also show three distinct behaviors as vendor H. For vendor C [Fig. 2(c)], the currents experience an initial decrease followed by distinct behaviors similar to vendor H and E. In the case of vendor D [Fig. 2(d)], the gate leakage currents continuously decrease under multiple gate bias (from 47 V to 43 V) until the devices break down.

B. Threshold voltage variations

The threshold voltages are monitored throughout the stress for two distinct cases of V_G=38 V and 33 V for vendor H (Fig. 3). A strong correlation between the threshold voltage variations and the gate leakage currents is observed. For vendor H at V_G=38 V [Fig. 3(a)], the threshold voltage decreases initially when the gate leakage current increases.

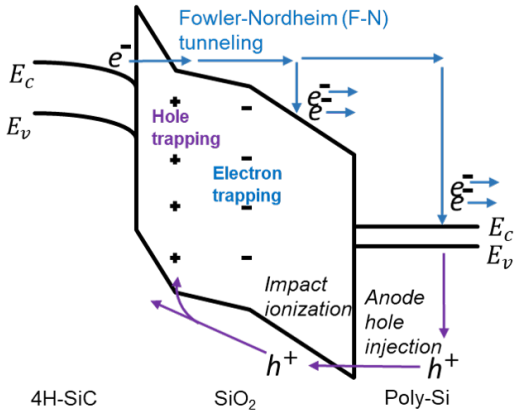


(a)

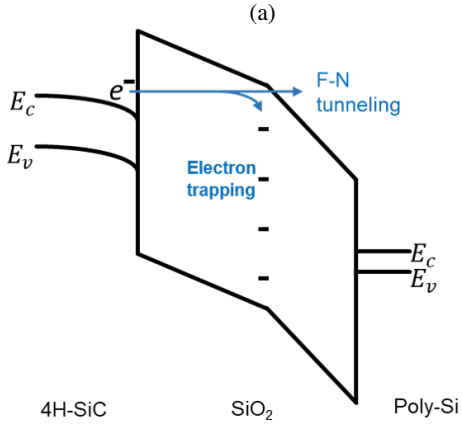


(b)

Fig. 3: Threshold voltage variations and gate leakage currents during gate voltage stresses at (a) V_G=38 V, and (b) V_G=33 V for vendor H.



(a)



(b)

Fig. 4: Band diagrams for (a) hole and electron trapping under high electric field and (b) only electron trapping under low electric field (the trapped electrons are represented by a sheet charge located at the centroid of the distribution).

Then the threshold voltage starts increasing at around 400 seconds when the gate leakage current begins to decrease. At V_G=33 V [Fig. 3(b)], the threshold voltage of the DUT continuously increases, and the gate leakage current decreases throughout the 24-hour measurement.

C. Hole and electron trapping under different gate voltages

The hole and electron trapping are considered to explain the distinct behaviors of the gate leakage current and the variations of the threshold voltage. As shown in Fig. 4, the positive and negative charge trapping in the gate oxide enhances and reduces the F-N tunneling, respectively, by modifying the electric field and barrier in the oxide near the SiC/SiO_2 interface. Under high gate voltages (high electric field in the gate oxides), electrons that tunnel into the gate oxide get trapped in the bulk of the gate oxide and some electrons gain enough energy under high oxide electric fields and cause impact ionization in the oxide near the anode [Fig. 4(a)] [26]–[28]. Electron and hole pairs are generated in this process. The generated holes drift to the SiC side and get trapped throughout the gate oxide. The electrons with high energy that reach the anode (polysilicon gate electrode) collide with Si atoms and generate electron and hole pairs. The generated holes gain part of the energy from the original electron and experience a lower barrier height. These holes inject into the SiO_2 through the AHI process as shown in Fig. 4(a) [18], [27], [29]–[33]. The holes from AHI also drift towards the cathode and get trapped in the gate oxide. The trapped holes from both processes enhance the electric field in the oxide near the SiC/SiO_2 interface, which further reduces the barrier width for electrons, and therefore increases electron injection by F-N tunneling current and subsequent trapping of electrons in the gate oxide. The enhanced electron injection causes additional hole current due to impact ionization and/or AHI and consequently initiates positive feedback that may or may not be quenched depending upon whether electron or hole trapping dominates. There is controversy in the literature as to which process of hole generation is truly present. In this paper, we simply assume that the holes are being created and injected into the gate oxide by either process and have no way of resolving the controversy with our data.

At low fields, holes are not present and only electron trapping [Fig. 4(b)] happens when electrons tunnel through the oxide. The electrons injected into SiO_2 get trapped both near the interface and throughout the bulk of the gate oxide. The trapped electrons (represented by a sheet charge located at the centroid of the distribution) relax the oxide electric field near the cathode, extend the tunneling barrier, and reduce F-N tunneling. With only electron trapping under low electric fields, the tunneling barrier width continuously increases and the tunneling current continuously reduces.

D. Influence for charge trapping on gate leakage currents and threshold voltage variations

The distinct behaviors of the gate leakage current (Fig. 2) are explained by positive and negative charge trapping. Under high gate biases (40 V and 39 V for vendor H, and 40 V for vendor E), the hole trapping dominates under high electric field in gate oxide and initiates positive feedback for the gate leakage current. Thus, the gate leakage current increases throughout the measurement until the device breaks down [5]. For reduced gate voltages (38 V to 36 V for vendor H, and 39 V to 36 V for vendor E), the hole trapping is dominant initially, and then the electron trapping overtakes. As a result, the currents are enhanced by positive charge trapping and then reduced by accumulating negative trapped charges in the gate oxide. For the lower gate voltages such as 35 V and 33 V for vendor H or vendor E, impact ionization and/or AHI are not triggered. Consequently, the electron trapping reduces the gate leakage current continuously. The oxide will break down eventually due to continuous electron trapping by charge to breakdown mechanism.

The positive/negative charge trapping is also responsible for the gate leakage current behavior for vendor C. The initial decreases of the currents are caused by electron trapping, which reflects that the gate oxide of vendor C has more defects near the SiC/SiO_2 interface which capture electrons possibly by direct band to trap tunneling than those of vendor H and E. This could be due to the poor gate oxidation process. For vendor D [Fig. 2(c)], the gate leakage current results show that the currents decrease until the devices break down (for gate voltages from 47 to 43 V). The phenomenon reveals that electron trapping in the gate oxide dominates under all stress voltages and continuously reduces the gate leakage currents for vendor D. The results imply a significant number of defects which trap electrons in the gate oxide of vendor D devices, reflecting the poor quality of the gate oxide.

With positive and negative charges trapped in the gate oxide, the threshold voltage changes. Since the hole trapping dominates initially and the positive charges increase in the gate oxide for vendor H at V_G=38 V, the trapped positive charges decrease the threshold voltage of the DUT [Fig. 3(a)]. Then the electron trapping overtakes, and the threshold voltage increases because of the build-up of negative charges in the oxide. At V_G=33 V for vendor H [Fig. 3(b)], only electron trapping exists so that the threshold voltage shows a monotonic increase. Therefore, the distinct threshold voltage variations

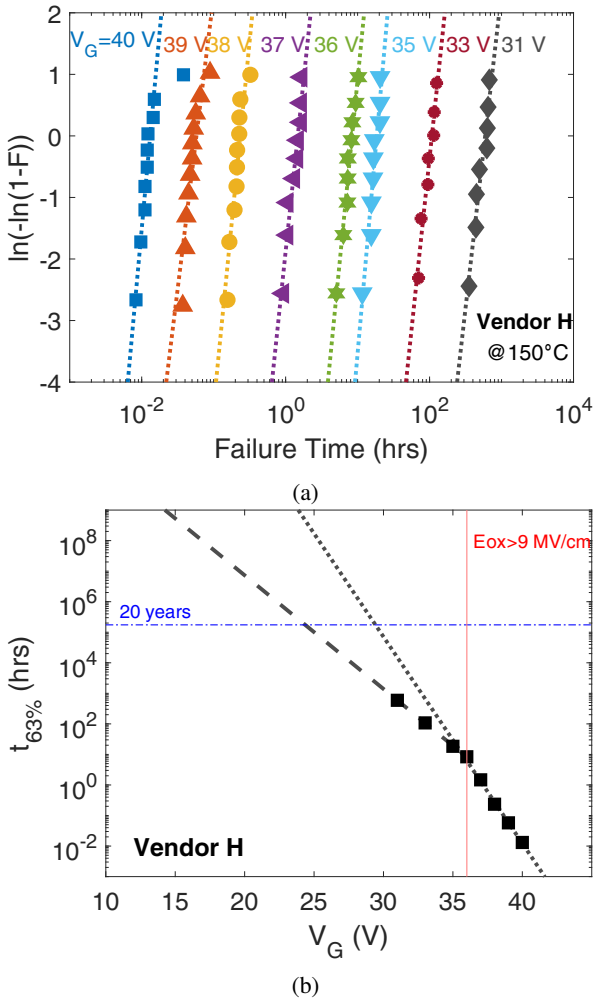


Fig. 5: TDDB measurements results for commercial SiC power MOSFETs from vendor H at 150°C: (a) Weibull distribution with gate voltages from 31 V to 40 V; (b) 63% failure times vs. gate voltages.

demonstrate the occurrence of both hole and electron trapping in the gate oxide.

E. TDDB Results

The constant-voltage TDDB measurements are conducted for commercial SiC power MOSFETs from vendor H at 150°C under gate voltages from 31 V to 40 V. Ten devices with similar threshold voltages are measured at each gate voltage. Figure 5(a) shows the Weibull distribution for the failure times of the devices under different gate voltages. Each point represents the failure time of one device. The 63% failure times for different gate voltages are extracted from the Weibull plot and shown in Fig. 5(b).

By linearly fitting the 63% failure times vs. gate voltages, an abrupt change in field acceleration factors is observed at the gate voltage of 36 V (electric field of 9 MV/cm with $E_{ox} = V_G/T_{ox}$). According to the analysis from the observed gate leakage current behaviors under high gate biases (V_G=37,

38, 39, and 40 V), hole trapping initiated by impact ionization and/or AHI accelerates the degradation of the gate oxide. However, under low gate biases (V_G=31, 33, and 35 V), the impact ionization and/or AHI is not triggered, and there is only electron trapping dominates and leads to a lower field acceleration factor. Thus TDDB results also support the explanation provided for gate leakage currents in terms of competition between electron and hole trapping.

Therefore, the investigation of gate leakage currents reveals the underlying mechanisms of the overestimation for the device normal operating lifetime in TDDB measurements at high gate voltages. Accordingly, TDDB measurements should be applied under the gate voltages (or smaller voltages) that will not trigger impact ionization and/or AHI to achieve more accurate lifetime projection. The gate voltages that will not trigger impact ionization and/or AHI can be determined by monitoring the gate leakage currents even if no information is available about the device from a given vendor. The principle also applies to on-wafer oxide screening during the manufacturing of the devices. The screening oxide field should be less than 9 MV/cm to prevent hole generation, which may reduce the lifetime of the devices.

IV. Conclusion

In conclusion, the gate leakage current behaviors and the corresponding threshold voltage variations indicate different failure modes under different gate oxide electric fields for commercial 1.2 kV SiC power MOSFETs. Under higher gate voltages, impact ionization and/or AHI can be triggered which produces hole trapping in the gate oxide. The trapped holes increase the gate leakage current and decrease the device threshold voltage. With only electron trapping (under lower gate voltages), the gate leakage current continuously decreases, and the threshold voltage increases.

The impact ionization and/or AHI triggered by higher gate voltages accelerates the degradation of the gate oxide and leads to the overestimation of the lifetime from constant-voltage TDDB measurements. Therefore, it is recommended that the constant-voltage TDDB measurements and the screening of the devices should be conducted with lower gate voltages (below 9 MV/cm) to avoid impact ionization and/or AHI.

Futher work, such as varying the temperature and testing of devices from additional vendors, is ongoing. The authors are also developing a quantitative model to further understand the gate leakage current behavior.

Acknowledgment

This research is supported in part by the US Department of Energy (DOE) Vehicle Technologies Office (VTO) under the Electric Drive Train Consortium and the block gift grant from the II-VI Foundation. The authors also gratefully acknowledge the contributions of the Power Electronics Teams at Ford Motor Company's Research and Innovation Center as well as at Sandia National Laboratories.

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