MMC-Based High Gain Solid-State Transformers for Energy Storage Applications

Diang Xing, Xiao Li, Yue Zhang, Qianyi Cheng, Zhining Zhang, Boxue Hu, Anant Agarwal, and Jin Wang
Center for High Performance Power Electronics (CHPPE)
The Ohio State University
Columbus, OH, USA
xing.174@osu.edu, wang.1248@osu.edu

Robert Guenther
GPEM LLC.
Marysville, OH, USA
rnguenther@gmail.com

2021 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-7281-8949-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/APEC42165.2021.9487233

***Abstract*— This paper examines modular high-gain isolated DC/DC converter topologies for energy storage systems (ESS). The structure and operation of the topologies discussed resemble modular multilevel converter (MMC) and dual-active-bridge (DAB), in that regulated bidirectional power flow is realized with traditional circuit building blocks by applying classic phase shift control. The operation of two topologies is presented. Both can realize a high voltage step-down ratio from a medium-voltage (MV) bus to a medium frequency (MF) transformer primary winding so that reduced winding insulation is achieved to shrink the transformer size. These two topologies are compared in terms of their step-down ratios, frequency multiplication factors, switching and conduction losses, submodule (SM) capacitance, and transformer area products. Preliminary experimental results are presented to verify the key features of both topologies using 3.3-kV silicon carbide (SiC) devices (Generation-2 engineering samples from GeneSiC).**

Keywords*— Medium-voltage (MV), DC/DC converter, solid-state transformer (SST), modular multilevel converter (MMC), high step-ratio, silicon carbide (SiC).

I. INTRODUCTION

Medium-voltage DC (MVDC) is considered as an alternative solution for renewable energy systems integration [1]-[5], whose resiliency can be improved by an energy storage system (ESS) as shown in Fig. 1. The DC/DC converter between the MVDC bus and the low-voltage DC (LVDC) battery generally requires galvanic isolation, regulated bidirectional power control, high voltage and power ratings, and a high voltage step ratio.

One popular converter type for this DC/DC application is the hybrid converter combining a modular multilevel converter (MMC) and one side of a dual-active-bridge (DAB) circuit [6]-[11]. In this hybrid converter, the MMC is on the MV side and the full-bridge circuit is on the LV side, with an isolated medium-frequency (MF) transformer in the middle. The MMC-based circuit on the MV side can achieve the following benefits: 1) the input voltage is not limited by the voltage rating of the semiconductor device, allowing the converter to be easily scaled up or down by adding or removing series-connected submodules (SMs); 2) the MMC output voltage's dv/dt can be reduced by the multi-level waveforms, which minimizes the insulation stress on the output side; and 3) the MMC-based circuits have a high level of operational flexibility due to various SM structures

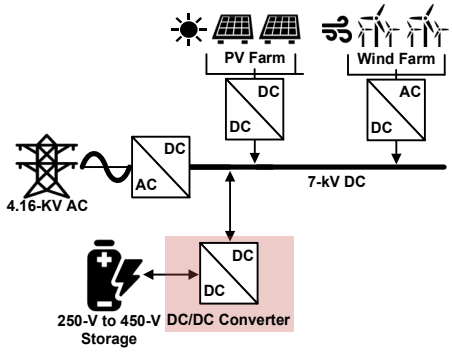


Fig. 1 MVDC-based renewable energy harvesting system with storage.

and modulation approaches [12]-[14].

The classic phase shift control of DABs can also be used in this hybrid circuit to regulate bidirectional power flow as shown in Fig. 2. In Fig. 2, two square-shape voltage sources represent the primary and secondary side circuits, where there is an adjustable phase shift angle (φ) for controlling the direction and magnitude of the transmitted power. The inductor (L_{aux}) is the transformer leakage inductance or auxiliary inductor reflected to the primary side. The amplitude of the primary side voltage can be represented as the MVDC bus voltage (V_{dc}) divided by a step-down ratio (r_v). Similarly, the transformer fundamental frequency (f_{trans}) is related to the SM switching frequency (f_{sw}) with a frequency multiplication factor (r_f). For this square-wave based MMC, some publications focus on the quasi two-level (Q2L) type modulation [6], [7], [15]-[18]. With up to $4/\pi$ effective modulation index, this approach can utilize the high excitation voltage amplitude to reduce the output current and lower the copper loss. However, generally no voltage step-down can be achieved in classic Q2L-type MMCs and the transformer frequency cannot exceed the semiconductor device switching frequency. Considering the windings' insulation and the limited frequency, the MF transformer volume may be relatively high. Alternate approaches target reducing the transformer primary side voltage amplitude [9], [11], [19]-[21]. These methods can potentially improve the MF transformer performance or shrink its size due to: 1) the reduced MMC output voltage requires less insulation distance; 2) utilizing the SM insert/bypass sequence, the transformer fundamental frequency can be significantly higher than the SM switching frequency, thus the frequency of the MF transformer can be increased and the transformer core

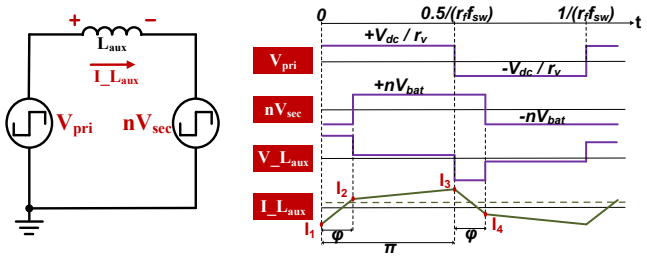


Fig. 2 Square-shape voltage-based DC/DC conversion with phase-shift control.

area can be reduced, and 3) better transformer coupling can be achieved by the lower transformer turns ratio. Though the increased output current may reduce the converter efficiency, the use of wide bandgap (WBG) semiconductor devices will alleviate this disadvantage [22]-[24]. Accordingly, under some operational conditions, there topologies may realize superior efficiency with extremely low transformer volume.

In this paper, two types of high step-down ratio MMC-DAB hybrid circuits for MVDC-to-LVDC conversion are introduced and compared. In Section II, their circuit topologies and modulation methods are discussed. And their comparison results are shown in Section III. In Section IV, experimental results with 3.3-kV discrete SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) [24] based MMC converter are presented to verify the key features of both circuits. A conclusion of the research presented is given in Section V.

II. Circuit Topologies and Modulation Methods

As shown in Fig. 3, a circuit topology is proposed, denoted as Type #1, which chooses the highest step-down ratio based on [19] and changes the secondary side from a rectifier to an active full-bridge circuit based on [21]. A comparable design, which is an isolated version, modified from [9], is shown in Fig. 4 and denoted as Type #2. Compared to the Type #1 topology with the traditional MMC structure, Type #2 topology inserts the transformer primary winding in series with two arms. Therefore, the transformer magnetizing inductance can be utilized to limit the circulating current (i_z) ripple, so extra arm inductors are not needed.

In Fig. 3 and Fig. 4, the operational principles of both type circuits are presented with the number of SMs per leg (N) equal to 6. On the primary side, the static voltages of all SM capacitors are identical and equal to the MVDC voltage (V_{dc}) divided by the averaged inserted SM number (N_i) per transformer fundamental cycle, where N_i equals 5 for the Type #1 topology and N_i equals 5.5 for the Type #2 topology. By inserting and bypassing SM capacitors as the sequences shown in Fig. 3 and Fig. 4, the transformer primary side voltages of both types equal $\pm V_{dc}/(2N_i)$. Additionally, the transformer frequencies equal $f_{sw}(N_i+1)/2$ and $f_{sw}(2N_i+1)/2$ for Type #1 and Type #2 topologies respectively. On the secondary side, the full-bridge circuit is actively controlled to generate the positive or negative LVDC voltage ($\pm V_{bat}$) at the transformer frequency with a phase angle φ. The key features of the two types of circuits are summarized in Table I.

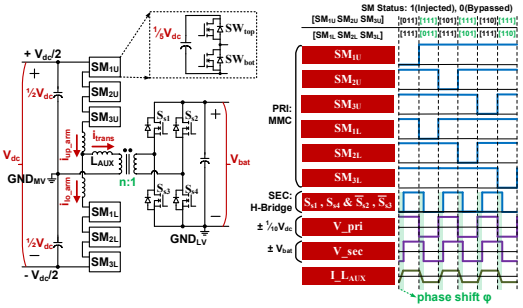


Fig. 3 The Type #1 hybrid topology: $N = 6$, $r_v = 10$, $r_f = 3$.

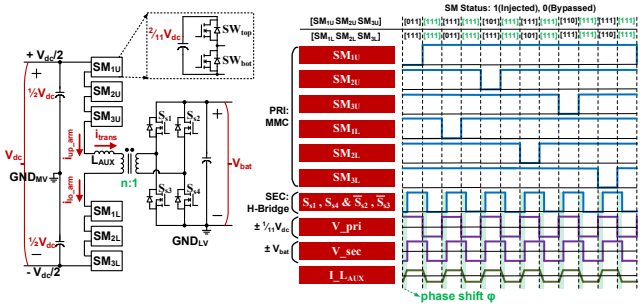


Fig. 4 The Type #2 hybrid topology: $N = 6$, $r_v = 11$, $r_f = 6$.

TABLE I
Key Features of Type I and Type II Topologies

	Type #1	Type #2
Minimum SM Number Per Leg	N	N
SM Capacitor Voltage (V_{sm})	$V_{dc}/(N-1)$	$2V_{dc}/(2N-1)$
Step-down Ratio ***($r_v = V_{dc}/\lvert V_{pri}\rvert$)***	$2N-2$	$2N-1$
Frequency Multiplication Ratio ***($r_f = f_{trans}/f_{sw}$)***	$N/2$	N
Arm Inductor	Stray inductance or extra arm inductors	Transformer magnetizing inductance

III. Topology Comparision Based on Case Studies

Based on case studies, this section compares the Type #1 and Type #2 topologies in terms of step-down ratio, power loss, and volumes of the transformer and SM capacitors. The comparison only focuses on the primary side MMC and the MF transformer, while the secondary side features are omitted. The step-down ratio has been discussed in Table I. The power loss calculation includes the conduction and switching losses of the semiconductor devices. The volume of the MF transformer uses the area product (AP_{trans}) and the volume of the SM capacitors uses the sum of SM capacitors energies ($E_{cap(tot)}$) as indicators respectively.

As summarized in Table II, the Type #1 and Type #2 topologies are configured on the MVDC side with a 7-kV bus voltage. On the battery side, there is a DC voltage ranging from 250 V to 450 V. The transformer turns ratio (n) is assumed to be 7:3, and its operating frequency is set to 30 kHz. It is assumed that the primary side MMC leads the secondary side full-bridge circuit by a phase angle φ. Six SMs with the half-bridge structure are used which is based on the discrete 3.3-kV SiC MOSFETs. The transmitted power is scaled down and fixed at 10 kW.

Assumptions and formula derivations are needed for conducting numerical results in case studies. The analysis will

TABLE II
PARAMETERS OF THE DC/DC CONVERTER IN THE CASE STUDY

P_{in}	Power rating	10 kW
V_{dc}	MVDC voltage	7 kV
V_{bat}	Battery (LVDC) voltage	250 V to 450 V
ΔV_{sm}	Peak-to-peak submodule voltage ripple	< 5% $V_{sm(base)}$
f_{trans}	Transformer frequency	30 kHz
φ	Phase shift angle	0° to 50°

start from the characteristics of apparent power (S_{in}).

Based on the power transmission circuit shown in Fig. 2, the apparent power can be presented as

$$S_{in} = I_{trans(rms)} \times \frac{V_{dc}}{r_v} \tag{1}$$

where $I_{trans(rms)}$ is the root-mean-square (rms) value of the transformer current, whose instantaneous value equals the auxiliary inductance current (I_L_{aux}), as shown in the following equation

$$i_{trans}(t) = i_{trans}(0) + \frac{1}{L_{aux}} \int \left(V_{pri}(t) - nV_{sec}(t) \right) \mathrm{d}t \tag{2}$$

The values for i_{trans} of I_1 to I_4 in Fig. 2 are shown in Table III [25]-[27]. In Table III, D is the ratio of the MVDC voltage to the battery voltage referred to the primary side, which is

$$D = \frac{nV_{bat}}{V_{dc}} \tag{3}$$

Assuming the circulating current ripple is neglected, the DC component of the circulating current $i_{z(dc)}$ is

$$i_{z(dc)} = \frac{P_{in}}{V_{dc}} \tag{4}$$

L_{aux} and f_{trans} can be eliminated by replacing the auxiliary inductance with

$$L_{aux} = \frac{D{V_{dc}}^2}{2\pi f_{trans} r_v P_{in}} \varphi \left(1 - \frac{\varphi}{\pi}\right) \tag{5}$$

Following the basic rms calculation procedure, the transformer rms current of type #1 topology can be derived as

$$I_{trans(rms)} = \frac{\pi P_{in}}{\varphi(\pi - \varphi) D V_{dc}} \sqrt{\frac{\pi^2 {r_v}^2 D^2}{12} - \left(\frac{2\varphi^3}{3\pi} - \varphi^2 + \frac{\pi^2}{6}\right) r_v D + \frac{\pi^2}{12}} \tag{6}$$

and the transformer rms current of the Type #2 topology can be estimated by

$$I_{trans(rms)} = \sqrt{\left(\frac{\pi P_{in}}{\varphi(\pi - \varphi) D V_{dc}} \sqrt{\frac{\pi^2 {r_v}^2 D^2}{12} - \left(\frac{2\varphi^3}{3\pi} - \varphi^2 + \frac{\pi^2}{6}\right) r_v D + \frac{\pi^2}{12}}\right)^2 + \left(\frac{P_{in}}{V_{dc}}\right)^2} \tag{7}$$

For (6) and (7), the values of phase shift angle can be calculated, which is

$$\varphi = \frac{\pi}{2} - \sqrt{\frac{r_v \pi^2 - 8 r_v \pi^2 f_{trans} L_{aux} P_{in}}{4 {V_{dc}}^2}} \tag{8}$$

By scanning the values of L_{aux} from 10 µH to 150 µH with 5-µH steps, the apparent power in (1) and the phase shift angle in (8) are plotted in Fig. 5. Based on Fig. 5, a 120-µH auxiliary inductance is appropriate to realize a relatively low apparent power without exceeding the 50° phase shift angle across the full

TABLE III
INSTANTANEOUS TRANSFORMER CURRENTS OF I_1 TO I_4

	Type #1	Type #2
I_1	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(-r_v D\varphi - \frac{\pi}{2} + r_v D \frac{\pi}{2}\right)$	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(-r_v D\varphi - \frac{\pi}{2} + r_v D \frac{\pi}{2}\right) + i_{z(dc)}$
I_2	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(\varphi - \frac{\pi}{2} + r_v D \frac{\pi}{2}\right)$	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(\varphi - \frac{\pi}{2} + r_v D \frac{\pi}{2}\right) + i_{z(dc)}$
I_3	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(r_v D\varphi + \frac{\pi}{2} - r_v D \frac{\pi}{2}\right)$	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(r_v D\varphi + \frac{\pi}{2} - r_v D \frac{\pi}{2}\right) + i_{z(dc)}$
I_4	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(-\varphi + \frac{\pi}{2} - r_v D \frac{\pi}{2}\right)$	$\frac{V_{dc}}{2\pi r_v f_{trans} L_{aux}} \left(-\varphi + \frac{\pi}{2} - r_v D \frac{\pi}{2}\right) + i_{z(dc)}$

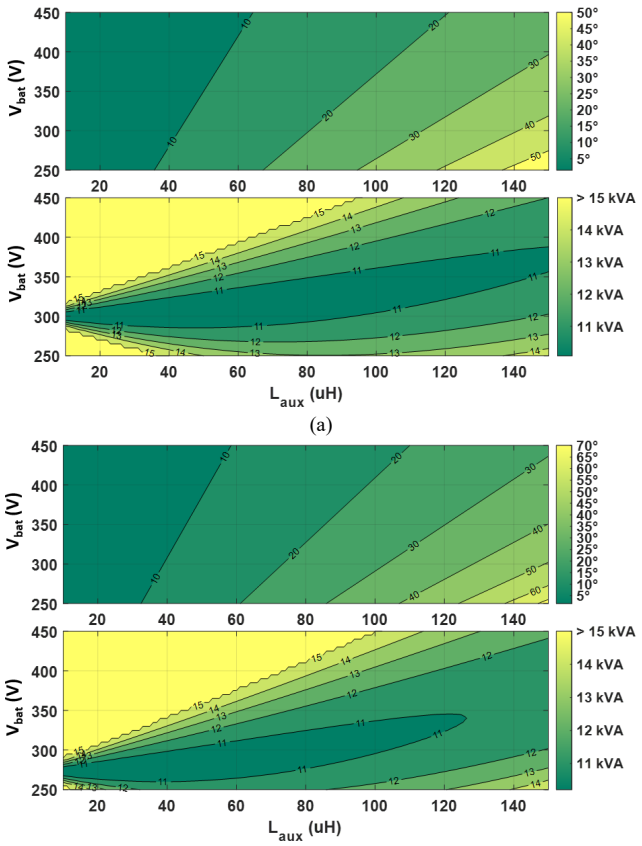


Fig. 5 Phase shift angle and apparent power vs. auxiliary inductance at different battery voltages for Type #1 topology (a) and Type #2 topology (b).

output voltage range for both the topologies. With this auxiliary inductance value, the Type #1 topology has a 19.8-to-41.1° phase shift angle range, and a 10.82-to-13.48-kVA apparent power range with 11.72-kVA average apparent power. The Type #2 topology has a 22.1-to-47.4° phase shift angle range, and a 10.97-to-13.58-kVA apparent power range with 11.82-kVA average apparent power.

A. Semiconductor Device Conduction Loss

The semiconductor device's conduction loss depends on the number of SMs, the turn-on resistance of the semiconductor device, and the rms values of the arm currents, and is shown as

$$P_{cond} = \frac{N {I_{up\_arm(rms)}}^2 R_{ds(on)}}{2} + \frac{N {I_{lo\_arm(rms)}}^2 R_{ds(on)}}{2} \tag{9}$$

where $R_{ds(on)}$ is the semiconductor device turn-on resistance and $I_{up\_arm(rms)}$ and $I_{lo\_arm(rms)}$ are the rms values of the upper and lower arm currents.

For the Type #1 topology, the transient arm currents are

$$i_{up\_arm}(t) = \frac{i_{trans}(t)}{2} + i_{z(dc)} \tag{10}$$

$$i_{lo\_arm}(t) = -\frac{i_{trans}(t)}{2} + i_{z(dc)} \tag{11}$$

Utilizing (2), (4), and (6), the Type #1 topology arm rms currents can be estimated as

$$I_{up\_arm(rms)} = I_{lo\_arm(rms)} = \sqrt{\frac{I_{trans(rms)}^{\ 2}}{4} + \left(\frac{P_{in}}{V_{dc}}\right)^2} \tag{12}$$

For the Type #2 topology, the upper and lower arm currents are the same as the transformer current, which can be shown as

$$i_{up\_arm}(t) = i_{lo\_arm}(t) = i_{trans}(t) \tag{13}$$

$$I_{up\_arm(rms)} = I_{lo\_arm(rms)} = I_{trans(rms)} \tag{14}$$

The next step is to calculate the device turn-on resistance based on the selected 3.3-kV SiC MOSFET. To fairly compare topologies that have different rms currents requiring different die areas, the product of the selected device's turn-on resistance ($0.31T_j + 37.65\ m\Omega$) and one quarter of its rated current ($0.25 \times 80\ A$) is considered a constant. Then the turn-on resistance, which depends on the operational current of the semiconductor device, is

$$R_{ds(on)} = (0.31T_j + 37.65) \times \frac{0.25 \times 80}{I_{semi(rms)}}\ (m\Omega) \tag{15}$$

where $I_{semi(rms)}$ is the assumed as the averaged arm rms current that can be calculated from (12) or (14) with the battery voltage ranging from 250 V to 450 V. The junction temperature (T_j) is assumed as 100°C.

The conduction loss calculation results obtained from the above formulas are: the Type #1 topology with 8.49-A $I_{semi(rms)}$ results in 162-mΩ $R_{ds(on)}$ and 69.94-W P_{cond}, and the Type #2 topology with 18.57-A $I_{semi(rms)}$ results in 74-mΩ $R_{ds(on)}$ and 153.11-W P_{cond}.

B. Semiconductor Device Switching Loss

For the semiconductor device's switching loss calculation, the following assumptions are made to simplify the analysis. First, the soft-switching only depends on the direction of arm current during switching transients, which means factors such as deadtime, busbar leakage inductance, and semiconductor device output capacitance are ignored. Second, all soft-switching losses are neglected. Third, all SM capacitor voltages are identical during switching transients.

The general switching loss formula can be presented as

$$P_{sw} = \sum_{1}^{N} E_{sw} f_{sw} \tag{16}$$

where the switching energy (E_{sw}) is the sum of hard turn-on and turn-off energies (E_{on} and E_{off}),

$$E_{sw} = E_{on}(I_{on}, V_{sm}) + E_{off}(I_{off}, V_{sm}) \tag{17}$$

in which, i_{on} and i_{off} are the arm currents during switching and V_{sm} is the static SM capacitor voltage. Similar to (15), based on the characteristics of the selected 3.3-kV SiC MOSFET, the values of E_{on} and E_{off} can be estimated as

$$E_{on} = \frac{V_{sm}}{2\ kV} \times \frac{I_{semi(rms)}}{0.25 \times 80\ A} \times 0.29 I_{on}\ \text{(mJ)} \tag{18}$$

$$E_{off} = \frac{V_{sm}}{2\ kV} \times \frac{I_{semi(rms)}}{0.25 \times 80\ A} \times 0.038 I_{off}\ \text{(mJ)} \tag{19}$$

The next step is to analyze all the hard-switching scenarios and calculate their switching energies. The direction and amplitude of arm currents need to be analyzed when one or several SMs are being inserted or bypassed. According to (10), (11), or (13), the arm currents of both topologies can be determined from the instantaneous transformer current shown in (2). Based on Fig. 2, only the currents of I_1 and I_3 are related to the SM switching energies. Fig. 6 shows the switching scenarios for the Type #1 and Type #2 topologies.

When a SM is being inserted with a positive arm current, the bottom switch will first experience a hard turn-off, and then the top switch will go through a soft turn-on; with a negative arm current, the bottom switch will have a soft turn-off, then the top switch will go through a hard turn-on. During the SM bypass process, the top switch experiences a soft turn-off and the bottom switch has a hard turn-on with a positive arm current; the top switch goes through a hard turn-off and the bottom switch a soft turn-on with a negative arm current. In an example of the Type #1 topology, the upper arm SMs switching status is shown in Fig. 7. During the first zone (Z1), between 250-V to 385-V V_{bat}, switches have a hard turn-off or soft turn-on whether the SM is being inserted or bypassed. In the second zone (Z2), between 385-V to 418-V V_{bat}, the top switch has a soft turn-off and the bottom switch has a hard turn-on when the SM is being

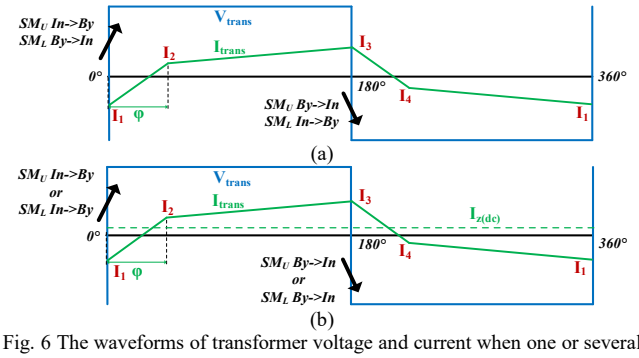


Fig. 6 The waveforms of transformer voltage and current when one or several SMs are being inserted or bypassed. (a) scenario of the Type #1 topology, and (b) scenario of the Type #2 topology.

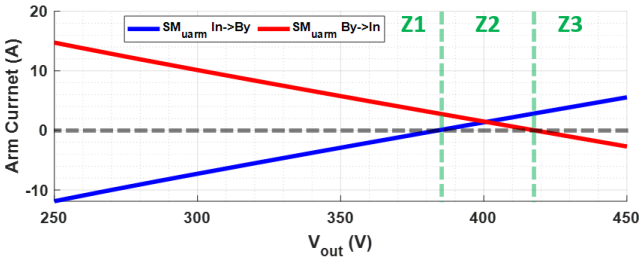


Fig. 7 Type #1 topology instantaneous upper arm current when one SM in the upper arm needs to be inserted or bypassed.

bypassed, and the bottom switch has a hard turn-off and the top switch has a soft turn-on when the SM is being inserted. In the third zone (Z3), switches have a soft turn-off or hard turn-on for both inserting and bypassing actions.

By considering all voltage conditions on the battery side, the switching loss can be calculated. The Type #1 topology has $E_{on} = (0.087 \times I_{on})$ mJ and $E_{off} = (0.011 \times I_{off})$ mJ which leads to 12.95-W P_{sw}. The Type #2 topology has $E_{on} = (0.17 \times I_{on})$ mJ and $E_{off} = (0.022 \times I_{off})$ mJ which leads to 29.91-W P_{sw}.

C. Transformer Area Product

The product (AP_{trans}) of transformer window area (A_{wind}) and core area (A_{core}) can be used to estimate the transformer's size. The formulas are shown as

$$A_{wind} = \frac{2N_{turns}I_{trans(rms)}}{K_w J_{max}} \tag{20}$$

$$A_{core} = \frac{\lambda_{pri(max)}}{2K_c N_{turns} B_{max}} \tag{21}$$

$$AP_{trans} = A_{core} \times A_{wind} = \frac{I_{trans(rms)}\lambda_{pri(max)}}{K_c K_w J_{max} B_{max}} \tag{22}$$

where all parameters are referred to the transformer primary side. N_{turns} is the number of winding turns. J_{max} and B_{max} are the maximum allowable current density inside the windings and flux density inside the core. K_w and K_c are the window filling factor and core area factor, which are both less than 1. The peak flux linkage $\lambda_{pri(max)}$ is related to the excitation voltage and the period time, which is derived as

$$\lambda_{pri(max)} = \frac{V_{dc}}{2r_v f_{trans}} \tag{23}$$

The values of J_{max} and B_{max} can be referenced from [28] and [29] which are 3.04 A/mm^2 and 200 mT respectively. By assuming K_w and K_c equal 0.7 and 0.9 respectively, and adopting the maximum value of $I_{trans(rms)}$ from (6) and (7) at certain battery voltages, the following results can be conducted: Type #1 topology has AP_{trans} = 58.64-cm^4, and Type #2 topology has AP_{trans} = 59.11-cm^4.

D. Submodule Capacitance Energy

Assuming all SM capacitors are identical, then the total required SMs capacitance energy can be defined as

$$E_{cap(tot)} = \sum_{1}^{N} \frac{1}{2} C_{sm} {V_{sm}}^2 \tag{24}$$

where V_{sm} is the static SM capacitor voltage, and C_{sm} is the SM capacitance which is used to sustain an acceptable peak-to-peak voltage ripple ($\Delta V_{sm}/V_{sm}$) during operation. The SM capacitance voltage ripple is estimated by integrating the arm current during half of fundamental cycle and splitting the charge among all inserted SM capacitors in this arm [30]. The formula for the Type #1 topology can be derived as

$$C_{sm} = \left(\frac{2}{N} \times \frac{2(N-1)}{N}\right) \frac{(\pi - \varphi)\varphi D V_{dc} + 2\pi^2 N \left(\frac{P_{in}}{V_{dc}}\right) L_{aux} f_{sw}}{4N\pi^2 f_{sw}^2 L_{aux} (\Delta V_{sm}/V_{sm}) V_{sm}} \tag{25}$$

and the formula for the Type #2 topology is

$$C_{sm} = \left(\frac{1}{N} \times \frac{2N-1}{N}\right) \frac{(\pi - \varphi)\varphi D V_{dc} + 2\pi^2 N \left(\frac{P_{in}}{V_{dc}}\right) L_{aux} f_{sw}}{4N\pi^2 f_{sw}^2 L_{aux} (\Delta V_{sm}/V_{sm}) V_{sm}} \tag{26}$$

In order to sustain less than 5% SM capacitor voltage ripple, the Type #1 topology requires at least 3.40-µF capacitance for each SM along with more than 20.0-J $E_{cap(tot)}$. The Type #2 topology requires at least 8.23-µF capacitance for each SM along with more than 40.0-J $E_{cap(tot)}$.

E. Comparision of Type #1 and 2 Topologies

The parametric comparison is summarized in Fig .8. According to Fig. 8, the Type #1 topology is inferior to the Type #2 topology in terms of device switching frequency and converter step-down ratio. The Type #1 topology shows lower conduction and switching losses. Both topologies have similar transformer area products. The Type #1 topology requires less SM capacitor energy with the same SM capacitor voltage ripple percentage.

IV. Experimental Results

For both Type #1 and Type # 2 topologies, prototypes with 10-kW rated power, 7-kV rated input voltage, six SMs and 7:3 transformer turns ratio were assembled using the 3.3-kV SiC MOSFETs. The picture of the MMC and the MF transformer is shown in Fig. 9.

The voltage step-down and frequency multiplication ratios were validated with a resistive secondary side at a 30-kHz transformer frequency. The Type #1 topology test waveforms are shown in Fig. 10 (a), with an input DC voltage of 1.3 kV, the amplitude of the transformer secondary side voltage was 56 V. The output voltage of $SM_{(3L)}$ was tracked, and its switching frequency was one-third of the transformer frequency. Fig. 10 (b) shows the experimental results of the Type #2 topology prototype, in which the input DC voltage was 1.27 kV and the amplitude of the transformer secondary side voltage was 48 V. The SM switching frequency in Type #2 was one-sixth of the transformer frequency.

The DC/DC converter operation was also validated with a down-scaled power and input voltage. Fig. 11 shows the converter test waveforms based on the Type #1 topology, where the converter was tested at a 1.22-kV DC bus voltage and 923-W load power.

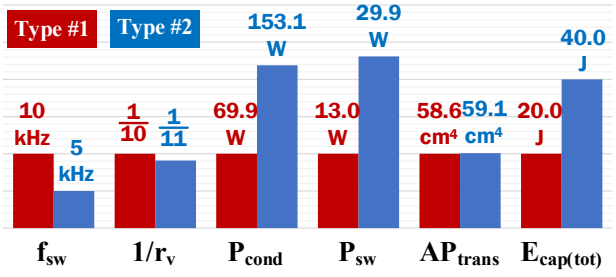


Fig. 8 Comparison results of Type #1 and Type #2 topologies in terms of SM switching frequency, voltage step-down ratio, semiconductor power losses, transformer area product, and total SM capacitors energy.

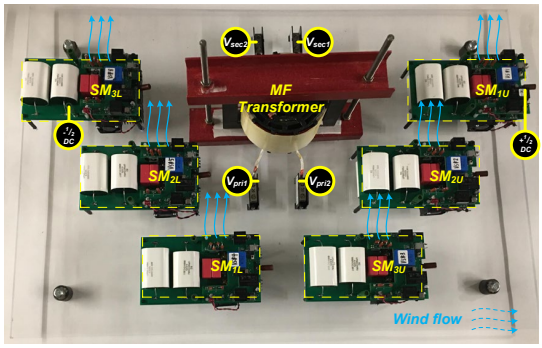
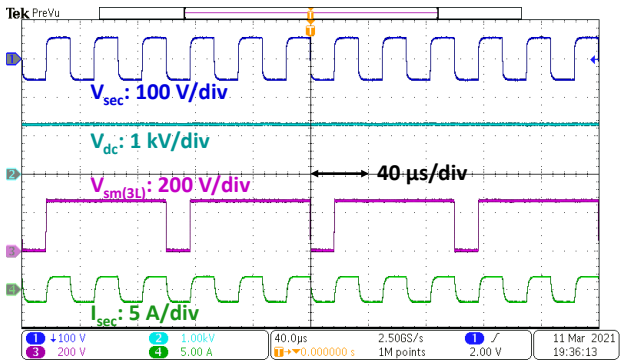
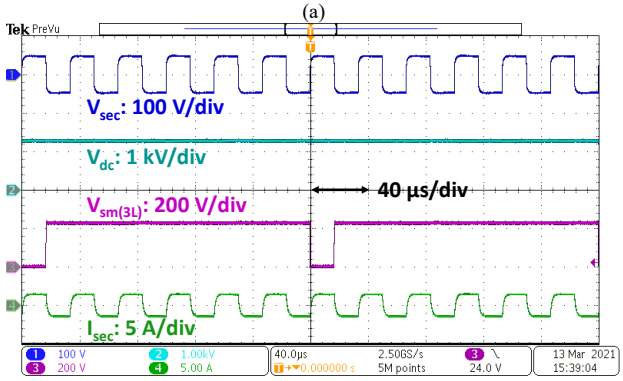


Fig. 9 Prototypes of Type #1 and Type #2 circuits (including the MMC and the MF transformer).



(a)



(b)

Fig. 10 Converter test waveforms with resistive secondary side in (a) Type #1 topology and (b) Type #2 topology.

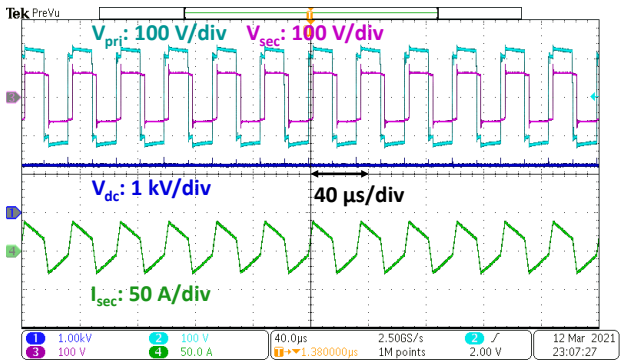


Fig. 11 Converter test waveforms with active full-bridge secondary side in Type #1 topology.

V. Conclusion

In this paper, two types of MMC-DAB hybrid high-gain isolated DC/DC converter topologies are presented. Both types of circuits can achieve high voltage step-down ratios and realize the transformer frequency multiplication function, thus the transformer winding insulation and core area can be reduced. Formulas have been derived for the step-down ratios, frequency multiplication ratios, conduction and switching losses, transformer area products, and total submodule capacitance energy. Numerical parameters have been calculated and compared based on case studies. The comparison results reveal that the Type #1 topology tends to have better efficiency and smaller SM capacitor volume, while the Type #2 topology shows higher voltage step-down and transformer frequency multiplication ratios.

Preliminary experimental results have been presented to verify the key functions of two topologies using 3.3-kV SiC MOSFETs-based prototypes. The test results at full power and voltage ratings will be reported in a following publication.

Acknowledgment

The authors gratefully acknowledge support for this work from the Energy Storage Program in the Office of Electricity Delivery and Energy Reliability at the U.S. Department of Energy.

The authors would like to thank GeneSiC for providing 3.3-kV SiC engineering samples.

References

[1] W. Chen, A. Q. Huang, C. Li, G. Wang and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 2014-2023, April 2013, doi: 10.1109/TPEL.2012.2215054.

[2] R. Suryadevara and L. Parsa, "FB-ZCS DC–DC Converter With Dual-Capacitor Resonant Circuit for Renewable Energy Integration With MVDC Grids," in IEEE Transactions on Industry Applications, vol. 56, no. 6, pp. 6792-6802, Nov.-Dec. 2020, doi: 10.1109/TIA.2020.3016926.

[3] A. Agrawal and R. Gupta, "Hybrid DERs enabled residential microgrid system with MVDC and LVDC bus layout facilities," 2018 IEEMA Engineer Infinite Conference (eTechNxT), New Delhi, India, 2018, pp. 1-6, doi: 10.1109/ETECHNXT.2018.8385349.

[4] L. Shu, W. Chen, F. Ning, W. Cao, J. Mei, J. Zhao, C. Liu and G. He, "A Resonant ZVZCS DC–DC Converter With Two Uneven Transformers for an MVDC Collection System of Offshore Wind Farms," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 7886-7895, Oct. 2017, doi: 10.1109/TIE.2017.2694389.

[5] G. Ning and W. Chen, "A Hybrid Resonant ZCS PWM Converter for Renewable Energy Sources Connecting to MVDC Collection System," in IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 7911-7920, Oct. 2018, doi: 10.1109/TIE.2018.2801783.

[6] Y. Shi and H. Li, "Isolated Modular Multilevel DC–DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application," in IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 2145-2161, March 2018, doi: 10.1109/TPEL.2017.2695575.

[7] Y. Qiao, X. Zhang, X. Yang and Y. Duan, "Trapezoidal Voltage Mode for Bidirectional Modular Multilevel DC-DC Converter," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, China, 2018, pp. 1-5, doi: 10.1109/PEAC.2018.8590330.

[8] Y. Wang, Q. Song, B. Zhao, J. Li, Q. Sun and W. Liu, "Quasi-Square-Wave Modulation of Modular Multilevel High-Frequency DC Converter for Medium-Voltage DC Distribution Application," in IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7480-7495, Sept. 2018, doi: 10.1109/TPEL.2017.2772833.

[9] Y. Li, X. Lyu and D. Cao, "A Zero-Current-Switching High Conversion Ratio Modular Multilevel DC–DC Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 151-161, March 2017, doi: 10.1109/JESTPE.2016.2623794.

[10] R. Mo and H. Li, "Hybrid Energy Storage System With Active Filter Function for Shipboard MVDC System Applications Based on Isolated Modular Multilevel DC/DC Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 79-87, March 2017, doi: 10.1109/JESTPE.2016.2642831.

[11] X. Xiang, X. Zhang, Y. Zhu, G. P. Chaffey, Y. Gu and T. C. Green, "The Resonant Modular Multilevel DC Converters for High Step-ratio and Low Step-ratio Interconnection in MVDC Distribution Network," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 5686-5693, doi: 10.1109/IECON.2019.8926939.

[12] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Pérez and J. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[13] S. Ali, Z. Ling, K. Tian and Z. Huang, "Recent Advancements in Submodule Topologies and Applications of MMC," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2990689.

[14] J. Wang, R. Burgos and D. Boroyevich, "A survey on the modular multilevel converters — Modeling, modulation and controls," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 2013, pp. 3984-3991, doi: 10.1109/ECCE.2013.6647229.

[15] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," in IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 662-669, June 2005, doi: 10.1109/TIE.2005.843973.

[16] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday and B. W. Williams, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5439-5457, Oct. 2015, doi: 10.1109/TPEL.2014.2377719.

[17] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 108-123, Jan. 2015, doi: 10.1109/TPEL.2014.2306453.

[18] A. Mertens and J. Kucka, "Quasi Two-Level PWM Operation of an MMC Phase Leg With Reduced Module Capacitance," in IEEE Transactions on Power Electronics, vol. 31, no. 10, pp. 6765-6769, Oct. 2016, doi: 10.1109/TPEL.2016.2537372.

[19] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales and Y. R. de Novaes, "Isolated DC/DC Structure Based on Modular Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 89-98, Jan. 2015, doi: 10.1109/TPEL.2014.2305976.

[20] F. Sun, J. Liu, F. Xiao, P. Chen and X. Li, "An Isolated Bidirectional Modular Multilevel DC-DC Converter for MVDC Distribution System in Ship," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, China, 2018, pp. 1-6, doi: 10.1109/PEAC.2018.8590405.

[21] X. Xiang, X. Zhang, T. Luth, M. M. C. Merlin and T. C. Green, "A Compact Modular Multilevel DC–DC Converter for High Step-Ratio MV and HV Use," in IEEE Transactions on Industrial Electronics, vol. 65, no. 9, pp. 7060-7071, Sept. 2018, doi: 10.1109/TIE.2018.2793249.

[22] A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S. Ryu and J. Zhang, "Progress in Silicon Carbide Power Devices," 2006 64th Device Research Conference, State College, PA, USA, 2006, pp. 155-158.

[23] B. Hu, X. Lyu, D. Xing, D. Ma, J. Brothers, R. Na and J. Wang, "A Survey on Recent Advances of Medium Voltage Silicon Carbide Power Devices," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 2420-2427.

[24] V. Mulpuri, S. Jadav, S. Sundaresan and R. Singh, "Characterization and Robustness Evaluation of 3.3 kV/40 mΩ SiC DMOSFETs," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 130-136, doi: 10.1109/WiPDA46397.2019.8998847.

[25] F. Krismer, Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies. Zürich: ETH, 2010. https://doi.org/10.3929/ethz-a-006395373

[26] L. Fu, X. Zhang, F. Guo and J. Wang, "A phase shift controlled current-fed Quasi-Switched-Capacitor isolated dc/dc converter with GaN HEMTs for photovoltaic applications," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 2015, pp. 191-198, doi: 10.1109/APEC.2015.7104351.

[27] L. Xue, D. Boroyevich and P. Mattavelli, "Switching condition and loss modeling of GaN-based dual active bridge converter for PHEV charger," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2016, pp. 1315-1322, doi: 10.1109/APEC.2016.7468038.

[28] C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, USA, 2014, pp. 2667-2674, doi: 10.1109/APEC.2014.6803681.

[29] Ferroxcube, "3C94 Material Specification," Supersedes data of February 2002. [Online]. Available: https://elnamagnetics.com/wp-content/uploads/library/Ferroxcube Materials/3C94_Material_Specification.pdf

[30] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao and C. Yuan, "Soft-Switching Operation of Isolated Modular DC/DC Converters for Application in HVDC Grids," in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 2753-2766, April 2016, doi: 10.1109/TPEL.2015.2448125.