Non-Isothermal Simulations to Optimize SiC MOSFETs for Enhanced Short-Circuit Ruggedness

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***Abstract*— Non-Isothermal simulations to understand Short-Circuit (SC) behavior of SiC MOSFETs were performed. Using the established model, structures to enhance the SC ruggedness were proposed. Thin gate oxide and a narrow JFET region are shown to reduce saturation current enhancing SC ruggedness without increasing $R_{on,sp}$. Results indicate thin gate oxide offers moderate improvement in SC capability, at the cost of increased C_{gs}. In contrast, narrow JFET region provides much improved (2×) SC ruggedness, as well as lower $R_{on,sp}$, with no negative impact on C_{gs}.**

Index Terms*—Short-Circuit capability, Thin gate oxide, Narrow JFET width, Non-Isothermal simulation, SiC, MOSFETs

I. INTRODUCTION

Although 4H-SiC MOSFETs are widely used in power electronics applications, detailed research on short-circuit failure mechanisms and device optimization based on device simulations is lacking. Generally, SC failure mechanisms for SiC MOSFETs can be categorized into three (Gate failure, Al melting, and thermal generated current) [1-3]. However, it is not obvious which mechanism dominates the short-circuit capability. Source doping reduction, lower channel density, and use of lower gate bias have been proposed to enhance SC capability [4]. However, these approaches result in the increase in $R_{on,sp}$. In comparison, SiC MOSFETs with reduced gate oxide thickness (t_{ox}) have demonstrated reduced saturation current (I_{sat}), with no impact on $R_{on,sp}$ [5,6].

In this paper, firstly, failure mechanisms for short-circuit are investigated. In order to precisely analyze the device structure, thermal-related simulation models are covered. The effect of thin gate oxide on SC capability has been studied in depth using Non-Isothermal device simulations. In addition, a novel approach to improve both short-circuit withstanding time and static performance, when compared to reduced gate oxide thickness, is proposed using a decreased JFET region width with increasing JFET doping concentration.

II. SHORT-CIRCUIT FAILURE MECHANISMS

During the short-circuit condition, three separate phenomena might occur when a device fails. In the first failure type (gate failure), the device undergoes gate failure due to the increase in Fowler-Nordheim (FN) tunneling, contributing to high gate leakage current at high temperatures. Furthermore, when gate oxide is exposed to high temperatures, the material properties of the gate oxide degrades. FN tunneling and high temperatures cause gate oxide to degrade and lose the gate control. The second failure type is Aluminum melting. At high temperature (>660 ºC), Al starts to melt, diffuse into SiC, and penetrate p-well of SiC, leading to drain-to-source shorting. The last failure type is related to thermally generated carriers. Although many research groups report thermal generated failure [1-3], it is hard to accept that thermal generated failure of SiC MOSFETs occurs at temperatures ~1600 ℃ since Al start to melt at approximately 660 ℃.

In order to explain thermal generated failure, the importance of increasing temperature rate is introduced by [1]. In failure mechanism 1 and 2, a device does not immediately fail when reaching critical temperatures of material degradation, but will eventually be destroyed after a certain degradation time passes. In other words, failure mechanism 1 and 2 occur after significant degradation of device materials (gate oxide and Al source metal) takes place. These failure mechanisms appear when low drain voltage is applied.

On the other hand, when junction temperature rapidly increases to critical temperature of thermal generation carrier (~1600 ℃) and degradation time is short, failure mechanism 3 will occur first before failure mechanisms 1 and 2. Moreover, as surface temperature ($T_{Surface}$) is much lower than junction temperature ($T_{Junction}$), thermal generated current can be generated in SiC MOSFETs. Generally, the last mechanism occurs when high drain voltage is applied. However, by the time of thermal generated current, the other materials, such as

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gate oxide and Al source metal, are also mostly degraded, resulting in combined failure mechanisms during the short-circuit condition.

In this paper, we will focus on gate failure mechanism using the developed Non-Isothermal simulation.

III. NON-ISOTHERMAL DEVICE SIMULATION

Using Sentaurus 2-D TCAD, Non-Isothermal simulations were conducted to investigate the influence of thin gate oxide and narrow JFET region on drain current and maximum junction temperature during the SC event. Sentaurus material library parameter sets related to SiC for Non-Isothermal simulations are lacking in previous literature. Therefore, as part of paper's effort, thermal-related simulation models, such as thermal conductivity, mobility, interface trap, gate tunneling, and SRH lifetime, were established and optimized (Table I for summary) [7-12]. The temperature dependence of heat capacity and thermal conductivity for 4H-SiC can be given as

$$C_V = 4.10 \times 10^{-9}T^3 - 1.22 \times 10^{-5}T^2 + 1.29 \times 10^{-2}T - 0.685 \text{ [7]} \quad (1)$$

$$K = (0.00105 \cdot T - 0.03)^{-1} \text{ [8]} \quad (2)$$

The bulk mobility and channel mobility can be given as

$$\mu = \frac{\mu_{max}(T/300)^{-\alpha}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}} \text{ [9, 10, 11]} \quad (3)$$

, with parameters for electron and hole given in Table I**.** In addition, for threshold voltage, V_{th}, both acceptor type traps, Q_A, and positive fixed charge, Q_F, is included at SiO_2/SiC interface, which is $Q_A = 1.5\times10^{12}$ cm^{-2}, E_c-E = 0.18eV, and $Q_F = 2\times10^{11}$cm^{-2} [9,11]. Finally, Shockley-Read-Hall (SRH) lifetime can be given as

$$\tau_{n,p} = \frac{\tau_{max}(T/300)^{\beta}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}} \text{ [12]} \quad (4)$$

, with parameters for electron and hole given in Table I**.**

Fig. 1 shows a cross section of a conventional accumulation-channel SiC MOSFET with t_{ox} of 50 nm, half JFET width (W_{JFET}) of 0.7 µm, and a diagram of the equivalent circuit for producing a SC event [13]. For a 1.2kV SiC MOSFET, drift layer doping concentration of 8×10^{15}cm^{-3} and thickness of 10 µm is designed in simulation. In order to increase channel mobility, an accumulation mode channel is used. The SC simulation with conventional structure uses an R_g of 3 Ω, V_{ds} of 800 V, and V_{gs} of 20 V. Fig. 2 shows simulated results of drain current, maximum junction temperatures ($T_{j,max}$), and gate voltage during the short-circuit event for the conventional MOSFET structure. At the start of the SC condition, maximum drain current occurs, resulting in high junction temperatures and reduction of V_{th}. Next, drain current decreases due to the decrease in electron mobility at high temperatures, despite the lowering of V_{th}. High temperatures also contribute to the

Table I. Simulation models

	Parameter model	Values
Heat capacity [7]	$C_V = 4.10 \times 10^{-9}T^3 - 1.22 \times 10^{-5}T^2 + 1.29 \times 10^{-2}T - 0.685$	
Thermal conductivity [8]	$K = (0.00105 \cdot T - 0.03)^{-1}$	
Bulk electron mobility [9]	$\mu_{Bulk}(SiC) = \frac{\mu_{max}(T/300)^{-\alpha}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}}$	α=2.8 μ_{max}=950 N_ref=1.94e17 Gamma=0.61
Bulk hole mobility [9]	$\mu_{Bulk}(SiC) = \frac{\mu_{max}(T/300)^{-\alpha}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}}$	α=2.8 μ_{max}=124 N_ref=1.76e17 Gamma=0.34
Channel electron mobility [9,10,11]	$\mu_{Channel}(SiC) = \frac{\mu_{max}(T/300)^{-\alpha}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}}$	α=-0.2 μ_{max}=28.5 N_ref=1.94e17 Gamma=0.61
Channel mobility degradation [9]	$\mu_{ph,3D} = \mu_{\max(\frac{T}{300K})^{-\theta}}$	μ_{max}=950 θ=3.2
SRH lifetime [9,12]	$\tau_{n,p} = \frac{\tau_{max}(T/300)^{\beta}}{1+[(N_D+N_A)/N_{ref}]^{\gamma}}$	β=1.72 N_ref=3e17 Gamma=0.3

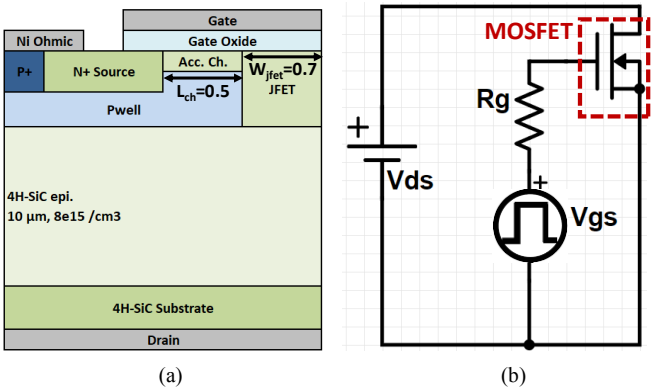


Figure 1. (a) Cross section of simulated conventional MOSFET and (b) diagram of the equivalent circuit for the short-circuit.

increase in the gate leakage current due to Fowler-Nordheim (FN) tunneling, which causes gate voltage to decrease, as shown in Fig. 3. This is because the gate leakage current leads to the voltage drop in the gate resistor (R_g). Decreased gate voltage can represent the degradation of gate oxide. In this paper, a short-circuit failure event at time t_{sc} is defined when a change in gate voltage, ΔV_{gs}, of 1 V occurs.

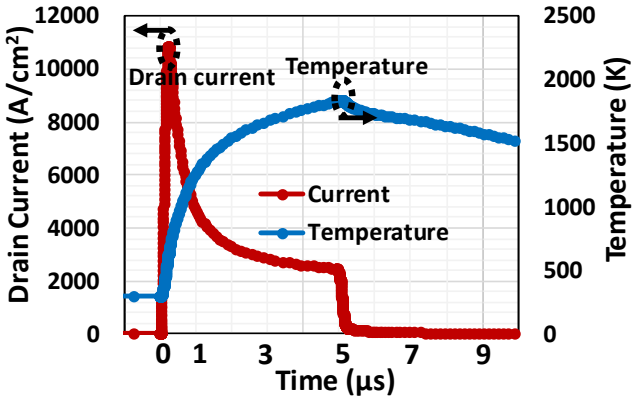


Figure 2. Simulated drain current and maximum junction temperature in SiC.

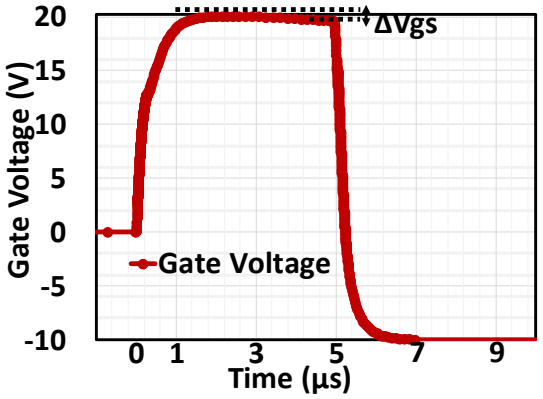


Figure 3. Applied gate voltage from +20 to -10 V during SC event.

IV. Thin Gate Oxide

Fig. 4 shows output characteristics with different gate oxide thicknesses. In order to obtain same $R_{on,sp}$ and V_{th}, different gate voltages and additional p-well implants in the channel region are applied. Although specific on-resistance of thin gate oxide is the same as that of thick gate oxide, saturation current decreases with thinner gate oxides and reduced gate voltage, as shown in Fig. 4. However, the maximum electric field in the gate oxide at the middle of JFET region increases under the forward-blocking mode, as shown in Fig. 5.

Fig. 6 shows simulated results of drain current, maximum junction temperature, and gate voltage during the short-circuit event for MOSFET with different gate oxide thicknesses. During the SC event, as mentioned in Fig.6, thin gate oxide has lower saturation current, enabling lower maximum junction temperature in SiC when compared with thicker oxide. Due to high junction temperature, more thermal generated current occurs in MOSFETs with thicker gate oxide. Moreover, these lower junction temperatures reduce Fowler-Nordheim tunneling, resulting in the low gate leakage current during the short-circuit event as shown in Fig. 7. Figure 8 shows energy band diagrams of 4H-SiC MOSFET with different gate oxide thicknesses and gate voltage at 300, 1000, and 1500 K using online band diagram program [14]. At 1500 K, thin gate oxide with V_{gs}=10V has a higher, thicker barrier between SiC and SiO_2 at high temperatures.

Figure 9 shows short-circuit time (t_{sc}) and delta Vgs (ΔVgs), and electric field in gate oxide as function of gate oxide thickness. Short-circuit time increases for t_{ox}=20 nm when compared with thicker oxides, as shown Fig. 7 and 9. This is due to lower junction temperature, contributing to low gate leakage and low gate voltage, resulting in a higher, thicker barrier between SiC and SiO_2 at high temperatures.

On the other hand, thinner gate oxides cause increased gate-to-source capacitance (C_{gs}) producing lower dV_{gs}/dt, which limits the reduction in saturation current during the SC event [5]. As a result, thin gate oxides provide low saturation currents only near the start of the short-circuit event, which offers moderate t_{sc} improvement.

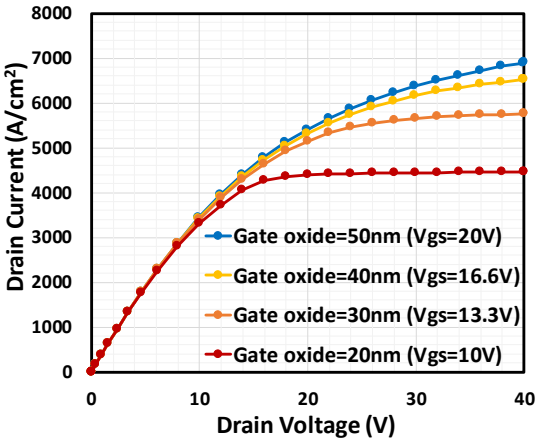


Figure 4. Simulated output characteristics with different gate oxide.

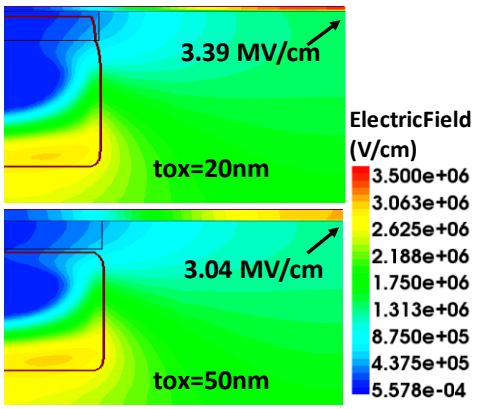


Figure 5. Electric filed under the forward blocking mode at 1600V for gate oxide thickness of 20 nm and 50 nm.

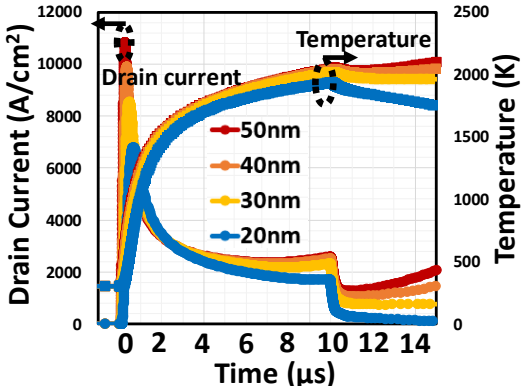


Figure 6. Simulated drain current and maximum junction temperature

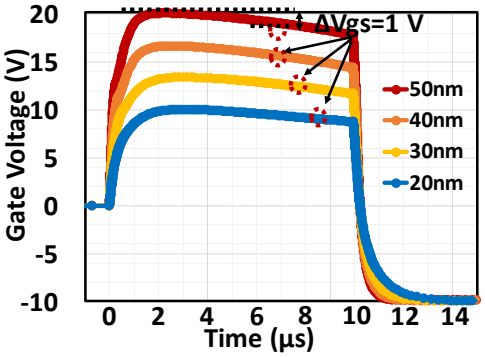


Figure 7. Simulated applied gate voltage during SC event.

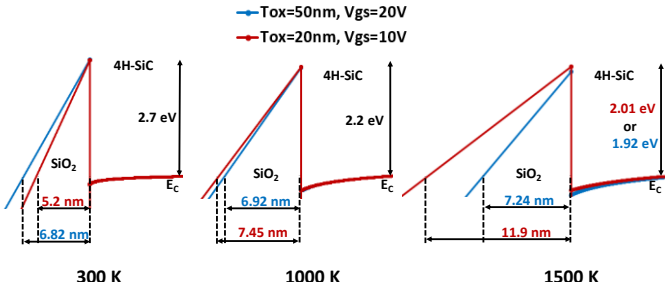


Figure 8. Energy band diagrams of 4H-SiC MOS devices with different t_{ox} and gate voltage at 300, 1000, and 1500 K.

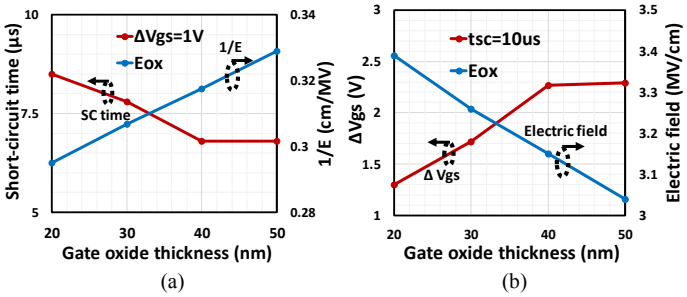


Figure 9. (a) Short-circuit time and electric field in gate oxide and (b) delta Vgs and electric field in gate oxide.

V. NARROW JFET REGION

Figure 10 (a) shows specific on-resistance as function of JFET width with different JFET doping concentration and (b) output characteristics with different JFET width. In order to achieve reduced saturation current and thereby an increase in short-circuit withstanding time, JFET width is reduced. Concurrently, it is necessary to increase JFET doping concentration to lower specific on-resistance to compensate for reduced JFET width, as shown in Fig. 10.

Figure 11 (a) shows simulated results of drain current, maximum junction temperature, and gate voltage during the short-circuit event for MOSFET with different JFET width. During the short-circuit capability, MOSFETs with narrow JFET width suppressed maximum saturation current, resulting in the reduction in maximum junction temperatures. Due to lower junction temperature, narrow JFET width avoid thermal generated current. Furthermore, in the same manner as thin gate oxide, low temperatures lead to reduced FN tunneling, resulting in the low gate leakage current. However, unlike reduced gate oxide, narrow JFET width has high dV_{gs}/dt, contributing to the large reduction in saturation current during the SC event. As a result, maximum junction temperature decreases (Fig. 11(a)), contributing to the decrease in ΔV_{gs} (Fig. 11(b)), thanks to the suppression of FN tunneling. Temperature distribution in SiC with different JFET width at the short-circuit time of 5 µs is shown in Fig. 13. The MOSFET with JFET width of 0.3 µm has largely lower junction and surface temperatures when compared with that with JFET width of 0.7 µm. Temperature rise beneath gate oxide, especially near n+ source, is significantly lower with narrow JFET width, allowing the reduction in FN tunneling.

Figure 13 and Table II summarize the simulated results. When using reduced JFET width, short-circuit capability is improved from 6.8 to 13.7 µs, as shown in Fig. 11 (b) and Fig. 13. Not only static (lower $R_{on,sp}$, lower maximum electric field in gate oxide, and higher breakdown voltage) and dynamic (high dV_{gs}/dt) performance, but also SC capability (longer t_{sc}, lower I_{sat}, reduced $T_{j,max}$) is improved when using SiC MOFSET with narrow JFET regions with increased JFET doping concentration.

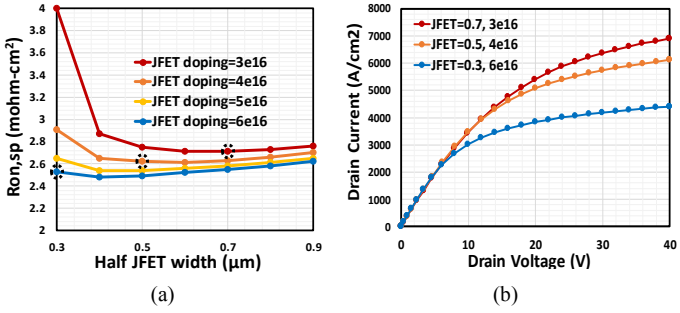
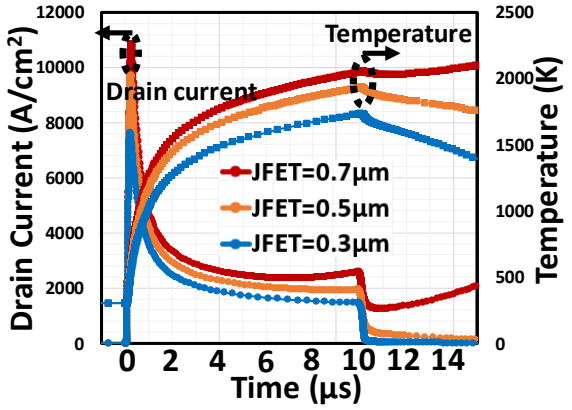
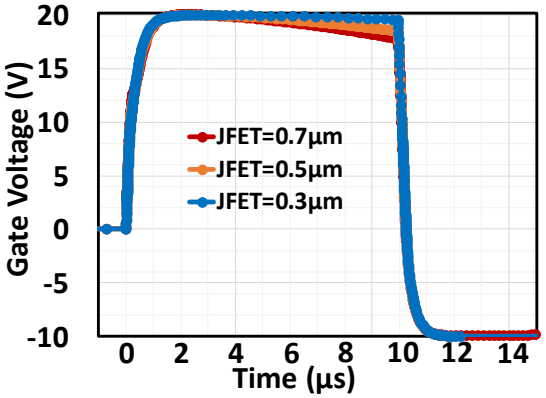


Figure 10. (a) Ron,sp as function of JFET width with different JFET doping concentration and (b) output characteristics with different JFET width.



(a)



(b)

Figure 11. (a) Simulated drain current and maximum junction temperature in SiC and (b) gate voltage.

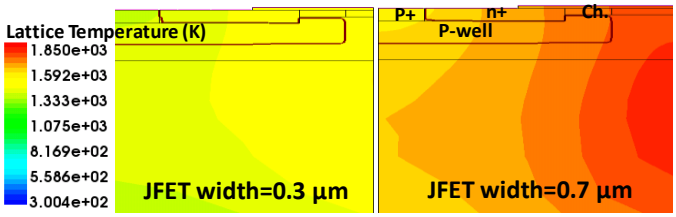


Figure 12. Temperature distribution of half JFET width=0.3 and 0.7 µm.

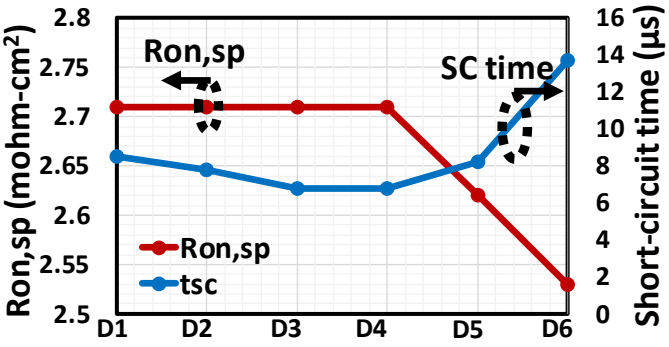


Figure 13. Summary of simulation results for t_{sc} and $R_{on,sp}$.

Table II. Summary of simulated results.

	Tox (nm)	W_{JFET} (µm)	JFET doping (cm^{-3})	Vgs (V)	Ron,sp (mΩ -cm^2)	BV (V)	Eox (MV /cm)	t_{sc} (µs)
1	20	0.7	3×10^{16}	10	2.71	1652	3.39	8.5
2	30	0.7	3×10^{16}	13.3	2.71	1662	3.26	7.8
3	40	0.7	3×10^{16}	16.6	2.71	1659	3.15	6.8
4	50	0.7	3×10^{16}	20	2.71	1660	3.04	6.8
5	50	0.5	4×10^{16}	20	2.62	1677	2.3	8.2
6	50	0.3	6×10^{16}	20	2.53	1690	1.47	13.7

VI. CONCLUSIONS

Non-Isothermal simulation for SC capability is performed to examine different types of SiC MOSFET structures. To obtain exact simulation results, thermal-related simulation models are developed and optimized. Thin gate oxide slightly increases short-circuit time while maintaining specific on-resistance due to reduced saturation current. However, the reduced gate oxide approach has drawbacks due to the increase in input capacitance, resulting in slow dV_{gs}/dt. Moreover, the MOSFET with thin gate oxide has higher electric field in the gate oxide when compared to MOSFET with thicker gate oxide. Ultimately, it is demonstrated in Non-Isothermal simulation that reduced JFET width with increased JFET doping concentration largely enhances both static performances and short-circuit capability of SiC MOSFETs.

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