Static Performance and Reliability of 4H-SiC Diodes with P+ Regions Formed by Various Profiles and Temperatures

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***Abstract*— Several designs of 1.2kV-rated 4H-SiC PiN diodes and Junction Barrier Schottky (JBS) diodes have been successfully fabricated with various P+ implantation conditions resulting in different junction profiles. P+ regions were implanted at both room temperature and elevated temperature (600˚C) to monitor the generation of Basal Plane Dislocations (BPDs) and study their impact on device long term reliability. It was found that, when the dose in the deeper portion of the junction (implemented by high energy implantations) is well suppressed, static and long-term reliability performances of room temperature implanted devices can be maintained similar to those of high temperature implanted devices.**

Keywords- 4H-Silicon Carbide (SiC), PiN Diode, Junction Barrier Schottky Diode, Leakage Current, Breakdown Voltage, Room Temperature Implantation, Current Stress, X-Ray Topography.

I. INTRODUCTION

The wide bandgap of 4H-SiC offers many benefits over Silicon for being the material of choice in high voltage power devices. Due to the large bandgap and ability to withstand high electric fields, 4H-SiC power devices can be designed using a thin but heavily doped epitaxial drift layer, resulting in significantly smaller resistance when compared to traditional Silicon at voltage ratings greater than or equal to 600V. Although 4H-SiC is a preferred material for high voltage devices, the material itself brings about unique challenges in processing techniques that are not seen in traditional Silicon devices. In Silicon processing, ion implantation is a low temperature process, which allows a photoresist to be used as the implant masking layer [1]. However, ion implantation of Aluminum (Al) in conventional 4H-SiC technology has been performed at elevated temperatures to mitigate the formation of Basal Plane Dislocations (BPDs) that can lead to device degradation when converted into stacking faults (SFs) under high bipolar current stress [2]. This high temperature (~600˚C) ion implantation requires the use of an oxide blocking layer, as the photoresist would not withstand the elevated temperature, therefore increasing processing time, cost, and complexity [3].

Due to the processing benefits, there have been studies to implement room temperature ion implantation without generating severe crystal damage such as BPDs. While the critical dose, 1×10^{15} cm^{-2}, of Al implantation that allows RT implantation has been studied in previous research [4], the impact of implantation energy and dose altogether, i.e., the profile, was not studied in greater detail. By properly optimizing the overall dopant profile, potential BPD generation from the ion bombardment during RT implantation can be mitigated and thus device reliability and lifetime will improve [2]. In this study, both PiN diodes and JBS diodes were investigated to elucidate the effects of this P+ implantation process.

II. DEVICE DESIGN AND DESCRIPTION

A. Active Area Design

Fig. 1 shows simplified layouts and cross-sectional views of the fabricated PiN and JBS diodes with 4.5mm^2 active area. To ensure adequate current density and low leakage current in the JBS diode, simulations were conducted to determine an optimal Schottky width of 2µm. For the PiN diode, P+ implantation was performed over the entirety of the active area, whereas the JBS diode contains P+ implanted regions over 50% of the active area due to the repeating stripe patterns to shield the Schottky contact during the blocking mode of operation. Fig. 2 shows four different P+ implantation profiles used in this study, where the profiles are varied with high (H), medium (M), and low (L) in concentration for the surface (S) and body (B) of the junction. The 'LSLB (meaning Low Surface Low Body in doping)' (simply '1x'), 'MSHB' ('5x'), and 'HSMB' ('9x') has a total Al dose of 1×10^{15} cm^{-2}, 5×10^{15} cm^{-2}, and 9×10^{15} cm^{-2}, respectively, while the 'RT Box' profile has uniform surface and body concentration with a total Al dose of 5×10^{15} cm^{-2}. All implants were performed at room temperature however, the '1x' and '5x' P+ profiles were also implanted at elevated

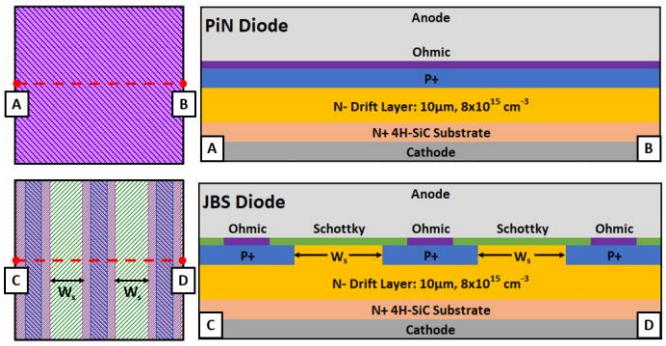

Figure 1. *Top and cross sectional views of the 4H-SiC PiN Diode (top) and JBS Diode (bottom) used in this study. Optimal Ws for JBS diode was determined to be 2µm.*

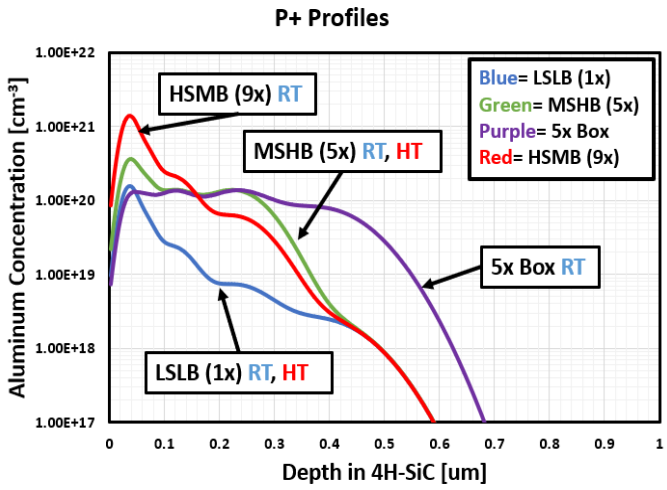

Figure 2. *Aluminum concentration profiles used in the various P+ regions. All profiles were implanted at room temperature. LSLB (1x) and MSHB (5x) conditions were also implanted at high temperature of 600˚C. Profiles were constructed using SRIM simulations.*

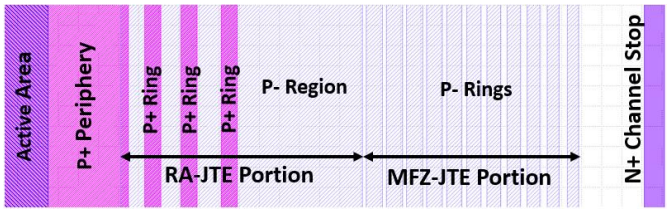

Figure 3. *Design of the Hybrid JTE edge termination used to ensure near ideal breakdown voltage and minimal leakage current. Main components and P+ regions of the hybrid JTE edge termination are labeled. JTE and N+ regions were implanted at room temperature (25˚C).*

temperatures of 600˚C (HT) for the comparison purpose.

B. Edge Termination Design

An n-epitaxial drift layer with a thickness of 10µm and a nitrogen doping concentration of $8x10^{15}cm^{-3}$ was designed to provide the devices with a near ideal parallel plane breakdown voltage. To further ensure near ideal breakdown, a 'hybrid edge termination' structure was used [5]. This edge termination structure combines the strengths of both the Ring Assisted Junction Termination Extension (RA-JTE) and the Multiple Floating Zone Junction Termination Extension (MFZ-JTE) structures providing a wide range of JTE dose to ensure high breakdown voltages [5]. Fig. 3 shows a top view schematic of the hybrid edge termination in which each portion of the edge termination structure was optimized using 2-D device simulations.

The RA-JTE portion in the hybrid edge termination structure consists of multiple ('n') P+ concentric rings with a width of 'w', where the first ring is placed near the main junction with a spacing of 'S_o', followed by other rings with incremental spacing of 'S_i', all within the JTE implanted area with a width 'W_{jte}'. Each ring spacing is described by the equation $S_n=S_o+S_i(n-1)$ where S_n is the spacing between the P+ rings with respect to the ring number. These optimal parameters used for S_o, S_i, n, W and W_{jte} are 4, 1, 3, 4, and 60µm, respectively. For the MFZ-JTE portion, gradually decreasing JTE zone widths are utilized described by the equation $W_n=W_1/\alpha^{(n-1)}$, where n denotes the ring number; W_n corresponds with the width in the n_{th} zone; and α denotes a decreasing parameter [5]. The optimal parameters used for n, W_1 and α are 11, 5 and 1.05, respectively. All the diodes used the same hybrid edge termination structure with an exception of the implantation profiles of the P+ rings within the RA-JTE portion.

III. Device Fabrication

Several 4.5mm^2, 10A rated 1.2kV 4H-SiC PiN and JBS Diodes were fabricated all on the same wafer using the same process flow. A heavily doped N+ buffer layer followed by a 10µm thick, $8x10^{15}cm^{-3}$ n-doped epitaxial layer grown on 4H-SiC substrates was used to accommodate the 1.2kV voltage rating as discussed in the previous section. Aluminum and Nitrogen were used for the formation of the P+/JTE and N+ channel stop regions, respectively. The '1x' and '5x' P+ profiles were implanted at the elevated temperature of 600˚C (HT) in addition to a RT condition to minimize any potential lattice damage and subsequent BPD generation during the implantation process. All other implants were performed at room temperature. After the implantation process, a carbon capping layer was applied to reduce surface deterioration while performing the activation anneal at 1650˚C for 10 minutes [6].

After the activation annealing process an interlayer dielectric was uniformly deposited and patterned to open ohmic contact areas. The Ohmic contacts were then formed by depositing Nickel (Ni) followed by the formation of a Ni silicide by undergoing 750°C anneal for 2 minutes by utilizing a rapid thermal anneal (RTA) to partially form the frontside ohmic contacts. The remaining Ni that did not form the silicide with SiC was then stripped. The cathode electrode was formed by depositing Ni on the backside of the wafer, followed by annealing all Ni at 965°C for 2 minutes using an RTA process, forming the ohmic contacts on both the frontside and backside of the wafer. Schottky contact areas in the JBS diodes were then opened using a wet etch in buffered oxide etch (BOE) followed by a Titanium deposition to form a Schottky contact on the n-epitaxial drift layer [7]. After the Schottky contact process, a thin layer of Titanium Nitride (TiN) followed by a 4µm thick Al layer was deposited and patterned by subtractive etch to form the anode contacts for the various diodes. To finalize the fabrication process, the frontside was passivated using a nitride followed by the deposition and etch of a thick polyimide layer.

IV. Data/Results and Discussion

A. X-Ray Topography Analysis

Grazing incidence monochromatic X-Ray topographs were recorded on high resolution X-ray films from the 4H-SiC device wafers at 1-BM, Advanced Photon Source at Argonne National Laboratory. BPDs from each P+ implantation condition are observed in Fig. 4 and Fig. 5, for both the PiN and JBS diodes, respectively. From these X-Ray topography images, '1x' conditions, '5x HT', and '9x RT' all show relatively low BPD damage throughout the entire device structure. However, in the '5x RT' implanted devices, BPD generation can be observed around the P+ rings and periphery region within the device layouts for both the PiN and JBS diodes, therefore this BPD generation was process related as opposed to being native to the starting material. The BPD generation can be observed to a greater extent in the '5x RT Box' devices with a larger density when compared to the previous conditions in the edge termination of the devices and within the P+ stripes of the JBS diode active area.

It is believed that BPD generation is triggered at the edge of the implantation region due to the unplanted regions being

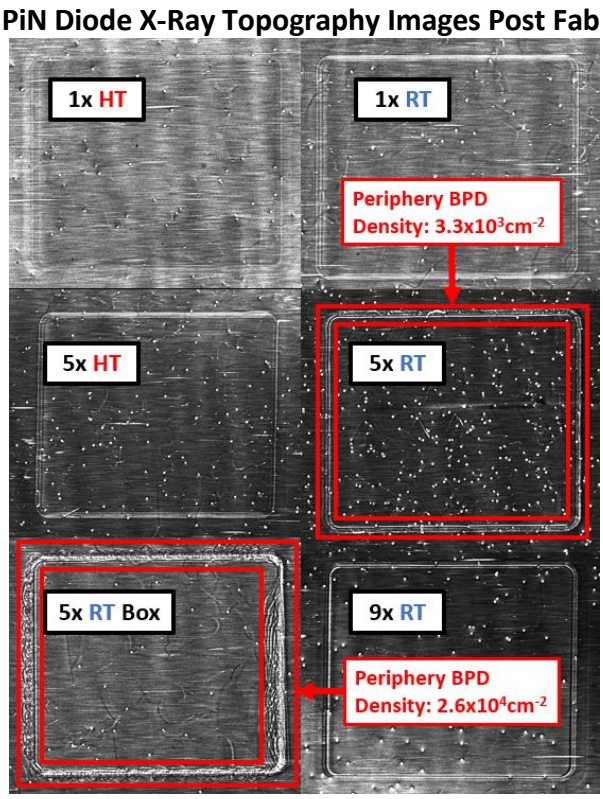

Figure 4. Post fabrication *X-Ray topography images of the PiN diodes with various P+ implantation conditions. Areas of high BPD generation within the edge terminations for both the '5x RT' and '5x RT Box' conditions are highlighted in red.*

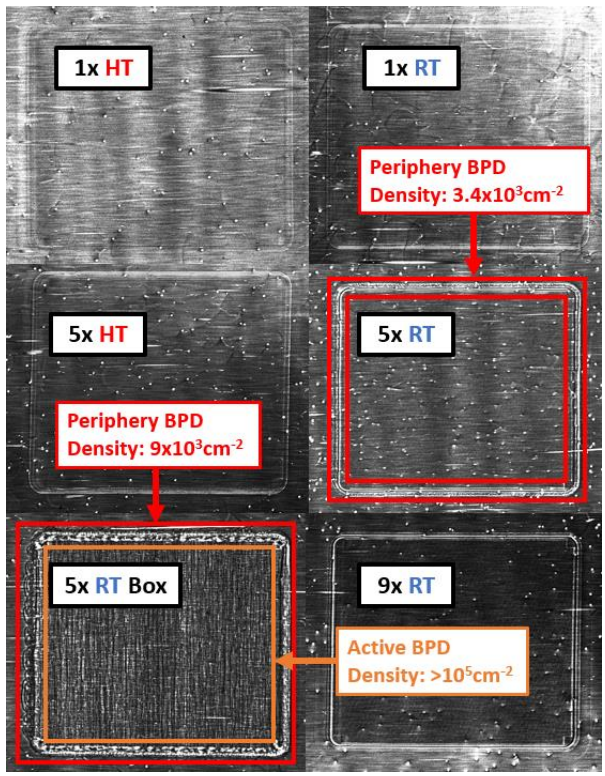

Figure 5. Post fabrication *X-Ray topography images of the JBS diodes with various P+ implantation conditions. Areas of high BPD generation within the edge termination for the '5x RT' and the '5x RT Box' conditions, and active area for the '5x RT Box' condition are highlighted in red and orange respectively.*

subject to compressive stresses during the activation anneal process after the ion implantation process [8]. Therefore, considering the device layout of the PiN and JBS diodes, it can be seen that the BPDs observed are located in the peripheral region where the P+ region ends, and the alternating P+ stripe pattern in the JBS diode, however are not seen within the PiN diodes with blanket P+ implantations over the entire active area.

BPD densities at the edge termination region for the '9x RT', '5x RT', and '5x RT Box' P+ implanted conditions were found to be $2.1x10^3$ cm^{-2}, $3.3x10^3$ cm^{-2}, and $2.6x10^4$ cm^{-2}, respectively for the PiN diodes and $1.9x10^3$ cm^{-2}, $3.4x10^3$ cm^{-2}, and $9.0x10^3$ cm^{-2}, respectively for the JBS diodes. Due to the very high density of BPDs within the active area of the '5x RT Box' JBS diode, the exact amount of BPDs was not able to be determined, however was estimated to be greater than 10^5 cm^{-2}. The BPD densities were calculated based on the BPD nucleation from device edges and assuming the entire device volume.

The creation of the '5x RT Box' profile uses greater doses at its higher energy implants when compared to the '5x' profile. The '9x' profile, however, while containing nearly 2x the total dose as the '5x' condition, uses higher doses at a lower energy implant. Overall, it is concluded that not only does total dose and temperature play a role in BPD generation, but the energy of each implant and thus the profile is also a vital component to consider for the P+ implantation.

B. Static Device Performance

Fig. 6 and Table I show typical IV curves and statistical values for PiN and JBS diodes implanted at various P+ conditions. For PiN diodes, the forward IV characteristics for the '5x' and '9x' conditions, regardless of the implant temperature, offer near optimal performance, while '5x Box RT' and to a greater extent the'1x' conditions produce higher resistances. These device characteristics reflect the P+ contact resistance; P+ conditions with a lower doping near the surface result in a higher contact resistance, and thus higher overall resistance in the forward IV as observed in Fig. 7.

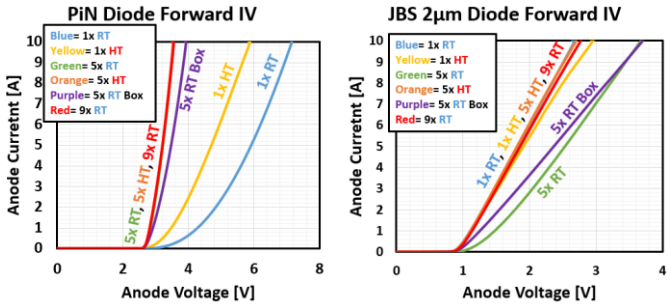

Figure 6. *Typical forward IV performances of various PiN diodes (Left) and Nominal JBS diodes (Right). All IV characteristics were measured on wafer and at room temperature (25˚C).*

Table I. *Average and standard deviation of forward voltage drop at 10A for 26 PiN and JBS Diodes at each P+ implantation condition. All devices were measured at room temperature (25˚C) and on wafer.*

P+ Condition	PiN Diode		JBS Diode	
	Average V_f @ 10A [V]	Std Dev [V]	Average V_f @ 10A [V]	Std Dev [V]
1x HT	6.07	0.11	1.73	0.03
1x RT	7.15	0.16	1.71	0.05
5x HT	3.51	0.04	1.73	0.07
5x RT	3.65	0.28	2.65	0.24
5x RT Box	4.11	0.22	2.88	0.26
9x RT	3.49	0.09	1.90	0.11

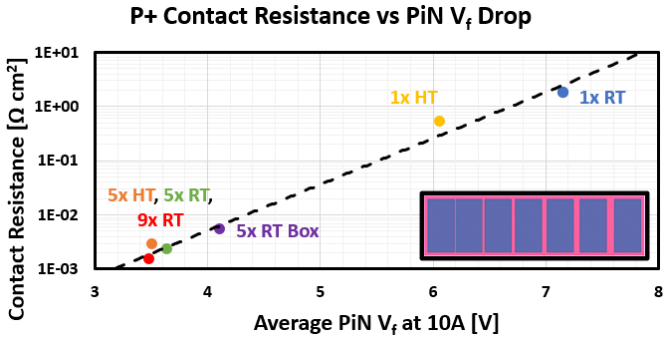

Figure 7. *Correlation between the average PiN forward voltage drop at 10A for each P+ implantation condition and the average P+ contact resistance. Devices with higher surface doping concentrations contain lower resistance when compared to their lower surface concentration counterparts. Contact resistance was measured on wafer and at 25˚C, using a bar type TLM structure.*

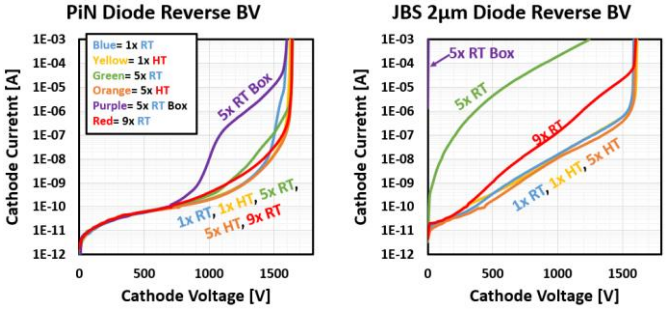

Figure 8. *Typical blocking behaviors of various PiN diodes (Left) and Nominal JBS diodes (Right). All curves were measured on wafer and at room temperature (25˚C).*

Table II. *Breakdown voltage average and standard deviation for 26 PiN and JBS Diodes at each P+ implantation condition. Breakdown voltage was determined once the device reached a cathode current of 1mA. All devices were measured at room temperature and on wafer.*

P+ Condition	PiN Diode		JBS Diode	
	Average BV [V]	Std Dev [V]	Average BV [V]	Std Dev [V]
1x HT	1631	12.16	1595	2.79
1x RT	1629	3.27	1605	14.16
5x HT	1640	3.93	1600	18.39
5x RT	1643	5.81	1157	160.2
5x RT Box	1610	9.91	N/A	N/A
9x RT	1644	5.78	1548	87.47

The forward characteristics of the JBS diodes with various P+ implant conditions show similar IV characteristics with the exception of the '5x RT' and '5x Box RT' conditions. Thesetwo conditions contain poorer forward conduction performances, coupled with higher standard deviations and thus a larger variation in the forward voltage drop (V_f). From the X-Ray topography analysis, it is expected that a greater number of random defects including BPDs inside the active area of the JBS diodes resulted in the larger variations observed in the devices [9]. However, the '9x RT' does not show this poorer forward conduction behavior and large variations as the number of defects within this implantation remained relatively low, similar to the HT and low dose implantation conditions.

Fig. 8 and Table II show typical blocking behavior curves and statistical values measured from PiN and JBS diodes utilizing the hybrid edge termination structure. Devices implanted at RT resulted in a larger leakage current during the blocking mode of operation. This larger leakage becomes more prominent for the '5x RT' and '5x RT Box' implanted devices than the '1x RT' and '9x RT' implanted devices. This trend is more clearly observed in the leakage curves measured from various JBS diodes as low dose and HT implantations show near optimal blocking characteristics, however, the '5x RT' shows increased leakage current and the '5x RT Box' condition shows no blocking capabilities.

From the observations in this study, the high density of process-induced BPDs shows a strong correlation between devices configured with large reverse leakage currents. There have been studies correlating leakage current with BPDs in devices [10]. However, further studies are required to elucidate the exact mechanism of leakage current generation in PiN and JBS diodes due to process induced BPDs.

C. Current Stress Measurement Performance

For long term reliability study, all fabricated devices were stressed at 125A/cm^2 over the course of 90 minutes and device performance was measured after every 15 minutes at room temperature. The PiN diodes forward IV behavior can be observed in Fig. 9 after 125A/cm^2 stress measurements. As shown, both the '5x RT' and '5x RT Box' conditions showed considerable degradations, while '1x', '5x HT', and '9x RT' implantations resulted in no degradation over the course of the 90 minutes. '5x RT Box' showed much more severe degradation and the 125A/cm^2 current stress measurements were halted on those devices after 30 minutes due to a ~135% increase in V_f.

Similar trends can be observed also in the reverse leakage curves, as shown in Fig. 10, where '1x', '5x HT', '9x RT' conditions showed negligible change in leakage current post stress, whereas '5x RT' and '5x RT Box' showed an increase of leakage current by several orders of magnitude. Once again,

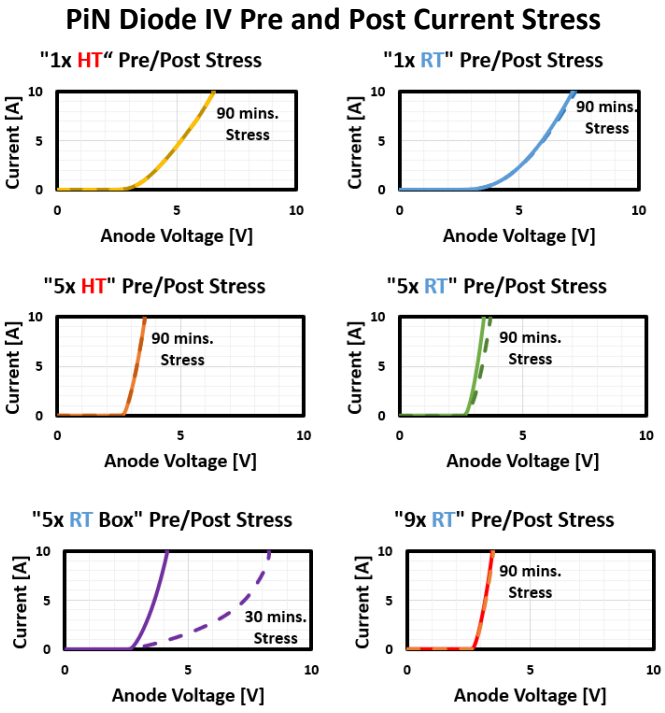

Figure 9. *Comparison of forward IV curves of various PiN diodes pre (Solid) and post (Dashed) 125A/cm^2 current stress for 90 minutes with exception of the '5x RT Box' condiotion which was halted after 30 minutes.*

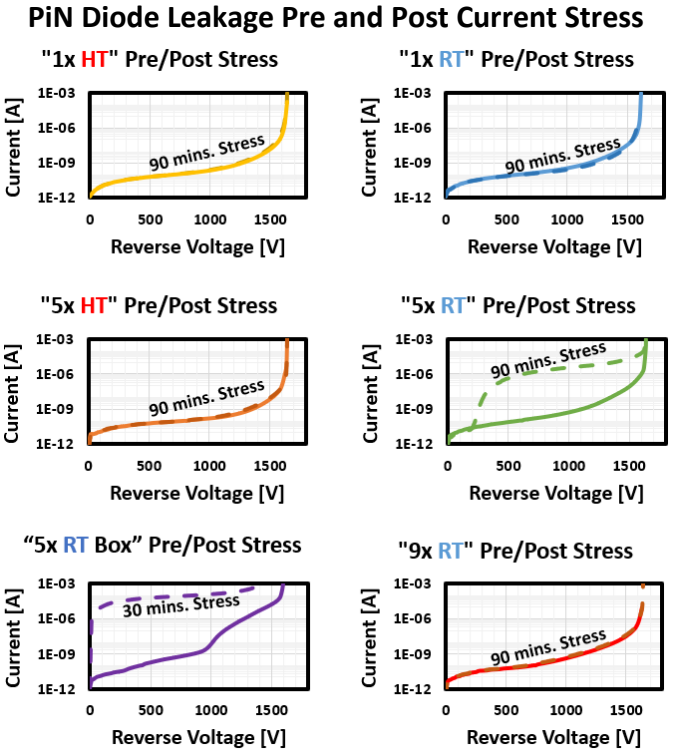

Figure 10. *Comparison of reverse blocking behaviors of various PiN diodes pre (Solid) and post (Dashed) 125A/cm² current stress for 90 minutes with exception of the '5x RT Box' condition which was halted after 30 minutes.*

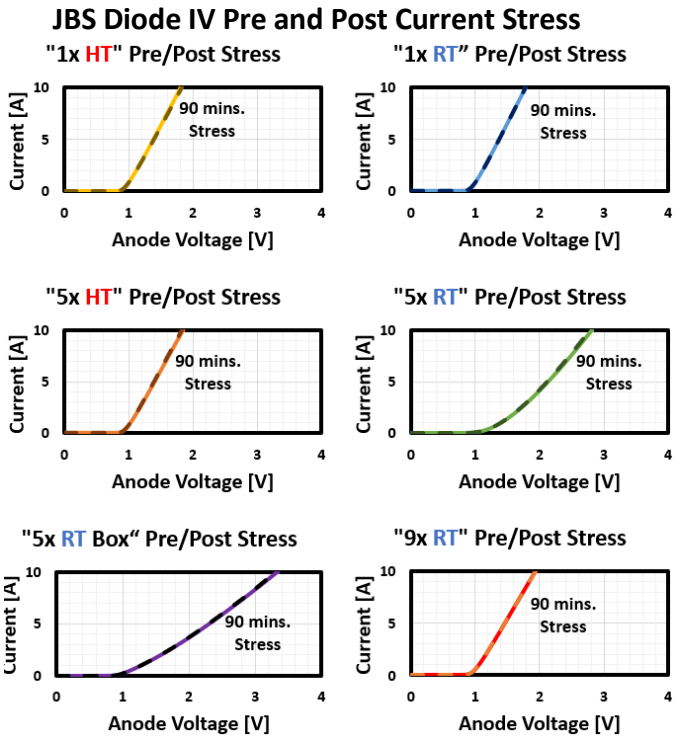

Figure 11. *Comparison of forward IV curves of various JBS diodes pre (Solid) and post (Dashed) 125A/cm² current stress for 90 minutes. No change in the forward conduction can be observed following the current stress condition.*

the '5x RT Box', which contains greater doses at its higher energy implants, shows a severe shift in its blocking capabilities after only 30 minutes compared to the 90 minutes for other devices.

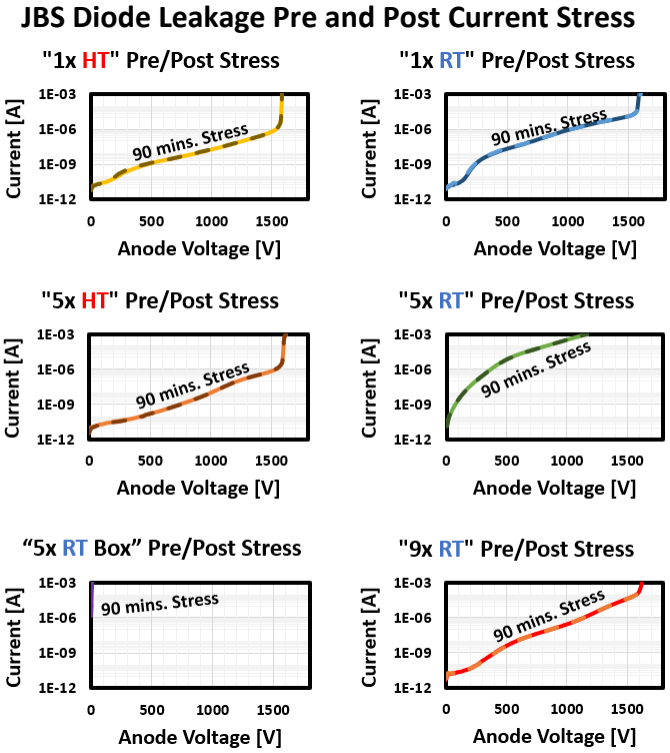

Figure 12. *Comparison of reverse blocking behaviors of various JBS diodes pre (Solid) and post (Dashed) 125A/cm² current stress for 90 minutes. No change in the forward conduction can be observed following the current stress condition.*

The stress measurement from the various PiN diodes follows the same trends observed in both forward and reverse current- voltage characteristics as well as the BPD density within the structure. In other words, the '9x RT' condition showed almost no degradation similar to '1x' and '5x HT' conditions as shown in Fig. 9 and Fig. 10. This can be attributed to the lower BPD density generation as previously discussed, therefore, limiting SF expansion. However, the '5x RT' and '5x RT Box' profiles both contained higher BPD densities when compared to the other conditions resulting in larger amounts of degradation in both the forward and reverse blocking behaviors. Therefore, the energy and dose combination of RT implant is a key component to consider in designing P+ implantation.

For the JBS diodes, no degradation following the same 125A/cm² current stress measurements were observed in both the forward conduction and reverse leakage curves as seen in Fig. 11 and Fig. 12, respectively. Even within high BPD density devices such as the '5x RT' and to a greater extent the '5x RT Box' implanted devices, degradation was not observed unlike its PiN counterpart. This can be attributed to the unipolar behavior of JBS diodes as the V_f drop across the device is less than the P/N junction turn on voltage of ~2.7V. This lack of bipolar current prevents electron hole recombination utilizing the BPDs, subsequently preventing SF expansion and device degradation. However, it should be emphasized that severe lattice damage produced by high dose, high energy implantations such as '5x RT' and '5x RT Box' conditions already degrade (pre Stress) IV performance that is possibly attributed to the constricted and damaged current path between two adjacent P+ grids.

V. CONCLUSIONS

Low dose implantations such as the '1x' conditions (both RT and HT) and implantations performed at elevated temperatures (HT) resulted in a negligible amount of BPD generation and degradation post current stress. However, to ensure proper device performances, a higher dose implantation such as the '5x' and '9x' conditions is preferred to reduce the contact resistance and therefore lower the voltage drop across the diode. However, these higher doses can lead to greater lattice damage (such as BPDs) and device degradation if the profile is not designed properly, while simultaneously being implanted at RT. It was found that, while utilizing these higher net dose conditions, by increasing the dose at lower energies and reducing the dose at higher energies, to create an implant profile with high surface and lower body concentration (i.e.,'9x'), the subsequent damage and BPD generation is well suppressed, along with no effect on the device static performances and long-term reliability through device degradation under bipolar current stress. Proper control of the implantation condition and profiles are necessary to minimize the BPD generation to fully implement RT implantations, therefore increasing device reliability and longevity, while simultaneously reducing processing time, energy, cost, and complexity.

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