Threshold Voltage Instability of Commercial 1.2 kV SiC Power MOSFETs

Susanna Yu, Tianshi Liu, Shengnan Zhu, Diang Xing, Arash Salemi, Minseok Kang,
Kristen Booth, Marvin H. White, and Anant K. Agarwal
Department of Electrical and Computer Engineering
The Ohio State University
Columbus, USA
1-919-397-4673, yu.2452@osu.edu

***Abstract*—This paper presents threshold voltage instability of commercially available 1.2 kV SiC power MOSFETs from multiple vendors. Time-dependent bias-stress measurements are implemented to define the threshold voltage change incurred by near interface oxide traps. Bias-stress on the gate gives rise to injection of carriers into the gate oxide by direct tunneling to the near interface traps. Positive gate bias tends to increase threshold, whereas, negative gate bias tends to decrease threshold voltage. Threshold voltage shifts for various vendors vary from 0.15 V to 0.74 V under bias-stress of +30 V, and -0.05 V to -0.2 V under bias-stress of -10 V for 50 hours. This wide variation in the shifts between vendors indicates the different trap distribution in their oxides. In general, a positive threshold voltage shift decreases current drive, while a negative shift can cause the device to move into an ON state. However, the shift by itself does not represent an operational problem in power electronics but signifies the high density of defects in the gate oxide which may have significance for useful lifetime of gate oxides.**

***Index Terms*— Gate oxide reliability, Near-interface traps, Silicon Carbide MOSFET, Threshold voltage instability.**

I. INTRODUCTION

The remarkable material properties of Silicon Carbide (SiC), such as wide bandgap, high critical electric field, and high thermal conductivity, have enabled SiC MOSFETs to become promising switching devices for high-temperature and high-power applications [1], [2]. Despite the material advantages, Metal-Oxide-Semiconductor (MOS)-based SiC devices lack ruggedness due to a high density of traps and charges at or near the interface of SiC/SiO_2 [3]. Furthermore, a high density of interface states is a major cause of low effective inversion layer mobility in SiC MOSFETs, which results in a reduced current drive and a high channel resistance [4]. Significant progress has been made to improve gate oxide quality with the development of post-oxidation techniques such as NO, N_2O, and $POCl_3$ [5]-[8]. However, the interface state density in SiC MOSFETs is still much higher than that of Si devices and the origins of these states are not fully understood [9].

The threshold voltage is affected by interface states since, in strong inversion, these states are negatively charged due to the capture of electrons. In addition to interface states, near-interfacial oxide traps (NIOTs), also known as border traps, give rise to threshold voltage instability [10]-[13]. NIOTs can be determined by time-dependent bias-stress measurements. Over a wide range of time, under bias-stress, we examine gate oxide reliability with carrier injection into NIOTs. Under a high positive DC bias applied to the gate, electrons in the conduction band (CB) of SiC are injected into NIOTs by tunneling. In addition, holes back-tunnel from traps in the oxide to the valence band (VB) in SiC resulting in a net positive threshold voltage shift. Conversely, when a negative DC bias is applied, the threshold voltage shifts in the negative direction as electrons back-tunnel into the CB with hole injection from the VB. This may place devices into a normally-on state, especially in the devices with a low threshold voltage. Thus, it is important to study the threshold voltage instability in the commercial devices to determine their robustness for automotive applications which require stringent reliability requirements. In this work, we examine the threshold voltage instability of Power MOSFETs under both positive and negative DC bias-stresses at room temperature in commercially available 1.2 kV SiC MOSFETs and discuss the charge trapping behavior in the oxide.

TABLE I. DEVICES UNDER TESTS (DUTS).

Vendor	Gate structure	Voltage rating	Current rating
C	Planar MOSFET	1.2 kV	10-20 A
D	Trench MOSFET		
D'	Planar MOSFET		
E'	Planar MOSFET		
I	Planar MOSFET		

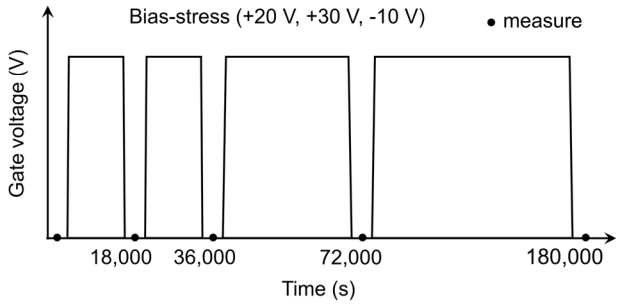

Figure 1. Bias-stress and threshold voltage measurement condition.

978-1-7281-3199-3/20/$31.00 ©2020 IEEE

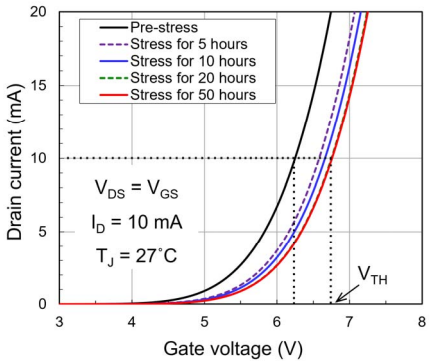

Figure 2. Constant-current (CC) method implemented on I_D-V_G transfer characteristics of the device C at various stress times.

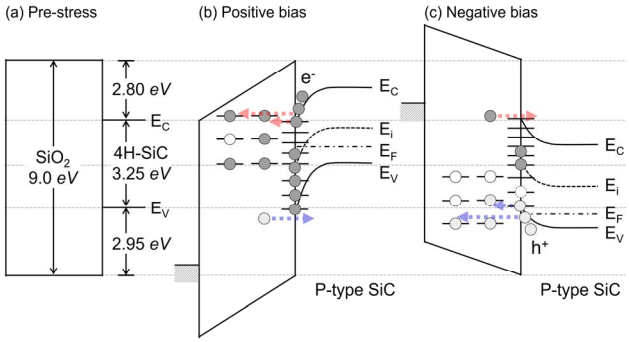

Figure 3. Band diagrams of MOS structure under (a) equilibrium, (b) positive, and (c) negative gate bias conditions.

II. Experiments

Threshold voltage instability measurements were performed with commercially available 1.2 kV SiC MOSFETs from different vendors. Devices Under Test (DUTs) are listed in Table I. Test circuit was fabricated to apply bias-stress on the gate with the remaining terminals grounded on 25 devices at the same time. Fig. 1 depicts the sequence for time-dependent threshold voltage instability measurement. Both positive (+20 V, +30 V) and negative (-10 V) gate bias-stresses were used. Before and after each bias-stress, for 5, 10, 20, and 50 hours, the threshold voltage was measured with an Agilent 4145 parameter analyzer. The traps being monitored are NIOTs with slow response time; therefore, a Constant-Current (CC) method was employed to evaluate the threshold voltage where the gate voltage is required to flow10 mA of drain current (See Fig. 2) [14].

This is a slow measurement, which allows charges injected during stressing to emit from traps in the interval between the end of bias-stress and measurement of threshold voltage. Unlike fast measurements, where most of the occupied traps even in the vicinity of the interface are observable, slow measurements give information on the injected charges that do not move from the deeper traps at a given recovery time [15]. Due to slow time scale, the measurements are sensitive to oxide traps near the interface but not to traps at the interface. Threshold voltage instability arises due to the capture of carriers by these traps as illustrated by energy band diagrams in Fig. 3. During positive bias-stress, electrons are injected into the NIOTs from the inversion layer in the CB via band-to-trap tunneling as depicted in Fig. 3 (b). The injection efficiency is determined by the tunneling probability, electric field, and the barrier height as a function of time [10]. As stress time increases, carriers are injected into the deeper traps in the oxide. These trapped electrons increase the threshold voltage. Similarly, previously trapped holes may tunnel back into SiC VB. Under a negative bias-stress, as shown in Fig. 3 (c), accumulated holes are injected from the VB into oxide traps while previously trapped electrons back-tunnel into the CB, thus resulting in a net negative shift in threshold voltage.

Fig. 4 shows time-dependent threshold voltage shifts with various bias-stresses. Error bars at each point represent the variation in 5 devices. The value for threshold voltage shift was determined by subtracting pre-stress threshold voltage from post-stress threshold voltage. When a positive DC bias of +20 V is applied to the gate for 50 hours, the threshold voltage shifts are 0.50 V, 0.35 V, 0.16 V, 0.06 V and 0.10 V for devices from vendor C, D, D', E', and I respectively (see Fig. 4 (a)). The largest threshold voltage shift was found in devices from vendor C (device C). The threshold voltage values are found to saturate in 20 hours in most cases. For the DC bias of +30 V, again devices from vendor C (device C) show the largest amount of shift about 0.74 V after 50 hours of stress. Most of vendors show the similar trend in threshold voltage shift with different bias-stresses. However, devices from vendor E'

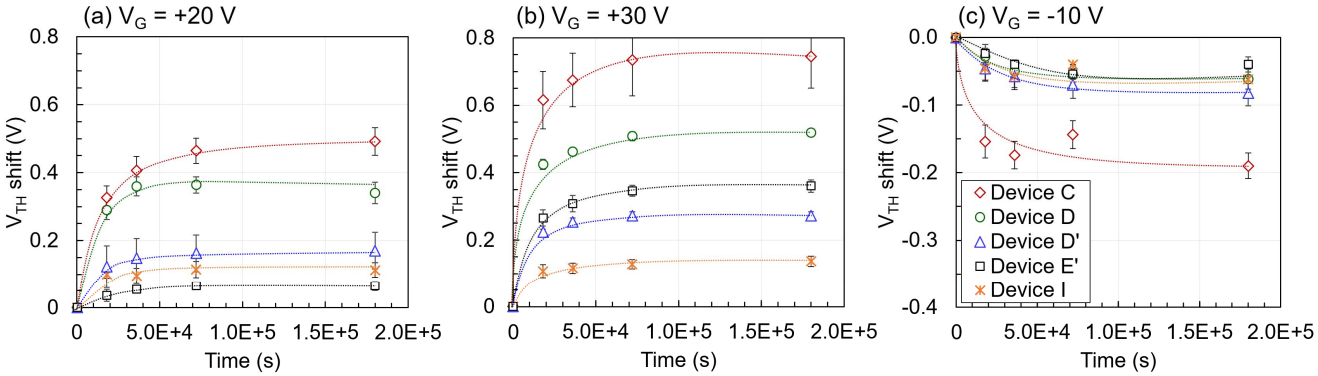

Figure 4. Time-dependent threshold voltage shifts for (a) positive bias-stress of +20 V, (b) +30 V, and (c) negative bias-stress of -10 V for 50 hours. The error bars represent the spread of 5 devices measured for each vendor.

(device E') which show the smallest shift at the bias-stress of +20 V now have higher threshold voltage shift of about 0.35 V than devices from vendor I (device I) and vendor D' (device D') (see Fig. 4 (b)). This indicates that trap distribution near the oxide in device E' is not uniform. Conversely, when a negative bias of -10 V is applied to the gate for 50 hours, the threshold voltage shifts in the negative direction. The maximum shift about -0.2 V is shown in device C while others show less than -0.1 V shift. Thus, for traps measured within the time scale of the measurements, we conclude that device C has the most number of NIOTs (see Fig. 4 (c)). Considerable variance between devices from different vendors implies that some vendors have been able to significantly reduce the NIOTs in the gate oxide.

III. Results and Discussion

When gate voltage is applied, the voltage drop across an ideal MOS gate structure is described by

$$V_G = \phi_{GS} + V_{ox} + \phi_s \tag{1}$$

where ϕ_{GS} is the gate-semiconductor work function difference, V_{ox} is the voltage across the insulator, and ϕ_s is the surface potential. V_{ox} is the product of oxide thickness (x_o) and the oxide electric field (ε_{ox}). If we consider electron injection into the oxide and trapping in the interface states, (1) becomes

$$V_G = \phi_{GS} - Q_s/C_{ox} + \phi_s + \frac{qD_{it}(\phi_s - \phi_F)}{C_{ox}} + \frac{qN_T}{C_{ox}} - \frac{Q_F}{C_{ox}} \tag{2}$$

where Q_s is the total charge in the semiconductor, D_{it} is an assumed constant interface state density ($cm^{-2}eV^{-1}$), ϕ_F is the potential difference between the Fermi level and the intrinsic level of the bulk, x_T is the tunneling distance to which interface traps are filled by direct tunneling, N_T is the number of NIOTs per unit area, and Q_F is the fixed oxide charge in the gate oxide. Here we neglect oxide field relaxation due to filled NIOTs. The fourth term in (2) depicts charges in interface states. The value of D_{it} appears not to change significantly as monitored with subthreshold measurements. The fifth term describes NIOTs and determines the threshold shift when $\phi_s = 2\phi_F$. Therefore, the large threshold voltage shift of device C in Fig. 4 implies higher N_T.

In a power MOSFET, under positive gate bias-stress, carrier injection into the oxide occurs at N^+ source, P-well and JFET as illustrated with the cross-section in Fig. 5. Energy band diagrams in Figs. 5 (a) and (b) show the voltage drops in the MOS structures at N^+ source and P-well region under gate bias of +20 V. In the case of N^+ source region in Fig. 5 (a), voltage drop across the oxide is higher than that of P-well region since N^+ source is in accumulation mode under positive bias. Consequently, ϕ_s consumes a very small part of applied voltage and therefore most of voltage drop is in V_{ox} as described in (1), while ϕ_{GS} remains the same. JFET region is similar to the case of N^+ source but less doping concentration gives slightly lower V_{ox}. On the other hand, P-well region in Fig. 5 (b) shows smaller V_{ox} since ϕ_s is required to be large to first achieve the depletion then invert the surface to form the channel. Therefore, the carrier injection is the highest over the N^+ source, then JFET region, which are n-type doped regions, and the lowest at the channel in strong inversion. However, the change in threshold voltage is only attributed to carrier injection from the channel region. Injected charges from the channel region are calculated from the measured threshold voltage shift (ΔV_{TH}) as

$$\Delta Q_{inj} = \Delta V_{TH} \times C_{ox} = qN_T. \tag{3}$$

The oxide thickness for C_{ox} is assumed to be 50 nm for all vendors. Then Q_{inj} divided by electron charge, q, which is $1.6 \times 10^{-19}\ C$ gives us the total number of traps per unit area that have captured electrons (N_T). Threshold voltage shifts, under bias-stress of +30 V, from Figs. 4 (a) and (b), and the number of traps per unit area calculated through (2) and (3) are summarized in Table II. The tunneling process is direct tunneling into traps which occurs at low electric field in the insulator. Band-to-band tunneling followed by trapping in the oxide has not been taken into account since the current level is low at the given gate voltages.

TABLE II. Threshold voltage shifts and NIOTs

Under +30 V	C	D	D'	E'	I
$\Delta V_{TH}(V)$	0.75	0.50	0.25	0.35	0.15
$N_T(\ cm^{-2})$	3.23E11	2.16E11	1.08E11	1.51E11	0.65E11

Using the barrier height (ϕ_B) for Fowler-Nordheim (F-N) tunneling from SiC to the gate oxide, barrier width from the SiC CB to the edge of the oxide (x_{BW}) indicated in Fig. 5 (b) is calculated by

$$x_{BW} = \phi_B/\varepsilon_{ox}. \tag{4}$$

where ϕ_B is 2.8 eV [16], x_{BW} are 67 Å and 45 Å under the gate biases of +20 V and +30 V, respectively.

Assuming a uniform trap distribution, spatially and energetically, tunneling distance to the point where threshold voltage shift saturates can be obtained by a quantum mechanical approach. Lundström and Svensson have shown that the tunneling time constant can be expressed by [17]

$$\tau = \tau_s = \tau_0 e^{2k_B x_T} \tag{5}$$

where $\tau = \tau_s$ is the time constant for tunneling from the SiC CB to traps, i.e. stress time, τ_0 is the time constant, x_T is the tunneling distance and k_B is the wave vector.

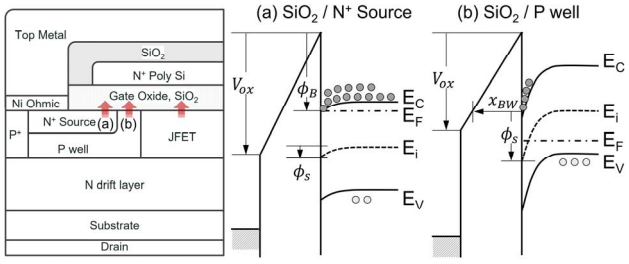

Figure 5. Cross-section of conventional DMOSFET with energy-band diagrams at (a) N^+ source and (b) P-well under a positive gate bias.

τ_0 is given by

$$\tau_0 = \frac{4\pi\hbar}{q\sigma_T k_B \varepsilon}\left(\frac{m_{T0}{}^*}{m_s}\right)^2 \quad (6)$$

where $\hbar$ is Planck constant, σ_T is the capture cross-section, ε is the applied electric field to the oxide, $m_{T0}{}^*$ is the effective mass in oxide for the tunneling electron, and m_s is the electron effective mass in semiconductor [18]-[20]. In this case, a good approximation for σ_T is $10^{-14}cm^2$. The wave vector k_B is given by [17]

$$k_B = \frac{\sqrt{2qm_{T0}{}^*\phi_B}}{\hbar} \quad (7)$$

Then the tunneling distance as a function of the stress time and the electric field is expressed by re-writing (6):

$$x_T = \frac{1}{2k_B}\ln\left(\frac{\tau_s}{\tau_0}\right) \quad (8)$$

Fig. 6 shows the tunneling distance under bias-stress of +20 V calculated with (6), (7), and (8). When the threshold voltage shift saturates, the x_T reaches a maximum where electrons tunnel 39 Å to NIOTs in 72,000 s. Electrons in 1 µs, tunnel to traps 18 Å away from the interface. Thus, in making measurements, there is a significant amount of back-tunneling from NIOTs within a 30 Å distance from the interface. For a stress time increase of one order of magnitude, electrons will penetrate 2 Å further into the oxide. If the bias-stress increases, tunneling distance will increase; however, this effect is limited by the oxide breakdown. This is also an indicator of gate oxide reliability which is demonstrated by Time Dependent Dielectric Breakdown (TDDB) tests [21], [22].

IV. Conclusions

Threshold voltage shifts on commercially available 1.2 kV SiC power MOSFETs have been observed by applying bias-stress to the gate for 5 to 50 hours. Bias-induced threshold voltages shift further as bias-stress is increased. Devices under test, from different manufacturers, differ considerably in the threshold voltage shift. This indicates different near-interface trap distributions in the oxide since the threshold voltage is significantly affected by those traps. Results also indicate some vendors have effectively reduced the NIOTs. A high density of NIOTs may have implications for the lifetime of the gate oxide and could affect the interpretation of TDDB tests.

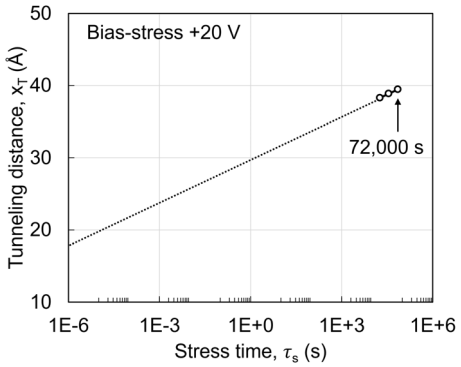

Figure 6. Tunneling distance as a function of stress time at DC bias-stress of +20 V.

Acknowledgment

This research is supported in part by the US Department of Energy (DOE) Vehicle Technologies Office (VTO) under the Electric Drive Train Consortium and the block gift grant from the II-VI Foundation. The authors also gratefully acknowledge the contributions of the Power Electronics Teams at Ford Motor Company's Research and Innovation Center as well as at Sandia National Laboratories

References

[1] J. A. Cooper, Jr. and A. K. Agarwal, "SiC power-switching devices—The second electronics revolution?," *Proc. IEEE*, vol. 90, no. 6, pp. 956-968, 2002.

[2] S. Dimitrijev, "SiC power MOSFETs: The current status and the potential for future development," *2017 IEEE 30th International Conference on Microelectronics (MIEL)*, 2017.

[3] S. Yu, M. Kang, T. Liu, D. Xing, A. Salemi, M. H. White, and A. K. Agarwal, "Bias-induced Threshold Voltage Instability and Interface Trap Density Extraction of 4H-SiC MOSFETs," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, in press.

[4] A. K. Agarwal and S. Haney, "Some critical materials and processing issues in SiC power devices," *J. Electron. Mater.*, vol. 37, pp. 646-654, 2008.

[5] S. Dahr, S. Wang, J. R. Williams, S. T. Pantelides, and L. C. Feldman, "Interface passivation for Silicon Dioxide layers on Silicon Carbide," *MRS Bulletin*, vol. 30, no. 4, pp. 288-292, 2005.

[6] J. Rozen, S. Dahr, M. E. Zvanut, J. R. Williams, and L. C. Feldman, "Density of interface states, electron traps, and hole traps as a function of the nitrogen density in SiO_2 on SiC," *J. Appl.*, vol. 105, p. 124506, 2009.

[7] P. Fiorenza, L. K. Swanson, M. Vivona, F. Giannazzo, C. Bongiorno, A. Frazzetto, and F. Roccaforte, "Comparative study of gate oxide in 4H-SiC lateral MOSFETs subjected to post-deposition-annealing in N_2O and $POCl_3$," *Appl. Phys. A*, vol.115, pp. 333-339, 2014.

[8] D. Okamoto, H. Yano, K. Hirata, T. Hatayama and T. Fuyuki, "Improved Inversion Channel Mobility in 4H-SiC MOSFETs on Si Face Utilizing Phosphorus-Doped Gate Oxide," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 710-712, 2010.

[9] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications. John Wiley & Sons, 2014.

[10] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1835-1840, 2008.

[11] T. Aichingera,G. Rescherb, and G. Pobegenb, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability*, vol. 80, pp. 68-78, 2018.

[12] A. J. Lelis, D. Habersat, R. Green, and N. Goldsman, "Two-way tunneling model of oxide trap charging and discharging in SiC MOSFETs," *Mater. Sci. Forum*, vol. 717-720, pp. 465-468, 2012.

[13] D. K. Schroder, "Negative bias temperature instability: What do we understand?," *Microelectronics Reliability*, vol. 47, pp. 841-852, 2007.

[14] A. Ortiz-Conde, F. J. Garcia-Sanchez, J. Muci, A. T. Barrios, J. J. Liou, and C. S. Ho, "Revisiting MOSFET threshold voltage extraction methods," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 90-104, 2013.

[15] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs,", *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316-323, 2015.

[16] D. J. Lichtenwalner, S. Sabri, E. V. Brunt, B. Hull, S. Ganguly, D. A. Gajewski, S. Allen, and J. W. Palmour, "Gate Oxide Reliability of SiC MOSFETs and Capacitors Fabricated on 150mm Wafers," *Mater. Sci. Forum*, vol. 963, pp. 745-748, 2019.

[17] I. Lundström and C. Svensson, "Tunneling to traps in insulators," *J. Appl.*, vol. 43, pp. 5045-5047, 1972.

[18] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2," *J. Appl.*, vol. 40, pp.278-283, 1969.

[19] N. T. Son, W. M. Chen, O. Kordina, A. O. Konstantinov, B. Monemar, E. Janzén, D. M. Hofman, D. Volm, M. Drechsler, and B. K. Meyer, "Electron effective masses in 4H-SiC," *Appl. Phys. Lett.*, vol. 66, pp. 1074-1076, 1995.

[20] J. Suñé, P. Olivo, and B. Riccó, "Self-consistent solution of the Poisson and Schrödinger equations in accumulated semiconductor-insulator interfaces," *J. Appl.*, vol. 70, pp. 337-345, 1991.

[21] T. Liu, S. Zhu, S. Yu, D. Xing, A. Salemi, M. Kang, K. Booth, M. H. White, and A. K. Agarwal, "Gate Leakage Current and Time-Dependent Dielectric Breakdown Measurements of Commercial 1.2 kV 4H-SiC Power MOSFETs," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, in press.

[22] K. Okada, K. Kurimoto, and M. Suzuki, "Anomalous TDDB Statistics of Gate Dielectrics Caused by Charging-Induced Dynamic Stress Relaxation Under Constant–Voltage Stress," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2268–2274, 2016.