REGULAR PAPER

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Japanese Journal of Applied Physics **61**, 061007 (2022) **REGULAR PAPER**
https://doi.org/**10.35848/1347-4065/ac6409**

Non-isothermal simulation of SiC DMOSFET short circuit capability

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Received December 14, 2021; revised March 15, 2022; accepted April 3, 2022; published online May 24, 2022

The short circuit (SC) capability is a crucial figure of merit for a power switching device in applications such as electrical vehicle traction inverters and chargers. SiC DMOSFETs are inferior to insulated gate bipolar transistors in terms of the SC withstand time. In this work, the SC capability of a SiC DMOSFET is investigated through non-isothermal simulations and measurements. Its sensitivity to process-induced channel length variability has been examined. Its dependence on important device design parameters has been studied, revealing the JFET width as the most sensitive amongst them for optimizing the SC capability. Previously reported SC enhancement techniques that require added fabrication steps were corroborated.

1. Introduction

With superior material properties,[1)] SiC devices are better suited than their Si counterparts to operate in extreme conditions, such as high power[2)] and high temperature. In the case of SiC DMOSFETs, traps at the SiC/SiO_2 interface prove to be the performance limiting factor.[3,4)] Extensive research in this field has been aimed at and has led to reduction in defects at the SiC/SiO_2 interface.[5–9)] There have also been suggestions for novel device designs[10–12)] to improve performance, working around this limitation. Like with all technology areas, as SiC DMOSFET technology matures in terms of satisfactory performance, questions of reliability and failure take on a more central role.[13)] The short circuit (SC) capability addresses a key failure mechanism in these devices, wherein the device experiences very high voltage between the drain to the source terminal when the device is on. The current and the lattice temperature of the device increases tremendously with the voltage stress. To withstand this higher temperature and current is a significant reliability challenge for the device. Left unchecked, it could lead to the device burning out. Among various reasons reported[14–16)] for this, the melting of contacts (aluminum) may be considered the most important factor. The conducting paths created will eventually kill the functionality of the device.

In this work, we investigate the SC capability of the SiC DMOSFET with respect to experimental models. The sensitivity of the SC capability to design parameters has been explored in microscopic detail. Possible process-induced variability has also been studied. SC capability improvement techniques reported in the literature[17–19)] have been simulated in order to investigate their efficacy. This paper attempts to examine a holistic picture of the SC capability and aims to explore and suggest ways to enhance the SC protection time for a SiC DMOSFET. This study may be especially significant in the context of electric vehicles, where insulated gate bipolar transistors (IGBTs) dominate today in part for their superior SC capability.

2. Device structure and simulation setup

A generic 1200 V vertical SiC DMOSFET structure shown in Fig. 1 is simulated in a non-isothermal environment of the TCAD platform to study the SC capability of the device. Thus, we have used the thermodynamic model in addition to the usual drift-diffusion for electrons and holes. The dependence of mobility on the transverse electric field, doping, velocity saturation, and incomplete ionization are included. Recombination models, namely SRH, Auger, and Band to Band are defined for the simulation.[20)] The acceptor type interface trap ($Q_A = 1.5 \times 10^{12}\,cm^{-2}$ at $E_C - E_F = 0.18\,eV$) and oxide fixed charge density $2 \times 10^{11}\,cm^{-2}$ are defined at SiC/SiO_2[21)] for the simulation.

The device is normally off.[22)] The half JFET width (W_{JFET}) is 0.45 μm with doping $8 \times 10^{15}\,cm^{-3}$. An oxide thickness of 58 nm has been used in the simulation. The parameters for bulk and interface mobility, its degradation with temperature[23–25)] and thermal parameters such as thermal conductivity[26)] and specific heat capacity[27)] have been taken from the experimental literature. It is observed that the default model equation for the heat capacity leads to breakdown by thermal generation as the temperature increases. As we have noted above, the device will actually fail at lower temperatures due to the melting of its Al contacts. Therefore, we seek to eliminate this superfluous complication in our quest to improve the SC capability by lowering the current and temperature transients. That is achieved by modifying the temperature dependence of the heat capacity, in particular its cubic coefficient.

$$C_v(JK^{-1}cm^{-3}) = 5.10 \times 10^{-9}T^3 - 1.22 \times 10^{-5}T^2 + 1.29 \times 10^{-2}T - 0.685, \quad (1)$$

where, C_v is the specific heat capacity of SiC.

3. Results and discussion

The result of a representative SC simulation is illustrated in Fig. 2 which is being reinforced by the experimental measurement shown in Sect. 3.4. Here, the device is biased with 5 μs, (20, −10) gate pulse and 800 V drain voltage. As can be seen from Fig. 2(a), the drain current initially increases because of inversion, followed by a decrease due to mobility reduction on account of phonon scattering. The energy density dissipated in the device is calculated by integrating the current density and multiplying it with the drain to source voltage; this is found to be $13\,J\,cm^{-2}$. The device temperature is also shown in the same plot, where the

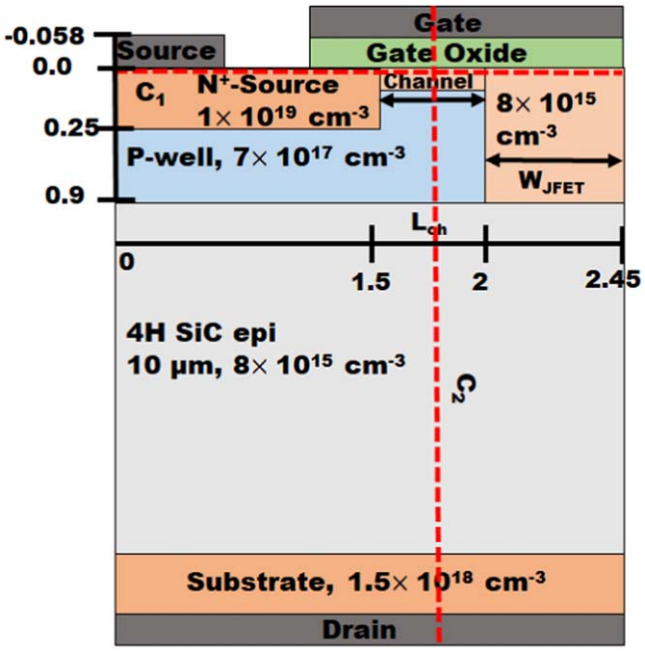

Fig. 1. (Color online) Half-cell SiC DMOSFET structure used in the simulation.

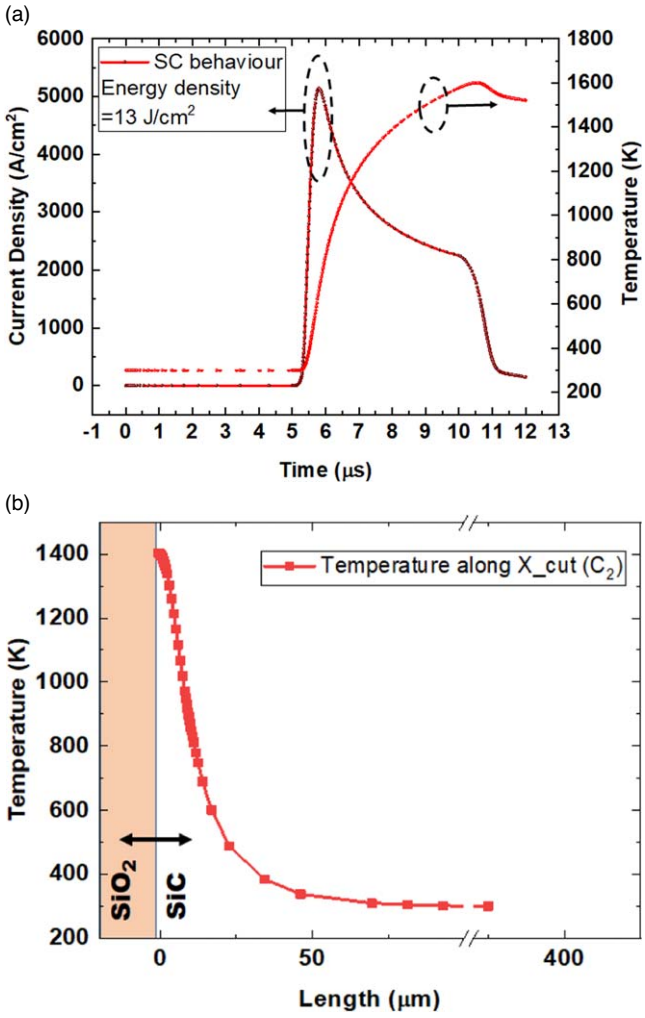

Fig. 2. (Color online) (a) Short circuit simulation of the DMOSFET with 20 V gate pulse with period of 5 μs and $V_{ds} = 800$ V. (b) The temperature profile with a vertical cut line along the channel (C_2: Fig. 1).

peak temperature is around 1600 K.[28] The temperature in the device increases until the gate pulse becomes negative. The temperature profile (at the end of the gate pulse), which gives the position of peak temperature in the device, is shown in Fig. 2(b). The peak is closer to the gate terminal, which is another reason for the inferior SC withstand time (SCWT) for the SiC DMOSFET compared to the IGBTs.[29] Further device engineering would be needed to move the peak of the temperature profile away from the gate contact, which is beyond the scope of this paper.

3.1. Variability study

We examine the sensitivity of the SC capability to channel length variability. We note that this refers to process variability, that is incidental to channel formation. We know that in SiC DMOSFETs, the channel resistance comprises a significant part of the overall resistance of the device. The length of the channel is a significant parameter as it directly controls this resistance.

We consider the variability arising from two possible processes for self-aligned channel formation. The first, illustrated in Fig. 3(a), arises from the dry etch process used to form an oxide spacer, which follows the P-well implant defined by the oxide hard mask. The spacer then acts as a hard mask during the N^+ source region (N^+-source) implant so as to define the channel (additive). The distance between the two P-well in this case is fixed. Thus, channel

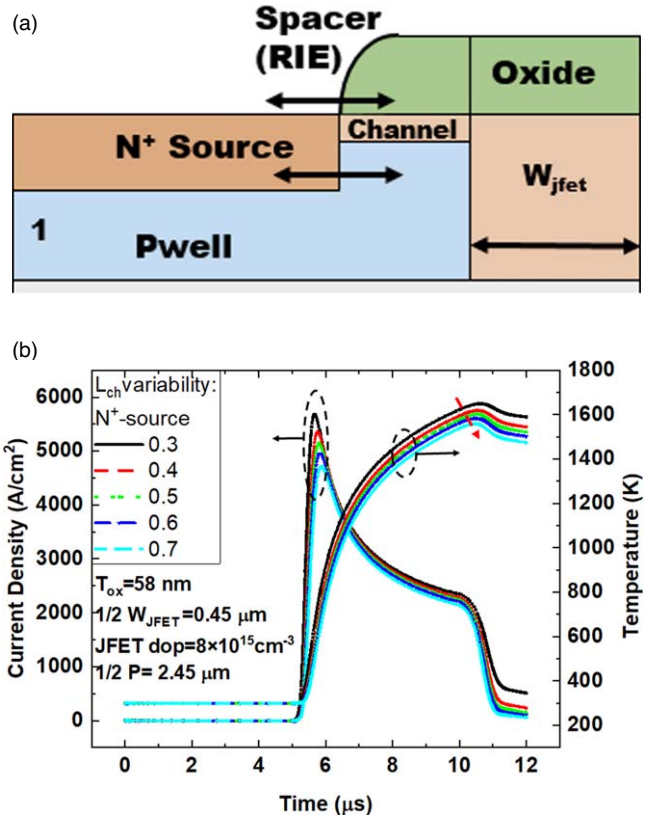

Fig. 3. (Color online) Effect of process-induced channel length (L_{ch}) variability towards the N^+-source side on the short circuit capability. (a) Device schematic for channel length variability: the oxide spacer oxide is deposited conformally and etched anisotropically to provide a hard mask for N^+-source doping. (b) Effect of channel length variability towards N^+-source: "1" on drain current and temperature transients. The fixed parameters of the device for the simulations are mentioned below the legend.

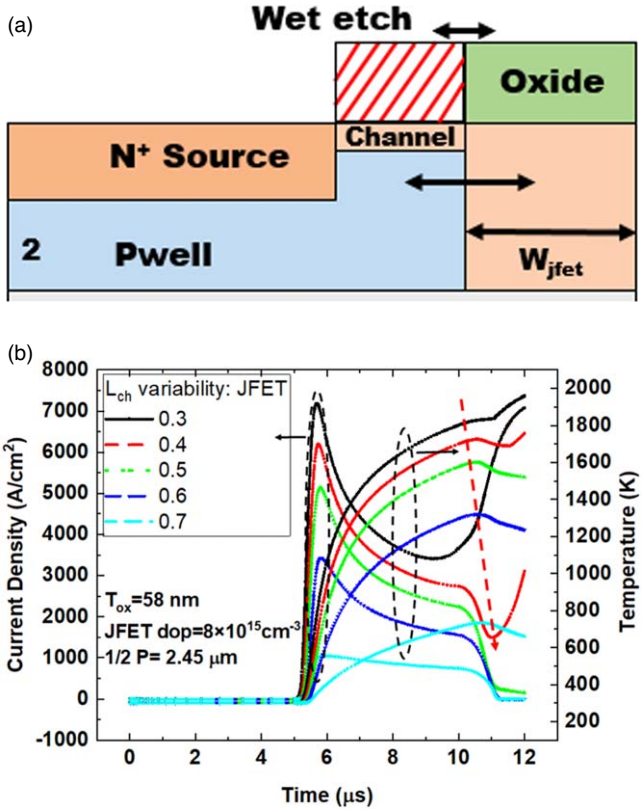

Fig. 4. (Color online) Effect of process-induced channel length (L_{ch}) variability towards the JFET side on short circuit capability. (a) Device schematic for channel formation and length variability: the wet etch moves back the oxide to provide a hard mask for the P-well doping. (b) Effect of channel length variability towards JFET: "2" on drain current and temperature transients. Note that the effect in this case is more pronounced than it was for variability towards N^+-source [Fig. 3(b)]. The fixed parameters of the device for the simulations are mentioned below the legend.

length variability in this case is towards the N^+-source side. The second, illustrated in Fig. 4(a), arises from a wet etch process to move back the oxide hard mask, which is used for the N^+-source implant. The shortened oxide now constitutes a hard mask for the P-well implant, and thereby defines the channel (subtractive). The distance between the two N^+-source implant in this case is fixed. The channel length variability in this case is therefore from the JFET region side. The total cell pitch remains constant in both case. Some degree of variability of the channel length is unavoidable in the device fabrication process, which would induce a variability of channel length from the N^+-source side ("1") or JFET side ("2") as shown in Figs. 3(a) and 4(a), respectively. The effect of these two types of variability on the SC capabilities has been studied, and the simulation results are shown in Figs. 3 and 4. We consider both a decrease and an increase of channel length from each side. The pitch of the device is kept fixed for the purposes of this study.

Figure 3(b) shows variability of type "1", while Fig. 4(b) shows variability of type "2". The effect of these variability types on the SC capability is different, and depends on the effective channel length, which here ranges from 0.3 to 0.7 μm. For type "1", the effective channel length increases and decreases with N^+-source, and most of the other device parameters are not affected as shown in Table I. For type "2", the varied channel length is effectively changing the JFET dimensions. The combined effect is more pronounced which can be observed from the resulting SC curves and also discussed individually in the next section (Sect. 3.2). The SC capability of the device worsens with a decrease in channel length, since that leads to higher currents. The results indicate for stable SC performance, the additive method of fabrication must be adapted for the SiC-based DMOSFET.

3.2. Sensitivity study

The on-resistance of the device is significantly determined by the doping, width of the JFET region, and the channel length. We next take up the dependence of the SC capability on key device parameters, which can be varied by design without additional lithography steps, in order to optimize the SC. The summary is tabulated in the Table II. The results are shown in Figs. 5 and 6. First and second, the results of channel length (0.3–0.7 μm) and oxide thickness (40–80 nm) variation are shown in Figs. 5(a) and 5(b), respectively. The observed variation produced the expected trend of SC capability as determined by the on-resistance, which is explained previously with the channel length variability. The oxide thickness will control the capacitance, which will vary the output current, and hence the SC performance. Third, the JFET doping is varied from 4×10^{15} cm^{-3} to 3×10^{16} cm^{-3} and the results may be seen in Fig. 6(a). With increase in JFET doping, the resistance decreases; and therefore, the current increases as expected. Fourth, we varied the JFET width, W_{JFET}, from 0.35 to 0.55 μm; the effect on SC capability is striking, as shown in Fig. 6(b). This was further investigated, and will be explained in the following paragraph. Note that the channel length and JFET width variation are accompanied by variation in the pitch as well. We recognize that the preceding variations (increased channel length and gate oxide thickness) to the device design intended to improve the SC capability can end up increasing the on-resistance, which would be detrimental to the overall device performance. This may be addressed, in the case of the most sensitive design parameter, by coupling a reduction in the JFET width with a compensating increase in the doping.

Before proceeding further, we seek to draw out the physical reason behind the strong sensitivity of the SC capability to JFET width variation. We note that this behavior has been observed earlier.[23] We analyze this by considering electrostatics potential plots on a horizontal cut line along the channel of the device (C_1: Fig. 1), as shown in Fig. 7. It can be observed that the JFET width variation has a far larger effect on the potential as well, compared to variation in channel length or oxide thickness. Now, let us consider in finer detail the left (or right) half of the potential profiles in Fig. 7(c). For a half JFET width (1/2 W_{JFET}) of 0.55 μm, it looks exactly like the source-drain potential profile for a planar transistor. However, as the 1/2 W_{JFET} decreases to 0.45 μm and 0.35 μm, the source contacts from both sides of the JFET region, acting in tandem, pull up (push down) the electron energy (electrostatic potential) therein. Thus, it is in some sense a two-dimensional inverse of the drain-induced barrier lowering or punchthrough effects; where the source contacts on the left and right, as they get close, tend to pull up the electron energy floor in the JFET region that is sought to be pulled down by the drain contact at the bottom.

Further, we investigate the design approach to gain SCWT without sacrificing the specific on-resistance ($R_{on,sp}$) of the

Table I. The vertical interfaces of the channel are affected by the proces-induced variability as discussed in Sect. 3.1. The change in the left interface will affect the length of N^+-source and channel. Similarly, the JFET and channel length will be affected for the right interface. As this is process-induced, the pitch of the device in both cases will remain constant. The summary of the variability study is presented in the table below, with the energy density obtained for each variability.

	L_{ch} (μm)	T_{OX} (nm)	1/2 W_{JFET} (μm)	JFET Doping (cm^{-3})	N^+-Source length (μm)	N^+-Source doping (cm^{-3})	Energy density (J/cm^2)	P (μm)
Ref	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
Channel length variability towards N^+-source region	0.7	58	0.45	$8\times10^{+15}$	1.3	$1\times10^{+19}$	12.1	2.45
	0.6	58	0.45	$8\times10^{+15}$	1.4	$1\times10^{+19}$	12.63	2.45
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.4	58	0.45	$8\times10^{+15}$	1.6	$1\times10^{+19}$	13.46	2.45
	0.3	58	0.45	$8\times10^{+15}$	1.7	$1\times10^{+19}$	14.37	2.45
Channel length variability towards JFET region	0.7	58	0.25	$8\times10^{+15}$	1.5	$1\times10^{+19}$	3.7	2.45
	0.6	58	0.35	$8\times10^{+15}$	1.5	$1\times10^{+19}$	8.9	2.45
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.4	58	0.55	$8\times10^{+15}$	1.5	$1\times10^{+19}$	17.22	2.45
	0.3	58	0.65	$8\times10^{+15}$	1.5	$1\times10^{+19}$	25.17	2.45

Table II. The summary of the sensitivity study for four design parameters is tabulated below. Each parameter is varied discreetly without affecting the others. The change in pitch follows the change in JFET and channel length variations. With the T_{ox} and JFET doping variations, the pitch remains fixed. The result indicates the variation of the JFET gap is the most sensitive one. The energy density obtained for each variation is tabulated.

	L_{ch} (μm)	T_{OX} (nm)	1/2 W_{JFET} (μm)	JFET Doping (cm^{-3})	N^+-Source length (μm)	N^+-Source doping (cm^{-3})	Energy density (J/cm^2)	P (μm)
Ref	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
Channel length variation	0.7	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	11.62	2.65
	0.6	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	11.76	2.55
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.4	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13.27	2.35
	0.3	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	15.53	2.25
Oxide thickness variation	0.5	40	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	14.27	2.45
	0.5	50	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13.4	2.45
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.5	70	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	12.35	2.45
	0.5	80	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	11.87	2.45
JFET doping variation	0.5	58	0.45	$4\times10^{+15}$	1.5	$1\times10^{+19}$	12.66	2.45
	0.5	58	0.45	$6\times10^{+15}$	1.5	$1\times10^{+19}$	12.83	2.45
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.5	58	0.45	$1\times10^{+16}$	1.5	$1\times10^{+19}$	13.2	2.45
	0.5	58	0.45	$3\times10^{+16}$	1.5	$1\times10^{+19}$	15.3	2.45
JFET gap (1/2 W_{JFET}) variation	0.5	58	0.55	$8\times10^{+15}$	1.5	$1\times10^{+19}$	16	2.55
	0.5	58	0.5	$8\times10^{+15}$	1.5	$1\times10^{+19}$	14.45	2.5
	0.5	58	0.45	$8\times10^{+15}$	1.5	$1\times10^{+19}$	13	2.45
	0.5	58	0.4	$8\times10^{+15}$	1.5	$1\times10^{+19}$	10.63	2.4
	0.5	58	0.35	$8\times10^{+15}$	1.5	$1\times10^{+19}$	9	2.35

device. So we decrease the JFET gap with an increase in JFET doping and simulate the device. The calculated the SCWT from non-isothermal simulation [not shown here] and $R_{on,sp}$ from output characteristic simulation [not shown here] ($V_{gs} = 20$ V, $T = 300$ K) for two 1/2 W_{JFET} (0.35 μm, 0.45 μm) with a range of JFET doping (8×10^{15} cm^{-3} to 5×10^{16} cm^{-3}). The result is presented in Fig. 8. The on-resistance of the device decreases with the increase in JFET doping and increase in the JFET gap. Lower resistance improves the drain current, so the temperature increases during the SC event. The resultant SCWT therefore decreases. For the calculation of SCWT, we consider the time at which the device temperature reaches the melting point of source metal (aluminum: 934 K). 1 μs time is added with that to emulate the time required for the melted Al to create shorts in the device.

3.3. Improvement techniques

Finally, we examine a couple of methods that have been proposed in the literature to improve the SC capability a shielded MOSFET design[17,18] as shown in Fig. 9(a) and increased source resistance through reduced doping[19] as shown in Fig. 9(b). These have been demonstrated in an isothermal simulation environment. Apart from that, these methods will require few additional fabrication steps (masking and lithography). More structural and working details can be found in the cited references. These modified structures are simulated, and their SC performance is shown in Fig. 10. The summary is tabulated in Table III. For the first technique, viz. shielding, a highly doped p^+ (doping variation: 1×10^{18} cm^{-3} to 1×10^{19} cm^{-3}) region with thickness 0.2 μm below P-well is introduced [Fig. 9(a)]; the results are shown in Fig. 10(a). We see that shielding is more effective in reducing the drain current with higher doping. The second improvement technique, viz. a lower doped source region, is introduced for 1 μm out of 1.5 μm of total N^+-source length [Fig. 9(b)]. This low doped region acts as an added external resistance, and the drain current decreases. The effect of the

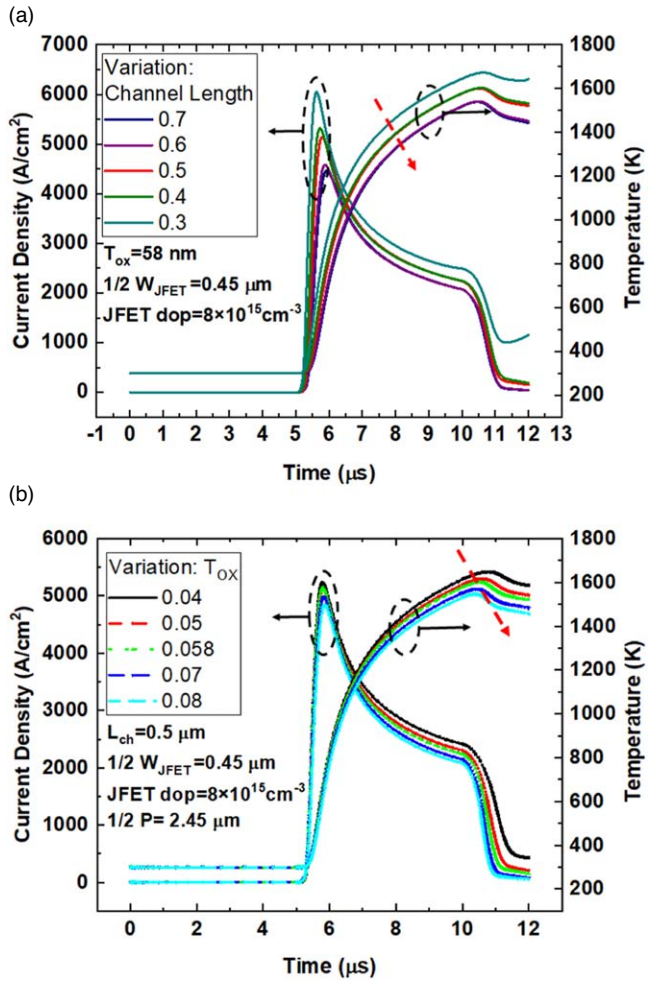

Fig. 5. (Color online) Sensitivity analysis of various parameters of DMOSFET on short circuit capability. (a) Channel length variation. (b) Oxide thickness variation. The fixed parameters of the device for the simulations are mentioned below the legend.

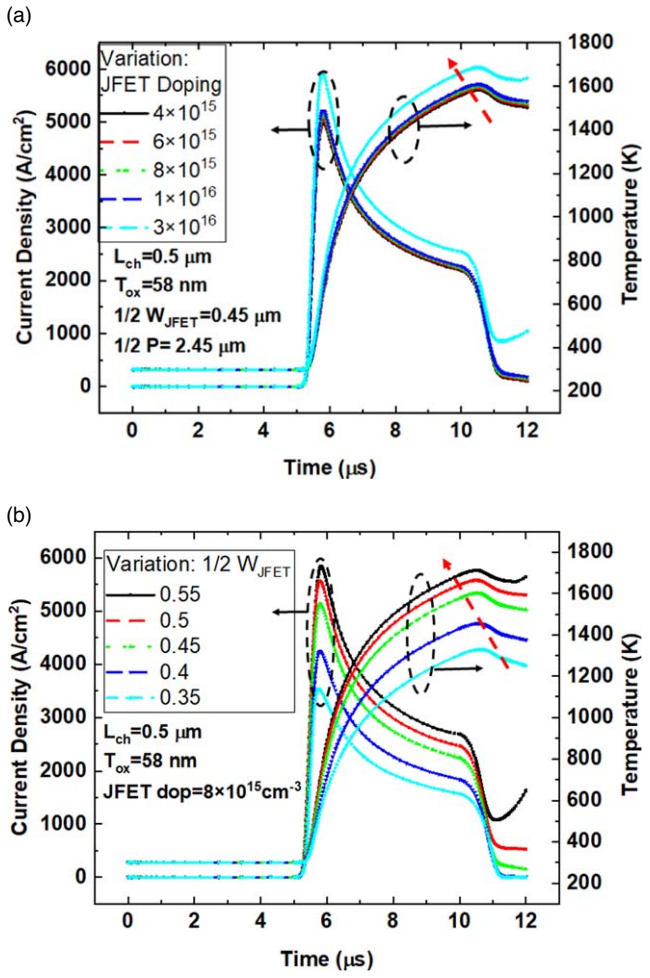

Fig. 6. (Color online) Sensitivity analysis of various parameters of DMOSFET on short circuit capability. (a) JFET doping variation. (b) JFET width variation. The variation of the JFET width is found to be the most effective parameter for SC capability. The fixed parameters of the device for the simulations are mentioned below the legend.

doping variation from 5×10^{17} cm^{-3} to 1×10^{19} cm^{-3} is shown in Fig. 10(b). The on-resistance (R_{on}) of the device is not affected by the P$^+$-shielding method where as the increased source resistance will affect the R_{on}.

3.4. Experimental results

1200 V DMOSFET devices with planar gate were procured from two vendors (designated as C and E) to test their SCWT.[30,31] Twenty-five devices from each vendor were tested for SC, and the results are presented in Fig. 11. The devices were subjected to a V_{ds} of 800 V and increasing pulse width of $V_g = (20, 0)$ V pulse was applied at the gate terminal until the device blew up due to thermal dissipation inside the package. Figure 11(a) shows the measured drain current of one selected device from each of the vendors. The higher drain current peak is obtained for vendor E as the device has lower R_{on} compared to vendor C. Figure 11(b) shows the SCWT of all the devices tested, in ascending order of SCWT, for both the vendors. The difference of SCWT is around 0.5 μs for the two vendors, and 1 μs and 0.4 μs variation is observed within 25 devices from vendor C and vendor E, respectively. The variation of the SCWT for the different devices within and between the vendors can be related to the variability and sensitivity study presented in the Sects. 3.1

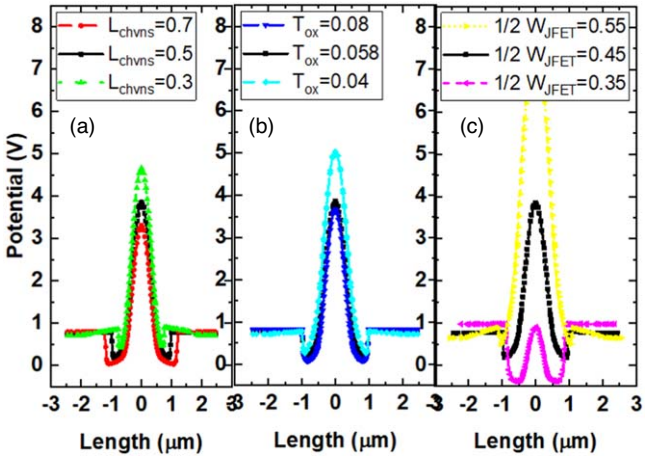

Fig. 7. (Color online) Potential in the device along the cut line (C_1) shown in Fig. 1. The potential for three variations are shown in this plot, such as L_{ch} variability (type "1") (a) [fixed parameters: $T_{OX} = 58$ nm, 1/2 $W_{JFET} = 0.45$ μm, JFET doping $= 8 \times 10^{15}$ cm^{-3}], the oxide thickness variation (b) [fixed parameters: $L_{ch} = 0.5$ μm, 1/2 $W_{JFET} = 0.45$ μm, JFET doping $= 8 \times 10^{15}$ cm^{-3}, 1/2 $P = 2.45$ μm], the JFET width variation (c) [fixed parameters: $L_{ch} = 0.5$ μm, $T_{OX} = 58$ nm, JFET doping $= 8 \times 10^{15}$ cm^{-3}].

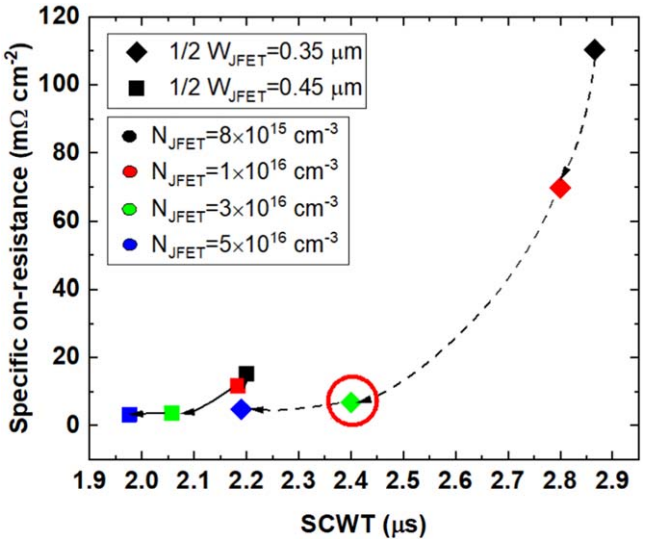

Fig. 8. (Color online) The trade-off between the SCWT and specific on-resistance for two 1/2 W_{JFET} at different JFET doping. With the increase in JFET doping, both SCWT and $R_{on,sp}$ decreases. The proposed design with lower $R_{on,sp}$, and higher SCWT is having 3×10^{16} cm^{-3} doping with 1/2 W_{JFET} of 0.35 μm (marked with a circle). The lines are meant to guide the eyes.

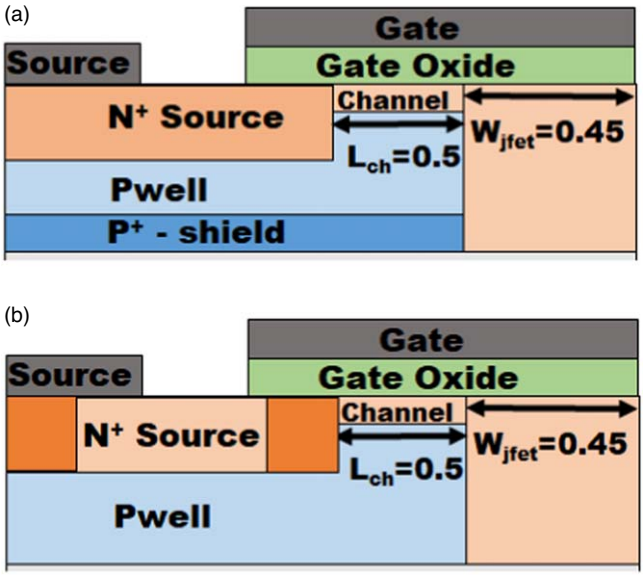

Fig. 9. (Color online) Short circuit capability with reported enhancement techniques.[18,19] (a) P^+ shield below p-base is added, and the doping is varied (b) source resistance is increased by adding low doped region, and the doping is varied.

and 3.2 respectively. The process-induced variability is the cause for the change of SCWT for the devices from a given vendor. The device design of vendor C is more robust when subject to SC conditions.

4. Conclusion

In this work, we explored aspects of the SC capability of the SiC DMOSFET using non-isothermal simulations and measurements. Its sensitivity to process-induced channel length

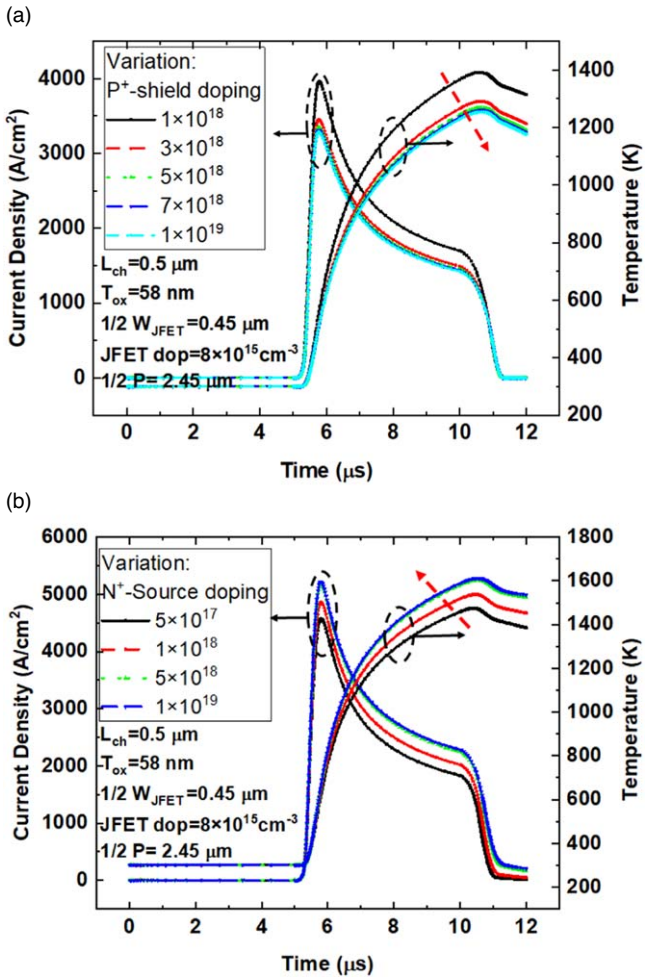

Fig. 10. (Color online) Short circuit capability with reported enhancement techniques.[18,19] (a) SC simulation results for the shielded MOS as shown in Fig. 9(a). (b) SC simulation results with N^+-source resistance variation as shown in Fig. 9(b). The fixed parameters of the device for the simulations are mentioned below the legend.

variability is investigated, and is found to be less pronounced for the variability towards N^+-source, indicating the adaptation of the additive method of fabrication of the power device for stable SC performance. Expectedly, the SC capability degrades with decreasing channel length. These variability is the cause of the obtained SCWT of the devices from a single vendor to diverge. Analysis of the dependence of the SC capability on a set of key device design parameters revealed that the JFET width variation could be the most effective knob in controlling the SC capability. Lastly, non-isothermal simulations of previously proposed device structures modified to enhance the SC capability, confirm notable improvement, which explains the improvement in SCWT for a vendor A. Thus, reduced width of the JFET region, with a compensating increase in the doping, and incorporating P^+-shield, can effectively improve the SC performance of the DMOSFET without an R_{on} trade-off. Lastly, non-isothermal simulations of previously proposed device structures modified to enhance the SC capability, confirm notable improvement.

Table III. The design variation of the shielded MOSFET and the source resistance method of improving the SC behaviour of the device is tabulated with the calculated energy density of each case. The cases of improvement techniques are individually designed, and the doping variations for them are independent of each other.

	L_{ch} (μm)	T_{OX} (nm)	1/2 W_{JFET} (μm)	JFET Doping (cm^{-3})	P^+ shield doping (cm^{-3})	N^+-Source length (μm)	N^+-Source doping (cm^{-3})	Energy density (J/cm^2)	P (μm)
Ref	0.5	58	0.45	$8\times10^{+15}$	-	1.5	$1\times10^{+19}$	13	2.45
P^+-shield doping variation	0.5	58	0.45	$8\times10^{+15}$	$1\times10^{+18}$	1.5	$1\times10^{+19}$	9.9	2.45
	0.5	58	0.45	$8\times10^{+15}$	$3\times10^{+18}$	1.5	$1\times10^{+19}$	8.75	2.45
	0.5	58	0.45	$8\times10^{+15}$	$5\times10^{+18}$	1.5	$1\times10^{+19}$	8.52	2.45
	0.5	58	0.45	$8\times10^{+15}$	$7\times10^{+18}$	1.5	$1\times10^{+19}$	8.43	2.45
	0.5	58	0.45	$8\times10^{+15}$	$1\times10^{+19}$	1.5	$1\times10^{+19}$	8.36	2.45
N^+-source doping variation	0.5	58	0.45	$8\times10^{+15}$	-	1.5	$5\times10^{+17}$	10.8	2.45
	0.5	58	0.45	$8\times10^{+15}$	-	1.5	$1\times10^{+18}$	11.8	2.45
	0.5	58	0.45	$8\times10^{+15}$	-	1.5	$5\times10^{+18}$	13.1	2.45
	0.5	58	0.45	$8\times10^{+15}$	-	1.5	$1\times10^{+19}$	13.3	2.45

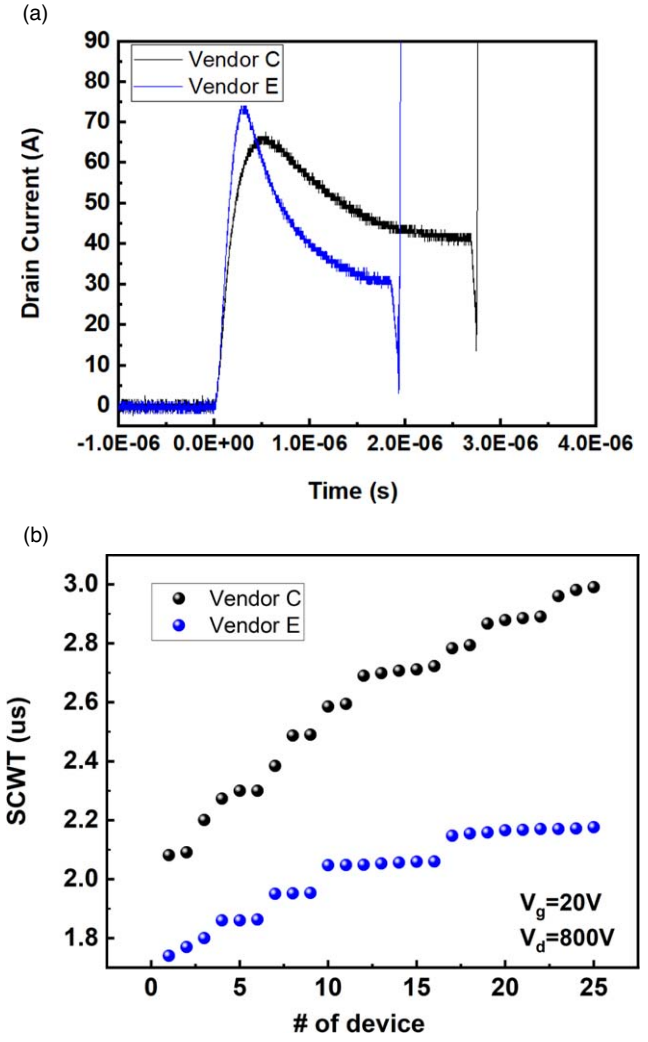

Fig. 11. (Color online) SCWT comparison of devices from two vendors. (a) Measured SC characteristic of a MOSFET from each vendors. (b) The SCWT arranged in ascending order for the MOSFETs from two vendors.

Acknowledgments

Suvendu Nayak, Swaroop Ganguly, and Anant K. Agarwal acknowledge support from the IIT Bombay-Ohio State University Frontier Center.

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