2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA) | 978-1-6654-8900-3/22/$31.00 ©2022 IEEE | DOI: 10.1109/WiPDA56483.2022.9955255

# A Comparison of Ion Implantation at Room Temperature and Heated Ion Implantation on the Body Diode Degradation of Commercial 3.3 kV 4H-SiC Power MOSFETs

Jiashu Qian[1], Tianshi Liu[1], Jake Soto[2], Mowafak M. Al-Jassim[3], Robert Stahlbush[4], Nadeemullah Mahadik[4], Limeng Shi[1], Michael Jin[1], and Anant K. Agarwal[1]
[1]Dept. of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210, USA
[2]Microchip Technology Inc., Bend, OR 97702, USA
[3]National Renewable Energy Laboratory (NREL), Golden, CO 80401, USA
[4]Naval Research Laboratory (NRL), Washington, DC 20375, USA

***Abstract* — It has been demonstrated that basal plane dislocations (BPDs)-induced stacking faults (SFs) cause body diode degradation in commercial 4H-SiC power MOSFETs, especially with higher voltage ratings. BPDs originate from 4H-SiC boule, epi growth, and ion implantation. Considering the lower cost of ion implantation at room temperature (RT), this work investigates the potential of RT ion implantation replacing heated (HT) ion implantation by comparing the influence of both ion implantations on the body diode degradation of commercial 3.3 kV 4H-SiC power MOSFETs. We demonstrate with long-term (up to 1000 hours) forward current stress that RT implantation can keep the body diode degradation of 3.3 kV 4H-SiC power MOSFETs within the specification limits compared with HT implantation.**

***Keywords—4H-SiC, MOSFET, body diode degradation, basal plane dislocation (BPD), ion implantation***

## I. INTRODUCTION

Basal plane dislocations (BPDs) can turn into stacking faults (SFs) in the drift layer of 4H-SiC power MOSFETs and keep expanding by absorbing the activation energy from the recombination of electron-hole pairs [1]. With the activated SFs, the carrier lifetime and mobility in the drift layer decrease, affecting the stable operation of the body diode. To reduce the density of BPDs, a low-dose high temperature Al implantation has been proved to be effective [2]. Besides, employing a recombination-enhanced buffer layer can suppress the expansion of BPDs-induced SFs [3]. Also, a molten KOH etching process before the conventional epitaxial growth is developed to enhance the conversion of BPDs to threading edge dislocations (TEDs) by creating BPD etch pits for low BPD density epilayers [4, 5]. However, K. Konishi., et al. have demonstrated that SFs originating from BPDs converted into TEDs within the buffer layer still expand under high current stress [6]. With these improvements in the material, it is not expected to find significant body diode degradation for low-voltage 4H-SiC power MOSFETs (600-1200 V). However, it is still a challenge in high-voltage 4H-SiC power MOSFETs (≥ 6.5 kV) because the longer growth time of the thicker drift layer (≥ 60 μm) significantly enhances BPDs formation and the spatial size of BPDs-induced SFs [7, 8]. Current process can already grow an epitaxial thickness of up to 30 μm from a 4H-SiC substrate with a negligible density of BPDs (0.5 BPDs on average per wafer in the substrate) for the fabrication of 3.3 kV 4H-SiC power MOSFETs [8]. To further minimize the density of BPDs in the drift layer, heated ion implantation (HT implantation) is employed to reduce generation of new BPDs in industry. Considering the costly heated ion-implantation systems and limited throughput, the main objective of this study is to investigate the possibility of ion implantation at room temperature (RT implantation) replacing HT implantation in the fabrication of 3.3 kV 4H-SiC power MOSFETs.

| | RT Implanted Devices | | HT Implanted Devices | |
|---|---|---|---|---|
| | Avg. | Std. | Avg. | Std. |
| $V_F$ (V) | -3.802 | 0.040 | -3.816 | 0.044 |
| $V_{th}$ (V) | 5.954 | 0.103 | 5.179 | 0.041 |
| $R_{ON}$ (Ω) | 0.071 | 0.001 | 0.066 | 0.001 |

Table. I Pre-test results of 3.3 kV 4H-SiC power MOSFETs under test. $V_F$ is extracted at $I_{DS}$ = -20 A under the 3rd quadrant operation. $R_{ON}$ is extracted at $V_{GS}$ = 20 V, $V_{DS}$ = 0.5 V. $V_{th}$ is extracted with the linear extrapolation method at $V_{DS}$ = 0.1 V.

## II. EXPERIMENTS

### A. *Device Under Test (DUT)*

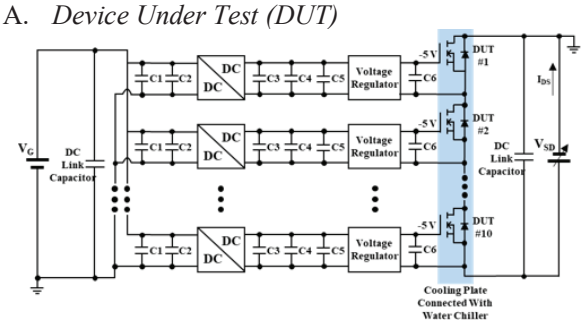


Fig. 1 Schematic of the body diode test setup for ten 3.3 kV 4H-SiC MOSFETs in series.

The 127 DUTs are provided by Microchip Technology Incorporated (MCHP), which are

engineering prototypes of their commercial 3.3 kV 4H-SiC MOSFETs (MSC080SMA330B).

Among these devices, 61 are RT implanted devices and 66 are HT implanted devices. The HT implantation is conducted at 500 °C. Both types of devices are from wafers of the same fab lot. All devices are either all implanted at RT, or all implanted at HT, using equivalent doses and energy. The specific doses and energy are MCHP proprietary information. The active area of the die for both types of devices is 14.3 $mm^2$.

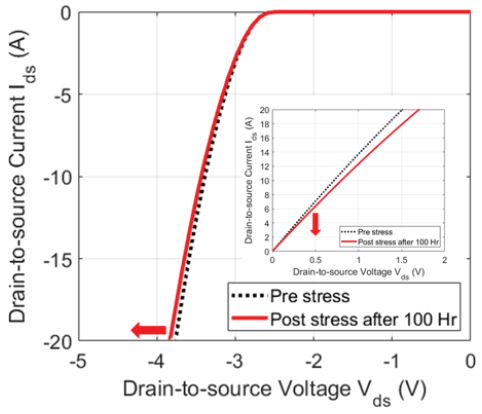


Fig. 2 The criterion (≥ 2% shift for $V_F$ and ≥ 10% shift for $R_{ON}$) for degradation is reflected in the 1st quadrant $I_{DS}$-$V_{DS}$ output characteristics ($V_{GS}$ = -5 V) and 3rd quadrant $I_D$-$V_D$ characteristics ($V_{GS}$ = 20 V).

## B. *Body Diode Stress Test*

To analyze the influence of the body diode degradation on the performance of devices under test, the 3rd quadrant $I_D$-$V_D$ characteristics, the 1st quadrant $I_D$-$V_D$ output characteristics, the 1st quadrant $I_D$-$V_G$ transfer characteristics, and the 1st quadrant forward blocking $I_D$-$V_D$ characteristics are measured by using a Keysight B1506A power device analyzer before and after the stress. Table I shows the pre-stress measurement results of the 61 RT implanted devices and 66 HT implanted devices. Both types of devices have similar average on-state resistance ($R_{ON}$) and average forward voltage drop ($V_F$) of the body diode with equivalent doses and energy for all the implants. Only the average threshold voltage ($V_{th}$) of the RT implanted devices is slightly higher than that of the HT implanted devices. This can be explained by the higher P-type doping concentration within the depth of the p-well in RT implanted devices than that in HT implanted devices [9]. 10 DUTs are connected in series as shown in Fig. 1 to conduct a constant 10 A DC (the stress current density is ~70 $A/cm^2$) through the forward-biased body diodes. Isolated DC-DC converters and voltage regulators help maintain stable gate-source voltages for all devices in series. The gate-source voltages in this study are set to -5 V to make sure the MOS channels of all the devices are pinched-off. The body diodes of all the devices in series are stressed for 100 hours, followed by a 10-min cool-down to room temperature. Then, the electrical measurements mentioned above are performed on each device for comparison with the pre-stress data. This process is repeated every 100 hours until the total stress time of 1000 h is achieved. During the stress, the metal sides of the DUTs' TO-247 packages are fixed on a heat sink with an industrial-grade water chiller connected to dissipate the generated heat and maintain the case temperature at a typical operating level.

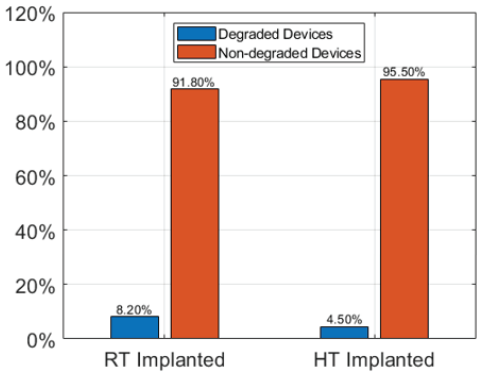


Fig. 3 Degraded vs. non-degraded device ratio of RT and HT implanted devices after 100-hr body diode stress.

# III. RESULTS AND DISCUSSION

## A. *100-hr Body Diode Stress Test*

After 100-hr stress, the body-diode-degraded parts are counted for both types of devices. The criterion of body diode degradation in this study is defined as ≥ 2% shift in $V_F$ and ≥ 10% shift in $R_{ON}$ as shown in Fig. 2. The shift percentage is calculated by the ratio of the shifted value and the pre-stress value. Based on this criterion, all 127 DUTs are binned into two parts (degraded devices vs. non-degraded devices). Fig. 3 illustrates that after 100-hr stress there is no significant difference between RT implanted devices and HT implanted devices on the body diode degradation with a similar sample size. The cumulative frequency plots in Fig. 4 for both RT implanted and HT implanted devices on the $V_F$ shift and the $R_{ON}$ shift give the information that most of both RT implanted and HT implanted devices have the $V_F$ shift and the $R_{ON}$ shift concentrated in 0-0.9% and 0-9% after 100-hr stress, which do not meet the criterion of a 'body-diode-degraded device'. However, RT implanted devices can reach a maximum $V_F$ shift and $R_{ON}$ shift in the range of 1.8%-2.1% and 18%-21%, a little larger than 1.2%-1.5% and 12%-15% of HT implanted devices. There is reason to believe that the RT implantation has the potential to replace the HT implantation in the fabrication of 3.3 kV 4H-SiC MOSFETs based on 100-hr test.

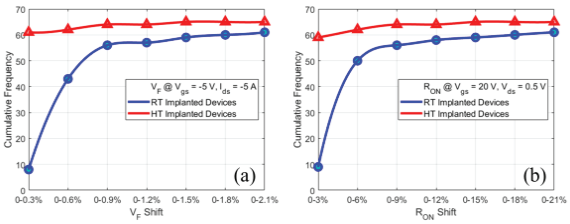


Fig. 4 The cumulative frequency plots for (a) the $V_F$ shift; (b) the $R_{ON}$ shift; of 61 RT implanted devices and 66 HT implanted devices after 100-hr stress. The Y-axis is the cumulative number of devices.

## B. *1000-hr Body Diode Stress Test*

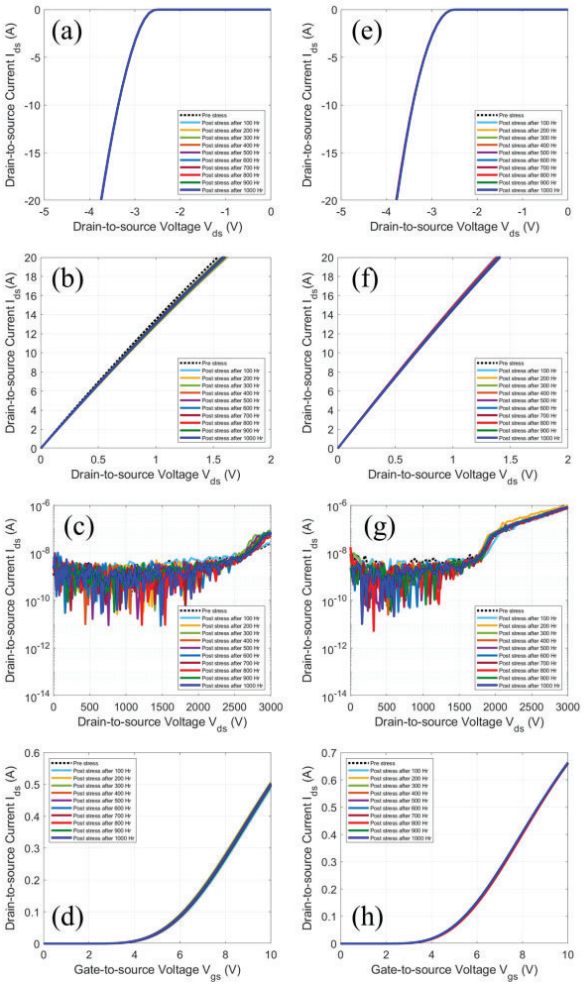


Fig. 5. The 3rd quadrant $I_{DS}$-$V_{DS}$ characteristics ($V_{GS}$ = -5 V) of the least degraded (a) RT; (e) HT; implanted device. The 1st quadrant $I_{DS}$-$V_{DS}$ output characteristics ($V_{GS}$ = 20 V) of the least degraded (b) RT; (f) HT; implanted device. The 1st quadrant forward blocking $I_{DS}$-$V_{DS}$ characteristics ($V_{GS}$ = 0 V) of the least degraded (c) RT; (g) HT; implanted device. The 1st quadrant $I_{DS}$-$V_{GS}$ characteristics ($V_{DS}$ = 0.1 V) of the least degraded (d) RT; (h) HT; implanted device. The stress hours are 1000h.

To further investigate, 20 DUTs each from both types of devices after 100-hr stress are selected for extra 900-hr stress in order to approach the practical lifetime requirement for the body diode of the commercial 4H-SiC power MOSFETs.

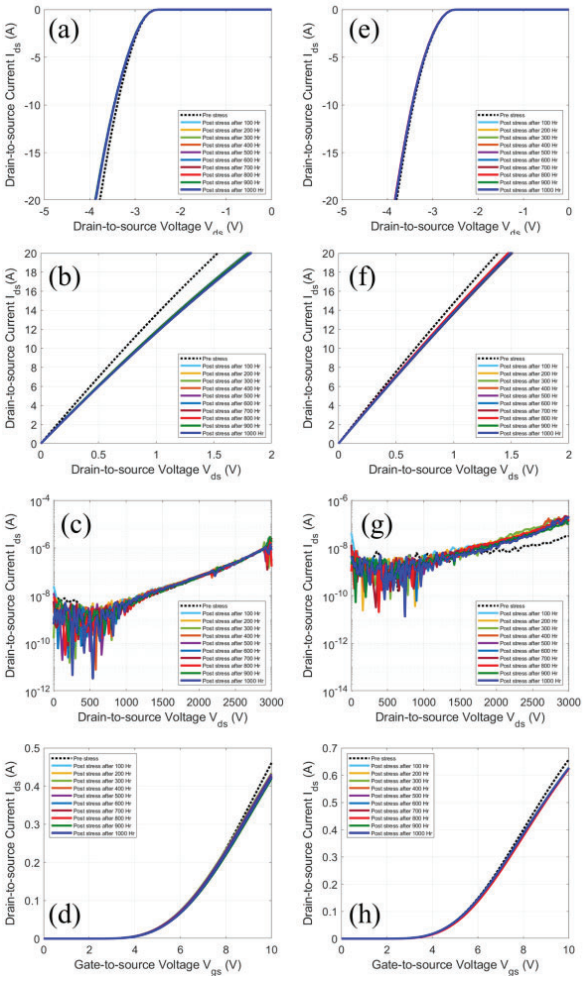


Fig. 6. The 3rd quadrant $I_{DS}$-$V_{DS}$ characteristics ($V_{GS}$ = -5 V) of the most degraded (a) RT; (e) HT; implanted device. The 1st quadrant $I_{DS}$-$V_{DS}$ output characteristics ($V_{GS}$ = 20 V) of the most degraded (b) RT; (f) HT; implanted device. The 1st quadrant forward blocking $I_{DS}$-$V_{DS}$ characteristics ($V_{GS}$ = 0 V) of the most degraded (c) RT; (g) HT; implanted device. The 1st quadrant $I_{DS}$-$V_{GS}$ characteristics ($V_{DS}$ = 0.1 V) of the most degraded (d) RT; (h) HT; implanted device. The stress hours are 1000h.

Fig. 5 shows the degradation evolution with 1000 hours of the least degraded parts for both RT implanted and HT implanted devices. The SMUs of the power device analyzer used in this study have the measurement limitations for the current and voltage of 20 A and 3 kV, respectively. Thus, the 3rd quadrant $I_{DS}$-$V_{DS}$ characteristics, the 1st quadrant $I_{DS}$-$V_{DS}$ output characteristics at $V_{GS}$ = 20 V, and the 1st quadrant forward blocking $I_{DS}$-$V_{DS}$ characteristics can be only observed within the above limits. Almost no visible degradation can be observed in the HT implanted device. Only slight and acceptable degradations can be observed in the output characteristics and the forward

blocking leakage current of the RT implanted device after 1000-hr stress. Most of the DUTs show a similar degradation level to the least degraded parts, regardless of implantations.

Fig. 6 shows the degradation evolution with 1000 hours of the most degraded parts for both RT implanted and HT implanted devices. Although the $V_{th}$ of both RT implanted and HT implanted devices shows a slight variation after 1000-hr stress, the influence on the degradation is negligible. In this case, the degradation reflected on the $V_F$ and $R_{ON}$ of the HT implanted device is still acceptable, however, it can be considered as a 'degraded' part for the RT implanted device. Nevertheless, few RT implanted devices can reach the 'degraded' level, which can be considered an allowable industrial spread. It is worth noting that the HT implanted device has significant blocking leakage current degradation, but the RT implanted device does not, even the RT implanted device is a 'degraded' part. It could be due to the fact that breakdown in the HT implanted device happens in the active area caused by the activated SFs, and breakdown in the RT implanted device occurs in the edge termination region where no SFs form [10].

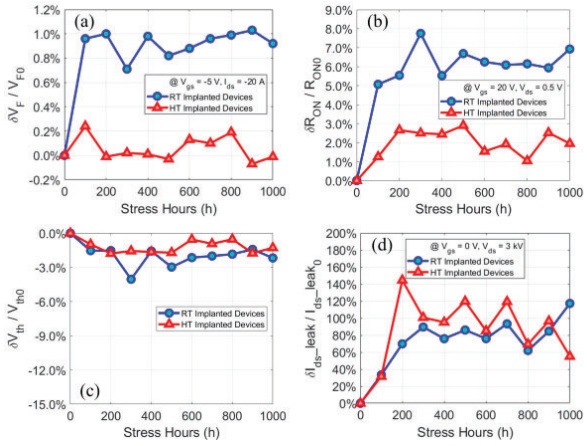


Fig. 7. Comparison between RT and HT implanted devices in terms of the influence of the 1000-hr body diode stress on (a) $V_F$ degradation. (b) $R_{ON}$ degradation. (c) $V_{th}$ degradation. (d) Degradation of the forward blocking leakage current.

The average degradation level of both the 20 RT implanted devices and the 20 HT implanted devices is reflected by the shift percentages in Fig. 7. Although the $V_F$ and $R_{ON}$ degradations of the RT implanted devices in Fig. 7 (a) and Fig. 7 (b) are slightly higher than the HT implanted devices, the degradations are still within an acceptable range based on the criterion above. Fig. 7 (c) shows that the $V_{th}$ shift induced by the gate oxide defects under 1000-hr negative bias (-5 V) is similar for both types of devices Fig. 7 (d) illustrates that the forward blocking leakage current degradations of both types of devices have similar trends and fluctuations at a similar level within the 1000-hr stress. It is worth mentioning that both the $V_F$ and $R_{ON}$ degradations of the RT implanted devices and the HT implanted devices increase significantly at the early 100-hr stage and eventually tend to saturate. The saturated degradation level is very close to the degradation level after 100-hr stress. Therefore, the conclusion that the RT implantation has the potential to replace the HT implantation in the fabrication of 3.3 kV 4H-SiC MOSFETs is also believed to be valid for 1000-hr stress conditions.

## IV. CONCLUSION

This paper has compared the body diode degradation of commercial 3.3 kV 4H-SiC power MOSFETs with the heated ion implantation and the ion implantation at room temperature, with equivalent doses and energy of the same implants for both types of devices. The results indicate that the ion implantation at room temperature has the potential to replace the heated ion implantation in the fabrication of commercial 3.3 kV 4H-SiC power MOSFETs, with a highly qualified 4H-SiC substrate and the latest generation of process. This replacement can help the industry eliminate the purchase and maintenance costs of heating equipment, and the step of device cooling in the fabrication to shorten the production cycle. Further investigation is needed to check if the conclusion applies to higher-voltage (>3.3 kV) devices since the thicker drift layer of the higher-voltage devices enhances the BPDs formation, whether this conclusion applies to higher-voltage (>3.3 kV) devices still needs to be investigated.

## ACKNOWLEDGEMENT

This research is supported in part by the US Department of Energy (DOE), the Office of Energy Efficiency and Renewable Energy (EERE), the Advanced Manufacturing Office (AMO), and technical support from Microchip Technology Inc. The authors would also like to thank National Renewable Energy Laboratory (NREL) for the helpful discussions.

## REFERENCES

[1] Galeckas., et al., "Recombination-enhanced Extension of Stacking Faults in 4H-SiC p-i-n Diodes under Forward Bias", *Applied Physics Letters*, Vol. 81, issue 5, pp. 883-885, 2002.

[2] K. Konishi., et al., "Investigation of Forward Voltage Degradation due to Process-Induced Defects in 4H-SiC MOSFET", *Materials Science Forum*, Vol. 924, pp. 365-368, 2018.

[3] T. Tawara., et al., "Suppression of the Forward Degradation in 4H-SiC PiN Diodes by Employing a Recombination-

Enhanced Buffer Layer", *Materials Science Forum*, Vol. 897, pp. 419-422, 2016.

[4] Z. Zhang., et al., "Basal Plane Dislocation-free Epitaxy of Silicon Carbide", *Applied Physics Letters*, Vol. 87, issue 15, 2005.

[5] Z. Zhang., et al., "Mechanism of Eliminating Basal Plane Dislocations in SiC Thin Films by Epitaxy on an Etched Substrate", *Applied Physics Letters*, Vol. 89, issue 8, 2008.

[6] K. Konishi., et al., "Stacking Fault Expansion from Basal Plane Dislocations Converted into Threading Edge Dislocations in 4H-SiC Epilayers under High Current Stress", *Journal of Applied Physics*, Vol. 114, issue 1, 2013.

[7] A. Agarwal., et al., "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs," *IEEE Electron Device Letters*, Vol. 28, no. 7, pp. 587-589, 2007.

[8] R. Stahlbush., et al., "Defects in 4H-SiC Epilayers Affecting Device Yield and Reliability," *IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022.

[9] J.F. Michaud., et al., "Aluminum Implantation in 4H-SiC: Physical and Electrical Properties," *Materials Science Forum*, Vol. 740-742, pp. 581-584, 2013.

[10] M. Kang et al., "Body Diode Reliability of Commercial SiC Power MOSFETs", *IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019.