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A New Cell Topology for 4H-SiC Planar Power MOSFETs and Comparison with Hexagonal and Octagonal Cell Topologies

Shengnan Zhu*, Tianshi Liu*, Arash Salemi†, Michael Jin*, Marvin H. White*, David Sheridan†, and Anant K. Agarwal*
*Department of Electrical and Computer Engineering, The Ohio State University, OH, USA (zhu.2670@osu.edu)
†Alpha and Omega Semiconductor, Sunnyvale, CA, USA

***Abstract*—A new Dodecagonal (polygon with twelve sides, short for Dod) cell topology is designed for 4H-SiC planar power MOSFETs. The Dod cell is used in the layout design of the 650 V SiC MOSFETs. The nominal Hexagonal (Hex) cell and a recently published Octagonal (Oct) cell are also used on the 650 V SiC MOSFET layout designs for comparisons. The devices are fabricated, diced, and packaged for static and dynamic characterizations. Experimental results show that the Hex-cell MOSFET has the lowest specific ON-resistance ($R_{on,sp}$) and is suitable for high-power applications. The Dod and Oct-cell MOSFETs have much smaller gate-drain capacitance than Hex-cell MOSFETs, making them good candidates for high-frequency applications. The new Dod cell is designed with optimized channel density to have reduced $R_{on,sp}$ compared to the Oct cell.**

***Index Terms*—SiC planar power MOSFET, Cell topology, High-frequency switching, High-frequency figure of merit (HF-FOM), Dodocagonal cell, Octagonal cell.**

I. Introduction

Due to the high operation temperature, fast switching speed, and low switching loss, silicon carbide (SiC) power MOSFETs are gaining increasing attention in the semiconductor industry and electric vehicles (EVs) market [1], [2]. The JFET region and cell topology designs are studied to improve the static and dynamic performances of SiC MOSFETs [3]–[5]. The Hexagonal (Hex) cell topology is a conventional cell topology that is used in SiC power MOSFETs. The devices with Hex cell topology usually have low specific ON-resistance ($R_{on,sp}$) due to the high channel density. Recently, an octagonal (Oct) cell topology was used on 1.2 kV SiC planar power MOSFETs to improve the high-frequency figures-of-merit (HF-FOM) compared with traditional Linear cells [3]. The Oct cell is designed with minimized JFET region area to achieve a low gate-drain capacitance (C_{gd}). The C_{gd}, which is known as the Miller capacitance, essentially determines the drain voltage slew rate during the switching transient [6]. Thus, the Oct-cell devices have a high switching speed and are suitable for high-frequency applications [7]. However, the Oct cell achieves low JFET density with a low channel density, resulting in a high $R_{on,sp}$.

This work reports a new cell topology called dodecagonal (polygon with twelve sides, short for Dod) cell. The Dod cell is designed to achieve a low C_{gd} with a low JFET density. The Dod cell has a $1.6\times$ higher channel density than the Oct cell, hence lower $R_{on,sp}$. The Dod cell has been used for 650 V SiC planar power MOSFETs for the first time. The Hex and Oct cells are also used on the layout designs of the 650 V SiC MOSFETs for comparisons. The devices were fabricated, packaged, and characterized.

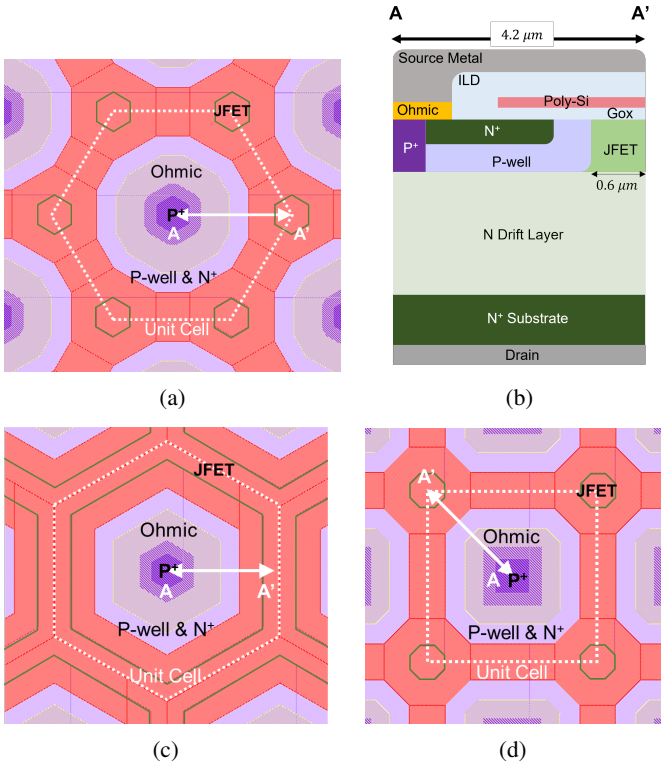


Fig. 1: (a) Layout of the Dod cell topology, (b) cross-sectional view along AA' of the designed 650 V SiC MOSFETs, (c) Layout of the Hex cell topology, and (d) Layout of the Oct cell topology.

II. Device Design and Fabrication

The Dod cell topology is shown in Fig. 1a. Six hexagonal JFET regions are located at the corners of the hexagonal unit cell. Poly-Si gate (hexagonal shapes connected by rectangles) is on the top of the JFET regions. A P^+ dodecagon (twelve-sided polygon) is located in the center of the unit cell with a

TABLE I: Design parameters for the 650 V SiC MOSFETs

Cell topology	Dod	Hex	Oct
Half Cell pitch [μm]	4.2	4.2	4.2
Active area [mm^2]	0.64	0.64	0.64
Channel density [μm^{-1}]	0.181	0.408	0.113
JFET density [unitless]	0.055	0.265	0.034

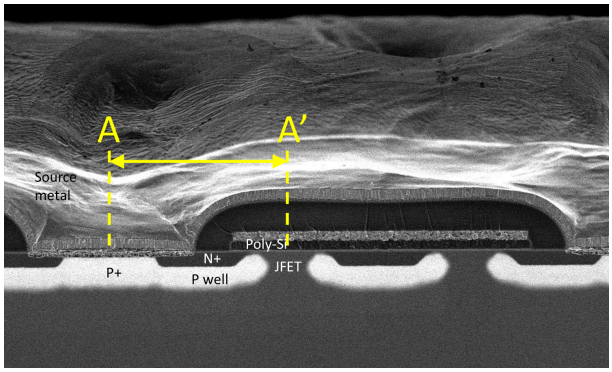


Fig. 2: Cross-sectional SEM image of the fabricated 650 V Dod-cell SiC power MOSFET. The AA' is correspond to the cross-sectional view in Fig. 1b.

dodecagonal Ohimc contact on top. The cross-sectional view of the designed 650 V SiC MOSFETs is shown in Fig. 1b. The same cross section is used for a conventional Hex cell layout (Fig. 1c) and the Oct cell layout (Fig. 1d). Design parameters for the MOSFETs with different layouts are listed in Table I. All devices have the same edge termination and die size as described in [5]. The 650 V MOSFETs are fabricated on a 6-inch SiC wafer by a state-of-art commercial SiC foundry. The cross-sectional SEM image of the fabricated Dod-cell MOSFET is shown in Fig. 2. Devices are packaged into open-cavity TO-247 packages for characterizations.

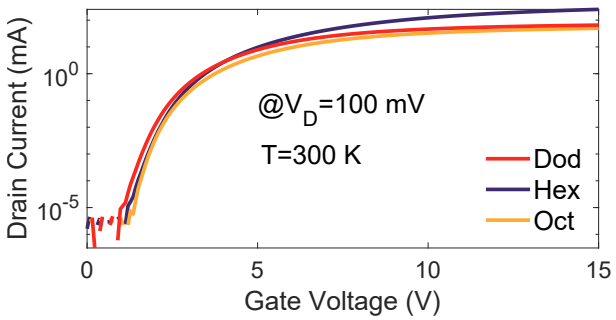
III. Experimental Results

A. Threshold Voltage and Breakdown Voltage

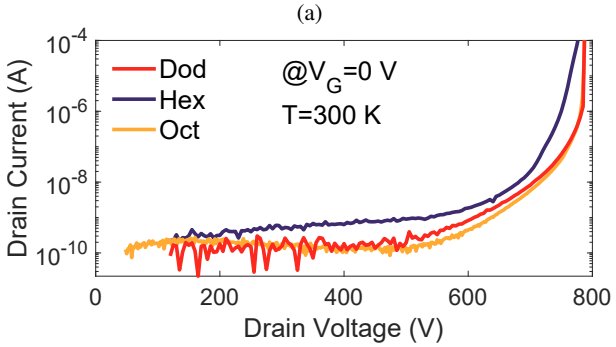
The transfer and blocking characteristics of the 650 V SiC power MOSFETs are measured using a Keysight B1506A power semiconductor analyzer and the results are shown in Fig. 3. The threshold voltage (V_{th}) and the breakdown voltage (BV) of the devices are extracted and listed in Table II. Minimal V_{th} difference is observed among the MOSFETs. The devices under test (DUTs) have similar BV of $\sim$780 V. The drain leakage currents are less than 10 nA up to 650 V for all the DUTs.

B. Specific ON-resistance

Fig. 4 shows the output characteristics (measured using Keysight B1506A) of the 650 V SiC MOSFETs with different cell topologies. A 3$\times$ higher drain current (I_D) at drain voltage (V_D) of 1.5 V is observed for Hex-cell MOSFET compared to Dod-cell MOSFET, which is contributed by the higher channel density and higher JFET density of Hex cell topology.



(a)



(b)

Fig. 3: (a) Transfer, (b) blocking characteristics of the 650 V SiC power MOSFETs.

TABLE II: Experimental results for the 650 V SiC MOSFETs

Cell topology	Dod	Hex	Oct
V_{th}@I_D = 1mA [V]	3.38	3.38	3.65
BV@I_D = 100μA [V]	787.2	776.7	787.3
$R_{on,sp}$@V_D = 1.5V [$m\Omega \cdot cm^2$]	8.34	2.54	15.35
C_{gd}@V_D = 400V [pF]	1.63	8.05	1.59
HF $-$ FOM($C_{gd} \times R_{on}$) [$\Omega \times pF$]	2124	3195	3814
dV/dt_{on} [V/ns]	11.50	*	5.71
$E_{loss,on}$ [μJ]	21.02	*	31.04
dV/dt_{off} [V/ns]	10.51	*	7.29
$E_{loss,off}$ [μJ]	4.86	*	5.72
$E_{loss,total}$ [μJ]	25.88	*	36.76
SCWT [μs]	>15	4	>15

*Not tested due to a different current rating.

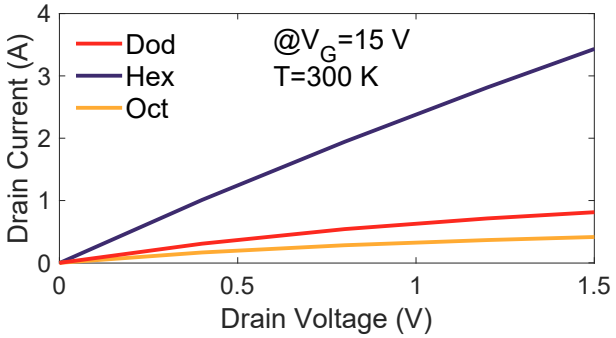


Fig. 4: Output characteristics of the 650 V SiC power MOSFETs.

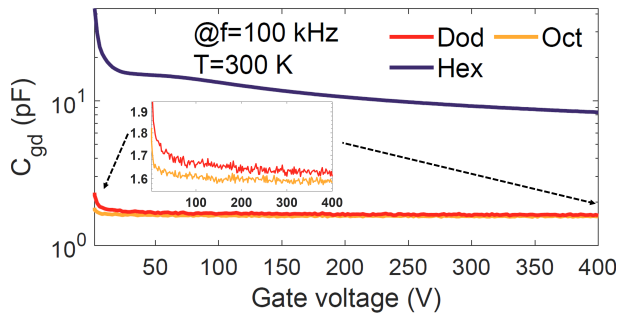


Fig. 5: Gate-drain capacitance of the 650 V SiC power MOSFETs.

The channel density is defined as the total channel width in a unit cell divided by the unit cell area. A higher channel density indicates more conduction current and lower channel resistance. The JFET density is the JFET region area in a unit cell divided by the unit cell area. A higher JFET density implies a lower JFET region resistance. The specific ON-resistances ($R_{on,sp}$) for the 650 V SiC MOSFETs are extracted and listed in Table II. The Dod-cell MOSFET produces a $1.8\times$ smaller $R_{on,sp}$ compared to the Oct-cell MOSFET.

C. Gate-drain Capacitance

The gate-drain capacitances (C_{gd}) of the fabricated 650 V SiC power MOSFETs are measured using a Keysight B1505A power semiconductor analyzer. The results are shown in Fig. 5. The Dod and Oct-cell MOSFETs have roughly one order of magnitude smaller C_{gd} than the Hex-cell MOSFET. The C_{gd} of a SiC planar power MOSFET is strongly related to the JFET region design [5]. The Dod and Oct cell topologies are designed with minimized JFET regions (low JFET densities), contributing to small C_{gd}. The C_{gd} at $V_D = 400V$ is extracted for all DUTs in Table II. Dod and Oct-cell MOSFET achieves $5\times$ smaller C_{gd} compared to Hex-cell MOSFET. The HF-FOMs of the 650 V SiC MOSFETs are also calculated. The Dod-cell MOSFET obtains the lowest HF-FOM as listed in Table. II, indicating a better high-frequency switching performance.

D. Switching Performance

It has been demonstrated that the Oct-cell devices have a faster switching performance and lower switching energy loss than the Hex-cell devices [7]. Thus the switching performance of the Dod-cell and Oct-cell MOSFETs are compared in this section. The Double-pulse tests are conducted on the Dod-cell and Oct-cell 650 V SiC power MOSFETs under a gate voltage (V_G) of 20 V, $V_D = 400V$, and $I_D = 2A$. The turn-on and turn-off waveforms are shown in Fig. 6.

The dv/dt and switching losses during turn-on and turn-off transients are extracted for all DUTs and listed in Table II. During the turn-on procedure, the Dod-cell obtains $2\times$ higher turn-on dv/dt and $1.5\times$ lower switching loss than the fabricated Oct-cell MOSFET. During the turn-off transient, the Dod-cell MOSFET shows a $1.4\times$ higher dv/dt and a lower switching loss than the measured Oct-cell MOSFET. The total switching

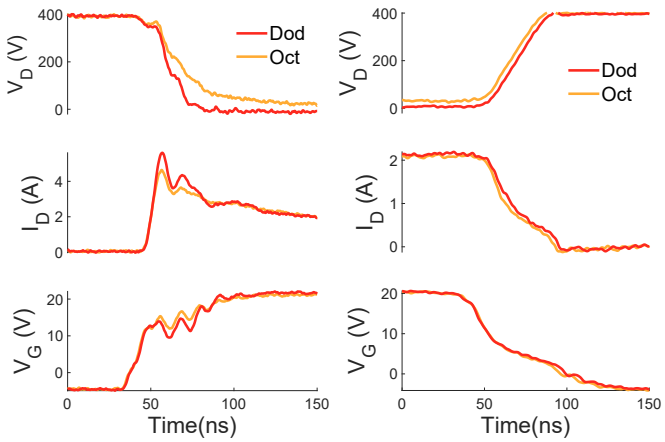


Fig. 6: (a) Turn-on, (b) turn-off waveform for the 650 V SiC power MOSFETs.

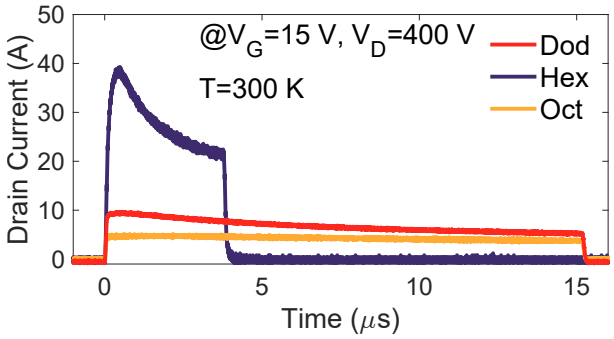


Fig. 7: Drain current waveform during short-circuit test of the 650 V SiC power MOSFETs.

losses are also calculated. Lower switching loss energy is observed for the Dod-cell MOSFET than the Oct-cell MOSFET.

E. Short-circuit Performance

The short-circuit measurements are conducted on the fabricated 650 V SiC power MOSFETs at $V_G = 15V$ and $V_D = 400V$. The Drain current waveforms are shown in Fig. 7. For the Hex-cell MOSFET, the waveform refers to that last test before device failure. For the Dod and Oct-cell MOSFETs, the devices survived for up to $15\mu s$ and the waveforms are from the last test when the time frame equals $15\mu s$. Due to the lower ON-resistance (R_{on}), the Hex-cell MOSFET shows a $4\times$ higher peak current than the Dod-cell MOSFET during the short-circuit events. The Oct-cell MOSFET shows the lowest peak current, corresponding to its highest R_{on} among all devices. The lowest R_{on} also results in the lowest short-circuit withstand time (SCWT) for Hex-cell MOSFET [8]. The measured SCWT for Hex-cell MOSFET is $4\mu s$. For the Dod and Oct-cell MOSFETs, the SCWTs are more than $15\mu s$.

IV. Conclusion

A new Dod cell topology is used on 650 V SiC planar power MOSFET. The conventional Hex cell and the recently

published Oct cell are also used in the device layout design. The devices are fabricated and packaged for static and dynamic characterizations. The experimental results demonstrate that the Hex-cell MOSFET has the best static performance with the lowest $\mathrm{R_{on,sp}}$ and can be used in high-power applications. The Dod and Oct cells are suitable for high-frequency applications due to their small $\mathrm{C_{gd}}$ and low HF-FOMs. Compared to the Oct cell, the Dod cell has a lower $\mathrm{R_{on,sp}}$ due to optimized topology design that has a higher channel density.

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