Investigation of different screening methods on threshold voltage and gate oxide lifetime of SiC Power MOSFETs

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***Abstract*—The effects of different screening methods for non-infant extrinsic defects on the gate oxide reliability of commercial 1.2 kV 4H-SiC power MOSFETs are investigated. This study aims to find the optimal screening voltage and duration for high gate-voltage pulse screening and long-term burn-in with acceptable constraints on threshold voltage (V_{th}) shift and oxide lifetime degradation. The V_{th} is monitored during the stress and recovery process under various screening conditions. SiC MOSFETs with the trench structure can be screened at high voltages due to the thicker gate oxide. Moreover, an optimized screening method is proposed which uses a multi-pulse mode screening technique to reduce the effects of high gate voltages on the permanent shift of V_{th}. Furthermore, constant-voltage time-dependent dielectric breakdown measurements are conducted on SiC MOSFETs with and without high-voltage screening. The results reveal that high voltage applied for a short period of time (≤ 1 s) has no obvious negative impact on the oxide lifetimes of SiC MOSFETs.**

***Index Terms*—Screening, Gate oxide lifetime, Threshold voltage, Burn-in, Extrinsic failure, Electron and hole trapping, Pulse.**

I. INTRODUCTION

Silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) are attracting attention from the power electronics industry due to their lower switching losses, and the capability to operate at both high temperatures and frequencies compared to Si-based power devices [1]. Considering the stringent requirements of the automotive industry for the reliability of devices, the gate oxide reliability of SiC power MOSFETs is a critical consideration. Although SiC MOSFETs exhibit enough intrinsic oxide lifetime at high temperatures [2, 3], SiC MOS structures have abundant extrinsic or early gate oxide failures which significantly determine overall product reliability [4-6]. There are several viewpoints on the origin of early failures. Aichinger et al. believe local oxide thinning due to the tiny distortions in the gate oxide can be used to explain the phenomenon of early breakdown [7]. Chbili et al. propose a new lucky defect model. Bulk defects in the gate oxide introduced during growth are responsible for extrinsic failures of gate oxide [6]. Some individual devices with large extrinsic defect density have a high failure probability and cannot meet the 20-year operational requirement. Therefore, it is necessary to implement effective screening techniques that remove potentially defective and unreliable devices. The failure probability of the remaining industrial devices can be adequately decreased [8].

There are two conventional screening techniques to identify and eliminate weak SiC power MOSFETs. One method is to use a fast high gate-voltage stress pulse to screen each device at room temperature or high temperatures [9, 10]. This technique can be carried out on wafer-level devices with automated probes to screen individual chips. Threshold voltage (V_{th}) shift and oxide lifetime degradation cannot be neglected under high gate voltage conditions even for a short screening time. Another method is called burn-in which is primarily used for packaged SiC MOSFETs. During burn-in, devices are stressed at lower screening voltages and high temperatures for a long time to screen out enough extrinsic failures. Although this approach is time-consuming and causes a large V_{th} shift [11], prolonged oxide screening enhances the possibility of removing devices with extrinsic defects, allowing better reliability of gate oxide for the remaining devices.

Efficient screening technology is required to screen out extrinsic failures without significantly shifting V_{th} or degrading the intrinsic lifetime of the gate oxide. Increasing the screening voltage and time at elevated temperatures ensures that more devices with early failures are filtered out.

However, manufacturers may adopt conservative screening conditions, which cause a portion of shipped devices with unreliable gate oxide to fail during operation. Additionally, the issue of V_{th} shifts caused by gate oxide screening have not been adequately addressed.

To guarantee adequate screening efficiency for these two approaches, it is required to determine the optimal screening voltage and duration to make V_{th} recover substantially without significantly decreasing gate oxide lifetimes. In this paper, the influences of screening conditions on V_{th} of commercial SiC planar and trench MOSFETs are monitored and compared. In addition, an innovative screening approach is introduced to suppress the V_{th} shift during the screening process. The gate oxide lifetimes of commercial SiC power MOSFETs with and without gate oxide screening are evaluated with time-dependent dielectric breakdown (TDDB) measurements at 150°C.

II. Device and Test Procedure Description

The commercial 1.2 kV SiC power MOSFETs packaged in TO-247 from two vendors are used in this work. These devices have been through some type of oxide screening or burn-in treatments by manufacturers. Table 1 shows the general information of vendor E devices with planar gate structure and vendor K devices with trench gate structure. Fig. 1 depicts the cross-sectional views of commercial SiC power MOSFETs from vendor E and vendor K. A semiconductor parameter analyzer (B1506A, Keysight, Inc) is used to test the relevant parameters of SiC MOSFETs. The ON-resistance (R_{on}) is obtained at V_{ds} = 1 V and the maximum operating gate voltage. To obtain gate oxide thickness (t_{ox}), gate oxide breakdown voltages are measured at 150°C as shown in Fig. 2. t_{ox} is calculated based on the average oxide breakdown voltages (V_{BR}) at 150°C, with the assumption that the critical oxide breakdown electric field is 11 MV/cm. The estimated t_{ox} is ~ 46.4 nm for SiC planar MOSFETs and ~ 68.2 nm for SiC trench MOSFETs, respectively.

To monitor the shifts of V_{th} before and after gate oxide screening treatment, a schematic of the V_{th} test sequence used in this study is shown in Fig. 3. V_{th} is read out during the stress and recovery process by using the constant current method. An initial threshold voltage (V_{th-pre}) at RT is measured to establish a reference for comparison. The screening temperature is set at 150°C to screen early failures. During the screening, gate voltage stress is applied with source and drain grounded. The V_{th} before and after gate oxide screening at 150°C are measured as V_{th1} and V_{th2}, respectively. ΔV_{th1} is equal to the difference between V_{th1} and V_{th2} which represents the V_{th} shift after the screening process. After stress, the device is cooled back to room temperature without the gate voltage stress. The recovery in V_{th} occurs when the stress is removed from the device. V_{th} is recorded during the recovery process until the value of V_{th} stabilizes (V_{th3}). ΔV_{th2} is defined as the difference between V_{th-pre} and V_{th3} which represents the V_{th} shift after the recovery phase.

TABLE I. Information for Commercial SiC Mosfets

Vendor	E	K
Voltage rating (V)	1200	1200
R_{on} (mΩ)	280	220
Gate structure	Planar	Trench
Oxide breakdown voltage (V)	~ 51	~ 75
Gate oxide thickness (nm)	~ 46.4	~ 68.2

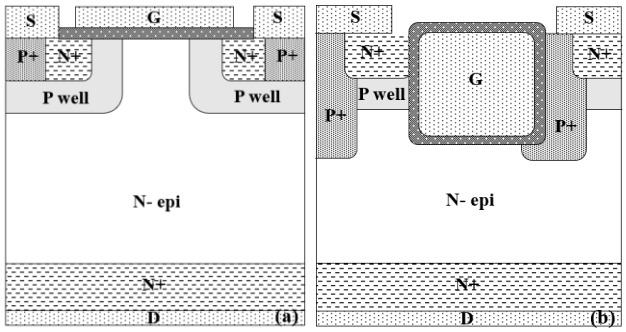


Figure 1. Cross-sectional schematic of (a) SiC planar MOSFET from vendor E and (b) SiC trench MOSFET from vendor K.

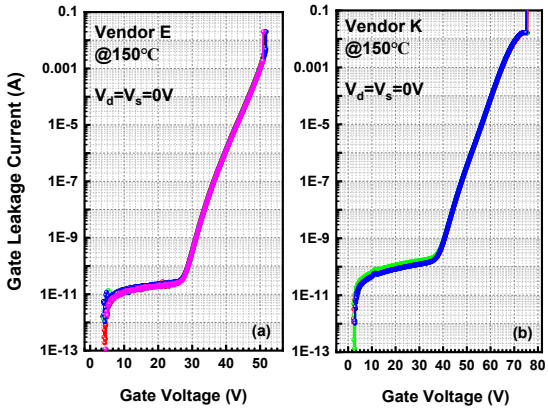


Figure 2. Gate leakage current versus gate voltage characteristics of (a) vendor E and (b) vendor K devices at 150°C.

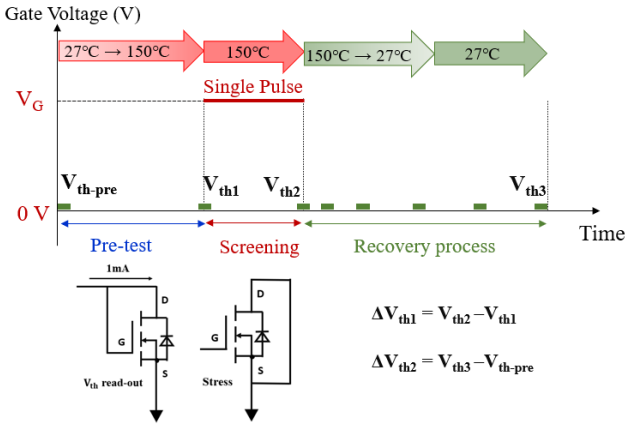


Figure 3. Measurement sequence of V_{th} before and after gate oxide screening.

Constant-voltage TDDB measurements are performed to obtain the oxide lifetimes of commercial SiC power

MOSFETs under different gate oxide fields (E_{ox}) at 150°C. During the TDDB measurement, a constant voltage is applied to the gate electrode, while the drain and source are grounded. For each value of E_{ox}, ten devices with similar V_{th} are selected for TDDB measurement. The gate leakage currents of the ten devices are recorded using a 10-channel digital multimeter during the TDDB measurement until dielectric breakdown at 150°C. The Weibull distribution of ten devices' gate oxide lifetimes is used to extract the gate oxide lifetime ($t_{63\%}$) at a defined E_{ox}. (Method described in more detail in [12, 13]). The oxide lifetime under the operational condition can be predicted based on the thermal-chemical E-model [14]. The TDDB analysis approach gives an obvious visualization of the $t_{63\%}$ under various E_{ox} conditions and facilitates the study of the effects of different gate oxide screening conditions on the lifetime of SiC MOSFETs. The $t_{63\%}$ of the devices subjected to different screening conditions are measured and compared with $t_{63\%}$of the devices that are not screened. The purpose of this investigation is to guarantee that the screening technique can prevent potential damage to the oxide of good devices.

III. Results and Discussion

In this section, V_{th} shift and recovery of SiC MOSFETs after different oxide screening treatments are investigated to determine recommended oxide screening conditions for vendor E and vendor K devices. In addition, an optimized screening approach is proposed to limit the shift in V_{th}. The gate oxide lifetimes of SiC MOSFETs with and without screening treatments are measured and compared using the TDDB method to avoid drastically reducing the intrinsic lifetime through the screening procedure.

A. Effect of screen, E_{ox} and time, on V_{th}

V_{th} shifts after oxide screening (ΔV_{th1}) at an ambient temperature of 150°C are depicted in Fig. 4. The positive and negative charge trapping in SiO_2 , especially in the region near SiO_2/SiC interface leads to V_{th} shift [15]. The dominance of electron trapping or hole trapping depends on the screen E_{ox} and time [16, 17]. For vendor E devices, with the planar gate structure, V_{th} displays distinct behaviors under different E_{ox} conditions when the screening time is 100 ms [Fig. 4(a)]. When the screen E_{ox} is in the range of 4 MV/cm to 8 MV/cm, capture of electrons occurs in the SiO_2, which causes V_{th} to shift positively. When E_{ox} exceeds 8 MV/cm, the holes originating from impact ionization and/or anode hole injection (AHI) get trapped in the SiO_2 resulting in a decrease of ΔV_{th1} [18, 19]. V_{th} shift approaches 0 V at E_{ox} of around 9 MV/cm, because the effects of hole trapping and electron trapping on V_{th} are canceled out by each other. V_{th} shifts in a negative direction when E_{ox} is larger than 9 MV/cm. This phenomenon indicates that hole trapping in the gate oxide is dominant. Negative V_{th} shifts lead to a significant increase in drain leakage current under reverse bias conditions and seriously degrade long-term reliability [20], so the behavior of negative threshold voltage shift should be avoided. It is useful to note that no negative threshold voltage shift occurs at screening voltages less than ~ 41 V and ~ 54 V for vendor E and vendor K devices, respectively.

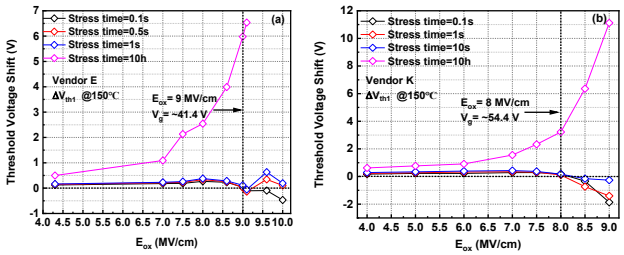


Figure 4. ΔV_{th1} of (a) vendor E devices and (b) vendor K devices as a function of E_{ox} for various stress times.

With the increase in screening time, the V_{th} shift undergo a transition from negative to positive values at high E_{ox} (> 9 MV/cm). This phenomenon can be explained by the fact that hole trapping contributes to an enhanced electric field at the SiO_2/SiC interface, and as a result, more electrons can tunnel into the gate oxide and get trapped. Subsequently, the electric field is reduced at the SiO_2/SiC interface resulting in reduced electron injection so that impact ionization and/or AHI is suppressed and therefore electron trapping overtakes hole trapping. When the stress time is 10 hours, a high number of electrons are concentrated in the oxide layer causing a high ΔV_{th1} and the effect of hole trapping is dominated by electron trapping.

The quality of the oxide layer and its interface is responsible for the threshold voltage shift value. In the case of SiC trench MOSFETs, vendor K device has a larger ΔV_{th1} compared to the vendor E device with the planar gate structure [Fig. 4(b)], which reflects that the gate oxide, possibly deposited, has more defects or more interface states generated during a prolonged stress period resulting in more possibilities for electrons to be captured. The authors are doing threshold voltage hysteresis measurements to investigate the variation of interface state density (D_{it}) during E_{ox} stress. The analysis of the effects of screening E_{ox} and time on D_{it} will be published.

B. V_{th} recovery after screening

The V_{th} shifts after the screening process influence the subsequent recovery of V_{th}. Fig. 5 shows the V_{th} during the screening and recovery phase observed on vendor E devices. ΔV_{th1} is 0.19 V when E_{ox} of 8 MV/cm is applied for 100 ms. After stress, V_{th} starts to increase with decreasing temperature. Electrons trapped at the interface and in shallow bulk traps in the gate oxide re-emit at high temperatures, thus making V_{th} of SiC MOSFET at high temperatures lower than V_{th} at room temperature [21]. Ultimately, the V_{th} shift after the recovery process (ΔV_{th2}) is 0.11 V. This is the residual shift due to the screening process.

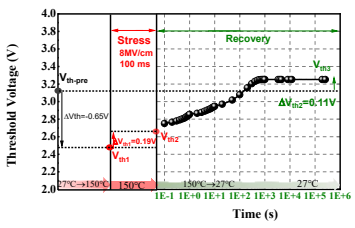


Figure 5. V_{th} for vendor E devices during the stress phase and recovery phase under E_{ox} of 8 MV/cm and stress time of 100 ms.

Fig. 6 plots ΔV_{th2} of vendor E and vendor K devices subjected to various E_{ox} stress levels with a duration of 100 ms and 1 s. The left Y-axis shows ΔV_{th2}, the residual shift after the recovery process. The right Y-axis is the ratio of ΔV_{th2} to initial V_{th}. For vendor E devices, ΔV_{th2} is positive due to the electron trapping when E_{ox} of less than 9 MV/cm is applied for 100 ms [Fig. 6 (a)]. And ΔV_{th2} is approximately less than 5% of the initial value. It should be noted that V_{th3} shows a negative shift compared to the initial value after high E_{ox} (> 9 MV/cm) stress for 100 ms due to the dominance of hole trapping. This phenomenon needs to be taken seriously in the industry because a pronounced reduction in threshold voltage can lead to an increase in the leakage current of SiC MOSFETs in the OFF state and has the potential to turn the device to normally-on. To prevent negative V_{th} shift of vendor E devices, the recommended screening voltage should be kept below ~ 41 V for 100 ms. The V_{th} recovery of vendor E devices is susceptible to the impact of screening time. From the test results, it can be found that electron trapping still dominates even at high E_{ox} (> 9 MV/cm) when the screening time is 1 s. Despite the increased screening time of 1 s, the V_{th} shift does not exceed 5% of the initial value after the recovery process.

Due to the thicker oxide, negative ΔV_{th2} appears only when the screening voltage exceeds ~ 54 V for vendor K devices. A large screening voltage can be applied to vendor K devices without causing ΔV_{th2} to exceed 10% of its initial value [Fig. 6 (b)]. Previous studies have shown that the higher the ratio of screening voltage to gate use-voltage, the higher the efficiency of the screening technology [7]. Thus, a lower field failure probability after screening treatment for vendor K devices can be acquired. Possibly due to the nature of defects in the gate oxide of trench mode devices, both the curves in Fig. 6 (b) turn negative at 8 MV/cm meaning hole trapping dominates above 8 MV/cm.

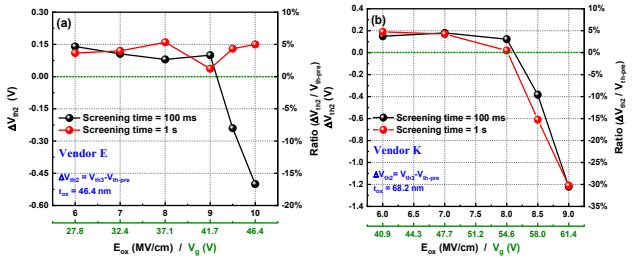


Figure 6. Effect of 100 ms/1 s high gate-voltage pulse screening on the ΔV_{th2} of (a) vendor E devices, and (b) vendor K devices. Devices are screened at 150°C.

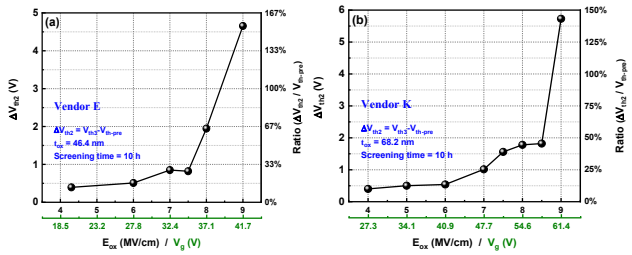


Figure 7. Effect of burn-in on the ΔV_{th2} of (a) vendor E devices, and (b) vendor K devices. The temperature of burn-in is 150°C.

Fig. 7 exhibits the ΔV_{th2} of the vendor E and vendor K devices after 10 hours of burn-in. It can be observed that when E_{ox} in burn-in is below 6 MV/cm, ΔV_{th2} is below 20% of the initial value for both vendor devices. However, high E_{ox} (> 6 MV/cm) applied at 150°C for 10 hours induces a large deviation between the final V_{th} and the initial value even after a long recovery time. The larger screening E_{ox}, the more difficult it is for V_{th} to return to its initial value due to the accumulation of electrons in the oxide layer. It is also typical to notice that vendor K devices can accept higher screening voltages in burn-in processing for the same range of V_{th} variations. This suggests that higher voltages can be selected for screening vendor K devices during burn-in, thus improving the possibility of removing non-infant extrinsic failures.

C. Optimization of screening technology

By recording the V_{th} shift and recovery of SiC MOSFETs after high gate-voltage pulse screening and burn-in, it can be concluded that the impacts of conventional screening techniques on V_{th} cannot be avoided. The increase in V_{th} leads to an increase in the ON resistance and reduces the power efficiency of SiC MOSFETs. Therefore, it is necessary to adopt an optimized screening technique to limit the V_{th} shift of SiC MOSFETs under high voltage or long-time stress conditions.

The forward shift of V_{th} originates from the trapped electrons in the oxide. The effect of electron trapping can be weakened by hole trapping. Considering this concept, an innovative screening method is designed to have a negligible impact on V_{th}. For the conventional high gate-voltage pulse screening method, a single pulse with a defined amplitude and duration is applied to the gate. Electrons tunnel into the gate oxide and get trapped at the high gate voltage. Some electrons still accumulate in the oxide even after the stress is removed for a long time, making it difficult to restore V_{th} to its initial value. To overcome this problem, a multi-pulse screening method is developed to counteract the effect of these negative charges on the V_{th} of SiC MOSFETs. The screening test procedure in multi-pulse mode is shown in Fig. 8. The multi-pulse screening method introduces a base gate voltage of -5 V. The pulse period is 5 ms. The duty ratio is the ratio of the duration of positive screening E_{ox} to the pulse period. The ΔV_{th2} of vendor E and vendor K devices treated by single-pulse screening and multi-pulse screening are shown in Fig. 9. It can be clearly observed that the high gate-voltage screening with multiple pulses effectively suppresses V_{th} shift. This result can be explained by the fact that when a negative voltage is applied to the gate, the holes accumulated in the valence band are captured by oxide traps, meanwhile the captured electrons under positive voltage tunnel back into the conduction band [22]. For vendor E devices, ΔV_{th2} after the multi-pulse screening with a duty ratio of 50% is negative [Fig. 9 (a)] since the impact of hole trapping in oxide exceeds the impact of electron trapping. A duty ratio of 80% reduces the possibility of holes being trapped in the oxide, thus preventing the negative V_{th} shift of vendor E devices. Choosing the appropriate duty ratio can balance the impact of electron trapping and hole trapping and make the V_{th} shift close to 0 V. For vendor K devices

with trench gate structure, a multi-pulse screening process with a 50% duty ratio allows V_{th} to basically return to its initial value [Fig. 9 (b)].

During burn-in, the prolonged oxide electric field stress causes the phenomenon that V_{th} is difficult to recover completely. If negative stress can be included in the continuous voltage stress process to allow electrons to be released and holes to be captured, it can prevent a large number of negative charges from accumulating in the oxide. The burn-in technology in multi-pulse mode with a total stress time of 10 hours, a pulse period of 1 s, and a duty ratio of 50% is illustrated in Fig. 10. Gate voltage stress transitions from positive screening voltage to -5 V. The effects of burn-in with multiple pulses and constant voltage on V_{th} are demonstrated in Fig. 11. The burn-in processing time for both modes is 10 hours. For the two types of SiC MOSFETs with different gate structures, the multi-pulse burn-in approach suppresses V_{th} shift to a certain extent, thus allowing SiC MOSFETs to be treated by burn-in at higher gate voltage without causing dramatic V_{th} variations. The implication of these results is that applying a negative voltage stress can facilitate the recovery of V_{th} , thus reducing the effect of high voltage and long-time stress on V_{th}.

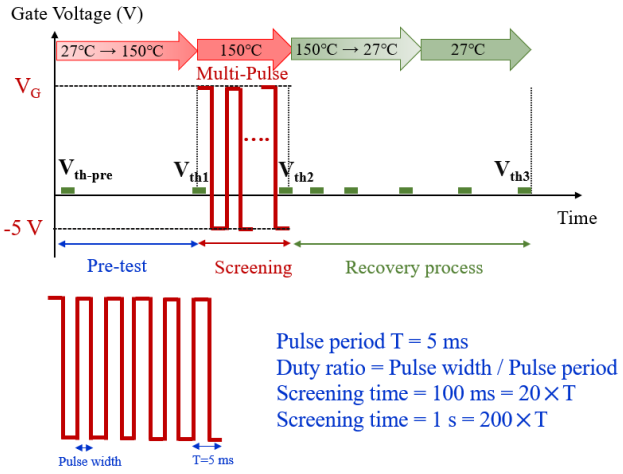


Figure 8. Measurement sequence of V_{th} before and after high gate-voltage multi-pulse screening.

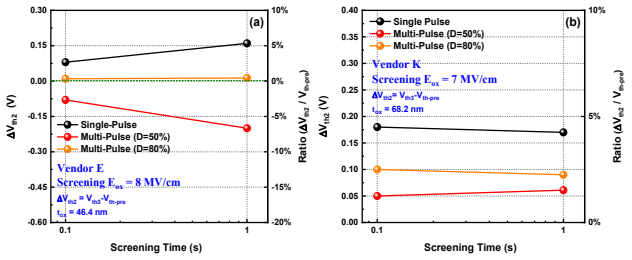


Figure 9. Effect of high gate-voltage single-pulse and multi-pulse screening on the ΔV_{th2} of (a) vendor E devices, and (b) vendor K devices.

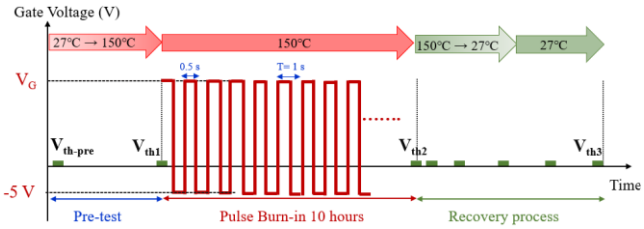


Figure 10. Measurement sequence of V_{th} before and after multi-pulse burn-in. The total time for the multi-pulse burn-in process is ten hours.

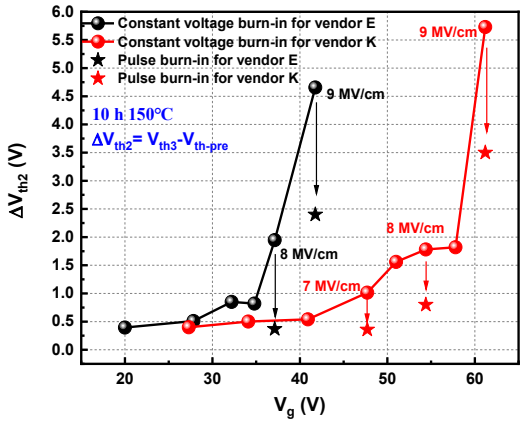


Figure 11. Effect of constant voltage and multi-pulse burn-in on the ΔV_{th2} of vendor E and vendor K devices.

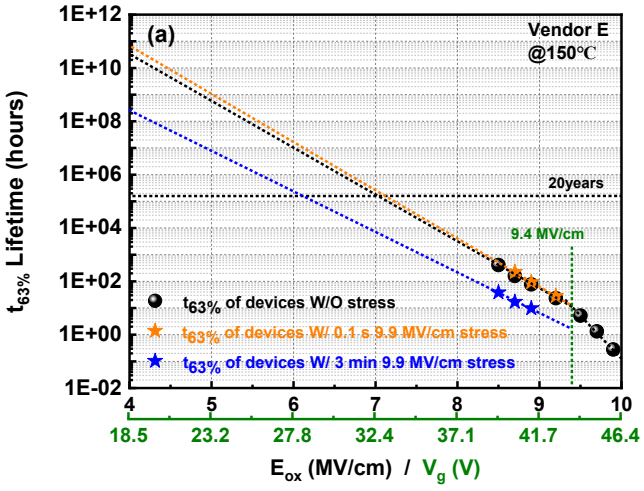
D. Effect of screening technology on the oxide lifetime

The screening technique must satisfy both the negligible impact on V_{th} and the requirement to not sacrifice oxide's intrinsic lifetime. Although high voltage or prolonged screening can reduce the oxide failure rate to levels acceptable for high reliability, there is a threat of oxide's intrinsic lifetime degradation. Therefore, it is necessary to measure and compare the oxide's lifetimes of SiC MOSFETs without and with different screening treatments. Constant-voltage TDDB measurements are initially performed on vendor E and vendor K devices without high gate-voltage screening. From the Weibull distributions, $t_{63\%}$ of SiC MOSFETs at various E_{ox} are extracted. Subsequently, a new batch of vendor E and vendor K devices are selected for the oxide screening treatments, followed by constant-voltage TDDB measurements to obtain $t_{63\%}$ of the screened SiC MOSFETs.

Comparison of gate oxide lifetimes of the screened and unscreened vendor E and vendor K devices at 150°C are depicted in Fig. 12. For vendor E devices, an abrupt change in field acceleration factors (slopes of the fitted lines) is observed at E_{ox} of ~ 9.4 MV/cm [Fig. 12 (a)]. In previous studies, it has been found that the Fowler-Nordheim (F-N) tunneling current rises continuously during high E_{ox} stress periods (> 9.4 MV/cm) due to hole generation in the gate oxide, which degrades the gate oxide lifetime, making $t_{63\%}$ decrease more rapidly as E_{ox} increases [13, 16]. The result indicates that high screening voltage is an important factor affecting the oxide intrinsic lifetimes of SiC MOSFETs.

Two types of screening conditions are selected for vendor E devices: E_{ox} of 9.9 MV/cm for 100 ms and E_{ox} of 9.9 MV/cm for 3 min. The $t_{63\%}$ of vendor E devices screened by E_{ox} of 9.9 MV/cm for 100 ms and 3 min are extracted and plotted in Fig. 12 (a). Less variation of gate oxide lifetimes can be observed for vendor E devices with 100 ms of screening and without screening. Therefore, it can be concluded that applying an oxide electric field of 9.9 MV/cm or less for 100 ms has no obvious damage to the gate oxide lifetimes of vendor E devices. However, TDDB measurement results on vendor E after screening E_{ox} of 9.9 MV/cm for 3 min demonstrate a notable degradation of oxide lifetimes. In addition, the predicted oxide lifetime at an operational condition (E_{ox}= 4 MV/cm) decreases by two orders of magnitude compared to the result on SiC MOSFETs without screening. These observations suggest that high gate voltage stress with long duration has the risk of damaging the intrinsic lifetime of the gate oxide because the hole generation is triggered and produces an enhanced F-N tunneling current [17], so it is not advisable to apply a high screening voltage for a long time.

TDDB results for vendor K devices at 150°C with three gate voltages are shown in Fig. 12 (b). Compared with the results for vendor E devices, vendor K devices with a trench gate structure maintain considerably longer oxide lifetimes at the same applied gate voltage. This result clearly demonstrates the advantage of the thicker gate oxide. The stress of 10.15 MV/cm for 1 s is selected as the screening condition for vendor K devices. Consequently, no noticeable degradation of gate oxide lifetimes for vendor K devices after the screening process is observed. To summarize, in terms of gate oxide lifetime, vendor K devices with thicker gate oxide can accept higher screening voltages and thereby achieve higher screening efficiency.



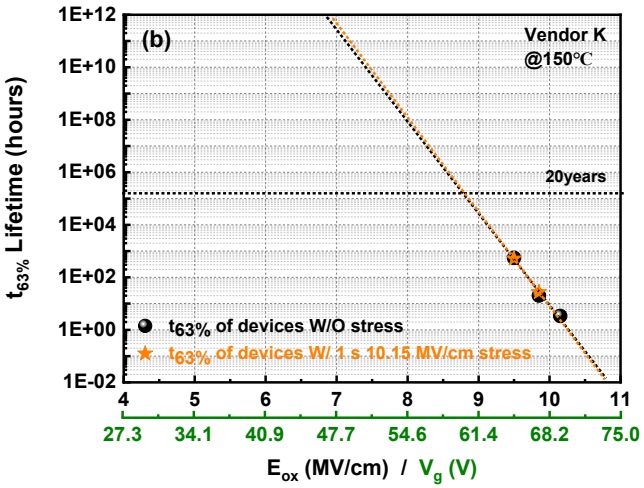


Figure 12. $t_{63\%}$ versus E_{ox} at 150°C for (a) vendor E devices, and (b) vendor K devices with and without high gate-voltage screening.

IV. Conclusions

In this paper, both threshold voltage and time-dependent dielectric breakdown measurements are performed on commercial 1.2 kV SiC MOSFETs with planar and trench gate structures to investigate the effects of high gate-voltage DC and pulse screening and burn-in. The V_{th} shift and recovery under different screening conditions for SiC MOSFETs are evaluated. For both structures, V_{th} shifts depend on the hole and electron trapping in the oxide. To avoid negative V_{th} shifts of SiC MOSFETs under high screening voltage conditions, it is recommended to keep screening voltage less than ~ 41 V (9 MV/cm) and ~ 54 V (8 MV/cm) for vendor E and K devices, respectively. In addition, a multi-pulse screening method is introduced to reduce the shift of threshold voltage during high-voltage screening, while compensating for the shortcoming of the burn-in technique that produces a large V_{th} shift. Furthermore, the fast high gate-voltage screening technology (100 ms, 9.9 MV/cm for vendor E and 1 s, 10.15 MV/cm for vendor K at 150°C) does not significantly degrade the gate oxide intrinsic lifetime during the screening process. The major advantage of SiC trench structure is that it allows higher screening voltages to reduce non-infant extrinsic failure probability as well as fulfill the long-term reliability requirements of the automotive market.

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