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Strain-insensitive intrinsically stretchable transistors and circuits

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Intrinsically stretchable electronics can form intimate interfaces with the human body, creating devices that could be used to monitor physiological signals without constraining movement. However, mechanical strain invariably leads to the degradation of the electronic properties of the devices. Here we show that strain-insensitive intrinsically stretchable transistor arrays can be created using an all-elastomer strain engineering approach, in which the patterned elastomer layers with tunable stiffnesses are incorporated into the transistor structure. By varying the cross-linking density of the elastomers, areas of increased local stiffness are introduced, reducing strain on the active regions of the devices. This approach can be readily incorporated into existing fabrication processes, and we use it to create arrays with a device density of 340 transistors cm^{-2} and a strain insensitivity of less than 5% performance variation when stretched to 100% strain. We also show that it can be used to fabricate strain-insensitive circuit elements, including NOR gates, ring oscillators and high-gain amplifiers for the stable monitoring of electrophysiological signals.

Recent breakthroughs in materials design and device fabrication have led to the development of electronic devices that are built entirely from intrinsically stretchable materials[1–7]. Such intrinsically stretchable electronics have tissue-like mechanical properties that can be used to seamlessly integrate devices with human skin[1,8–11]. Compared with stretchable electronics that are based on geometrically engineered rigid components[12–21], intrinsically stretchable electronics offer advantages such as high device density and good mechanical robustness and compliance[1,22]. However, polymer-based intrinsically stretchable electronics are designed without strain engineering; as a result, the applied strain is almost uniformly distributed over the entire electronic sheet[1,3,4]. Because the application of strain inevitably changes the device geometry, significant performance variations can occur. This limits the use of intrinsically stretchable electronics in the quantitative processing of physiological signals[1,3,23].

Based on Hooke's law and the series and parallel spring model, the strain distribution of a stretched substrate is affected by the stiffness of the localized regions[24–26], and thus, the stiffening of the active regions of the device in stretchable electronic sheets can be used to reduce the strain experienced by devices[24]. In particular, stretchable electronics can be built using rigid materials connected by stretchable interconnects (with strain on electronic devices less than 1%), where a thick layer of rigid, non-deformable material (for example, polyimide) can be added to increase the stiffness in the selected regions[12,15,16,27,28]. However, this approach has several disadvantages: the rigid materials are not intrinsically stretchable; the materials used are dissimilar to the substrate materials, making the development of mechanically stable interfaces under stretching challenging; the large modulus mismatch between the devices and the substrate causes significant strain concentration at the interface and can cause interconnect failure[12,29]; the rigid structure usually needs to be fabricated separately and subsequently transferred onto the substrate, which limits the production yield; and the rigid materials cannot achieve the simultaneous realization of high device density, mechanical stability and stretchability. An alternative approach is the local stiffening of the active regions of the device via engineering the elastomeric substrates[26,27,30–34]. However, the materials used so far (polydimethylsiloxane or polyurethane), as well as the patterning methods employed, are not compatible with the fabrication of state-of-the-art intrinsically stretchable electronics (Supplementary Table 1).

In this Article, we report an all-elastomer fabrication process to create strain-insensitive, intrinsically stretchable transistor arrays. In particular, we introduce patterned regions of mechanical heterogeneity (termed as elastiff layers) into the elastomer substrates by selectively varying the cross-linking density, implementing local stiffening and strain distribution to the active regions of the device. Because the elastiff layers are layers of transistor structures and are prepared by solution printing, this approach can be easily incorporated into an established fabrication process[1].

We use our patterned strain distribution technique to fabricate intrinsically stretchable transistor arrays with a device density of 340 transistors cm^{-2} (which is equivalent to the state-of-the-art

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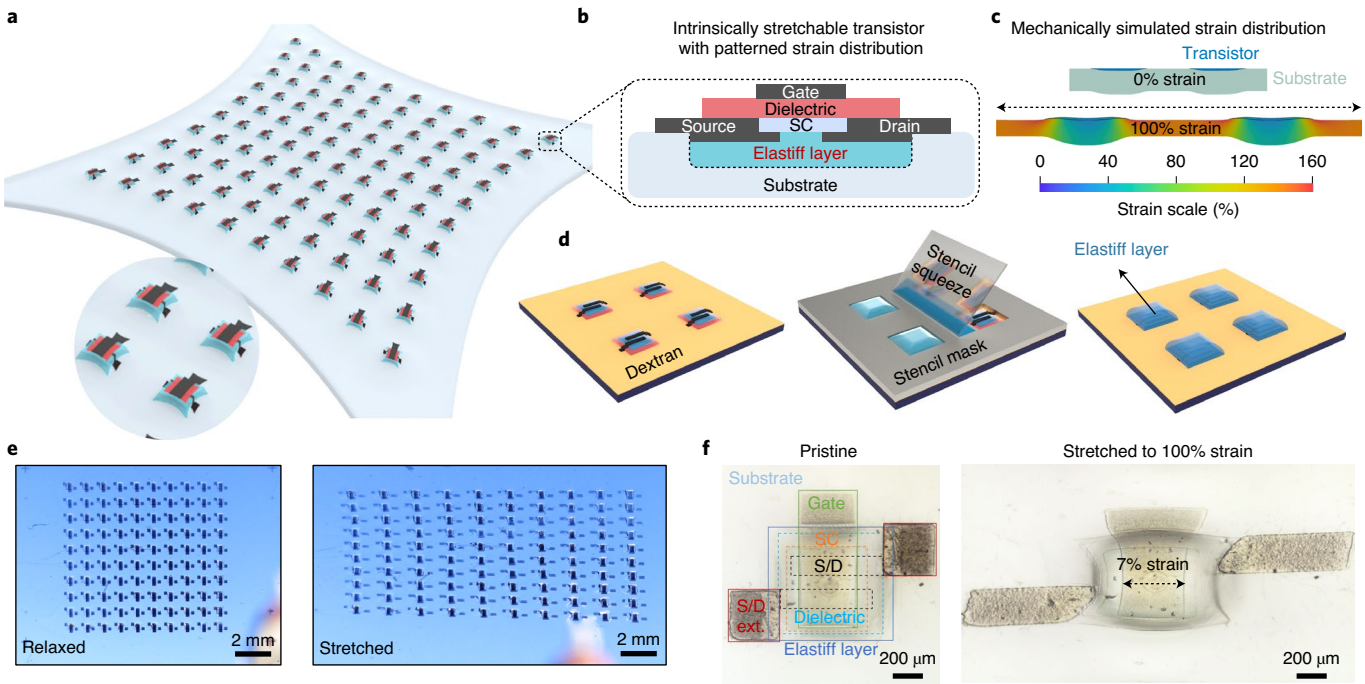

Fig. 1 | Strain-insensitive intrinsically stretchable transistor arrays with patterned strain distribution. a, Schematic of the strain-patterned stretchable transistor array under stretching. **b**, Two-dimensional diagram showing the representative transistor structure. **c**, Mechanical simulation showing the strain distribution of a strain-patterned transistor array (the ratio between the inter-device distance and device size is 1; elastiff layer thickness, 25 μm; device density, 51 transistors cm^{-2}) for stretching under 100% strain. **d**, Patterning of the elastiff layer by the stencil printing method in the overall fabrication flow of the transistor array (Supplementary Fig. 3). **e**, Photographs of a transistor array under the original (left) and stretched (right) states, clearly showing that deformation mostly occurs in the inter-device empty areas. **f**, Optical microscope images of one transistor in the array, under 0% (left) and 100% (right) global strain. Dielectric: azide-cross-linked H1052-SEBS, 1.2 μm thickness and 5.0 MPa modulus; elastiff layer: H1043 SEBS (rigid SEBS), 50 μm and 47.3 MPa modulus; substrate: H1221 SEBS (soft SEBS), 180 μm and 1.5 MPa modulus; SC: semiconductor fabricated via a conjugated-polymer/elastomer phase-separation-induced elasticity (termed CONPHINE) methodology[2,46], 80 nm thickness; S/D: CNT source and drain electrodes; gate: CNT gate electrode; S/D ext.: CNT/P3HT composite. Channel length, 80 μm; channel width, 320 μm; dielectric capacitance, 1.67 nF cm^{-2}.

technology[1]) and a strain insensitivity of less than 5% performance variation when stretched up to 100% strain. With this approach, the trade off between mechanical stability and device density can be adjusted for different electronic functions, and the wide range of materials choices can offer improved device performance. As a proof of concept, we demonstrate stable operation for intrinsically stretchable NOR gates and ring oscillators for up to 100% strain. Furthermore, we build strain-insensitive stretchable amplifiers with high gain (up to 25 for a single-stage amplifier and 120 for a two-stage amplifier) for a skin-like polymeric circuit that could amplify weak electrophysiological signals (down to a few millivolts).

Device design for patterned strain distribution

With the elastiff layers in an intrinsically stretchable transistor array, the strain is mainly experienced by the lower modulus interspace between the active devices (Fig. 1a,c and Supplementary Fig. 1). To experimentally implement the patterned strain distribution concept via the addition of the patterned elastiff layers (Fig. 1b), both the materials selection and the fabrication process for the elastiff layers need to be carefully considered.

The material of the elastiff layer needs to have the following attributes: (1) high stretchability (ideally >50% strain) such that the entire device can still be soft and stretchable, (2) significantly higher Young's modulus than the substrate (that is, at least over one order of magnitude) to minimize deformation in the active regions of the devices[27], and (3) strong adhesion with the substrate material to endure large shearing stresses generated by the substantial in-plane strain differences across the interface[28,29,35]. To simultaneously fulfil all these requirements, it would be ideal to choose both the elastiff and substrate materials from the same family of elastomers with various cross-linking densities to achieve vastly different mechanical properties, while sharing similar chemical compositions for strong interfacial interactions. In this work, with the styrene–ethylene–butylene–styrene (SEBS) family chosen as the elastomeric substrate, the modulus difference between the elastiff layer and the substrate is realized by varying the percentage of the polystyrene block that serves as the physical cross-linking areas. We adopt the most rigid version (termed as rigid SEBS, consisting of 67 vol% polystyrene) as the elastiff layer, and the softest version (termed as soft SEBS, consisting of 12 vol% polystyrene) as the substrate, and therefore, the modulus difference is 32 times (Supplementary Fig. 2).

The patterning process for the elastiff layer also needs to be integrated into existing fabrication processes for intrinsically stretchable transistor arrays. Preferably, this process should be performed after the fabrication of the dielectric, semiconductor and source/drain layers on the rigid Si/SiO_2 substrate, but before the lift-off process to the SEBS substrate for the gate layer (Fig. 1d). To ensure process reliability and compatibility, we adopted the stencil printing[12,36] method to pattern the SEBS elastiff layer on top of the targeted transistors. This one-step method has a relatively high printing resolution of around 100 μm (Supplementary Fig. 3). We note that one of the key parameters is the choice of the octane/hexane co-solvent for the SEBS printing ink to provide orthogonality with the fabricated device components[37] and high printing resolution[38] from its high viscosity. The entire fabrication flow for the intrinsically

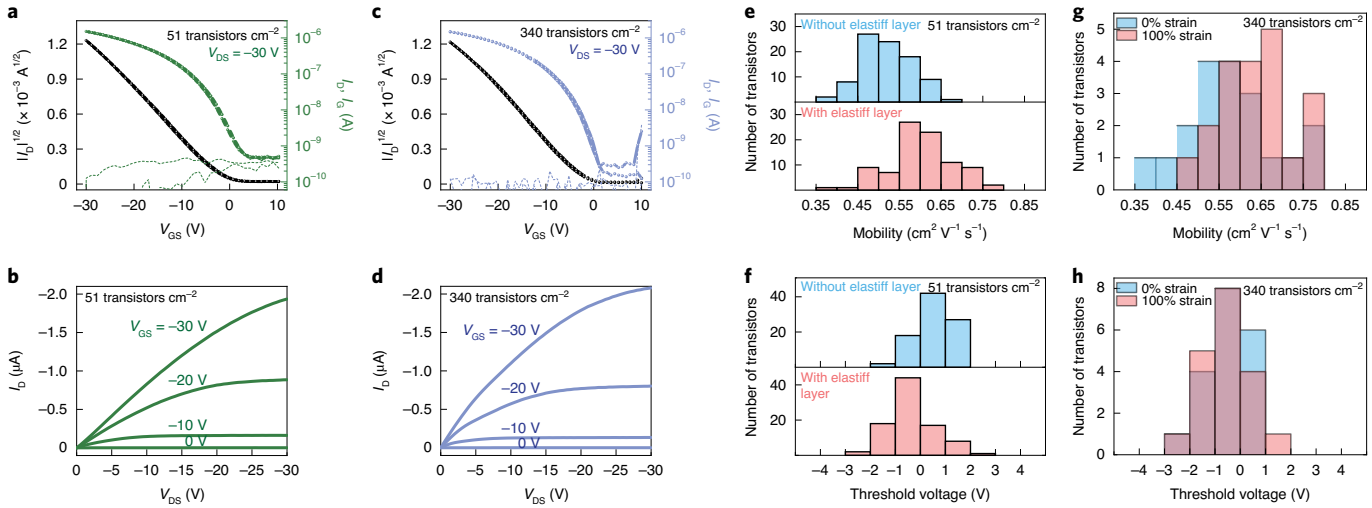

Fig. 2 | Performance uniformity of intrinsically stretchable transistor arrays with patterned strain distribution. a,**b**, Typical transfer (**a**) and output (**b**) characteristics from the transistor array with a density of 51 transistors cm^{-2}. **c**,**d**, Typical transfer (**c**) and output (**d**) characteristics from the transistor array with a density of 340 transistors cm^{-2}. In **a** and **c**, the black curve shows the square root of the drain current. **e**,**f**, Histograms showing the mobility (**e**) and the threshold voltage (**f**) from the working transistors in a 100-transistor array (with a density of 51 transistors cm^{-2}), with the comparison showing the influence of adding the elastiff layer for the strain patterning. **g**,**h**, Histograms showing the mobility (**g**) and the threshold voltage (**h**) from the working transistors in a 100-transistor array (with a density of 340 transistors cm^{-2}), with the comparison showing the influence of strain. For the array with 51 transistors cm^{-2}, the channel length and width are 80 μm and 320 μm, respectively; for the array with 340 transistors cm^{-2}, the channel length and width are 70 μm and 280 μm, respectively. I_D, drain current, represented by solid lines; I_G, gate current, represented by dashed lines; V_{GS}, the gate–source voltage; V_{DS}, the drain–source voltage.

stretchable transistor array with patterned strain distribution is shown in Supplementary Fig. 4.

Indeed, when a large global strain (for example, 100%) was applied to the transistor array with the elastiff layer, the active devices experienced only a small local strain (~10%, which is termed as the strain on device), as confirmed through both mechanical simulations (Fig. 1c; details are available in the Methods) and experimental results (Fig. 1e,f). Our obtained simulation results also suggested that the strain on device could get even smaller by decreasing the transistor density in the array (that is, a decrease in the ratio of the transistor size to the inter-device distance; details are shown in Fig. 4) and vice versa. Owing to the broad tunability of the elastiff layer with regard to its thickness and modulus, the transistor array could maintain a high density of up to 340 transistors cm^{-2} (Supplementary Fig. 5), with the strain on device still less than 10% under 100% global strain. This density is the same as the previously reported highest density for an intrinsically stretchable transistor array[1]. Notably, this device density is at least two orders of magnitude higher than the densities reported in 'rigid-island' stretchable electronics[12,13,15]. In addition, due to the strong adhesion between the elastiff and substrate layers, no delamination or wrinkle formation were observed under stretching (Fig. 1f). The intrinsic softness of the designed strain-patterned platform also promises good skin conformability during the movement of the human body (Supplementary Figs. 6 and 7).

Device electrical performance characterization

To investigate if the addition of the elastiff layer has any negative impact on the initial transistor performance, we measured the individual devices from the arrays with and without the patterned strain distribution. Here two different device densities are used to show the scaling down of the array dimensions without negatively influencing the electrical performance. Given the compatibility of the materials selection and the reliability of the patterning process, our strain-patterned transistor arrays afforded a high yield of up to 91% and typically above 85% for ten batches of fabricated devices, which are similar to the non-strain-patterned ones (up to 90% yield). A representative transistor in the array shows ideal transfer and output behaviours with an on/off ratio above 10^3, the leakage currents are in orders of magnitude lower than the on currents, negligible hysteresis and no observable electrode–semiconductor contact issues (Fig. 2a–d). Both the strain-patterned and non-strain-patterned transistor arrays have similar uniform distribution of charge carrier mobility (0.62 ± 0.08 cm^2 (V s)$^{-1}$ from the strain-patterned array versus 0.51 ± 0.06 cm^2 (V s)$^{-1}$ from the non-strain-patterned array) and threshold voltage (Fig. 2e,f and Supplementary Fig. 8). The minor difference is well within the normal batch-to-batch fluctuations.

Next we show that the patterned strain distribution design leads to the improved stability of the transistor electrical performance under strain. When the transistors in the non-strain-patterned array were stretched in both parallel (Fig. 3a,c) and perpendicular (Fig. 3d and Supplementary Fig. 9) directions with respect to the channel, substantial changes were observed in their transfer behaviours, that is, both on currents and mobilities. These strain-induced performance changes result from a combination of changes in the device geometry (including the channel length, channel width and dielectric thickness) and variations in the semiconductor mobility and electrode–semiconductor contacts. On the contrary, when the transistor array with the elastiff layer was tested under strain, the strain-induced performance instability was significantly suppressed (Fig. 3b–d and Supplementary Fig. 9) as a result of the minimized strain experienced by the active regions of the device. The detailed distributions of the mobility and threshold voltage did not appear to have been altered much (Fig. 2g,h). The device density shown here is the same as the present state-of-the-art value (340 transistors cm^{-2}) for intrinsically stretchable electronics. Furthermore, the devices can maintain their original performance even after 1,000 stretching cycles under 100% strain (Fig. 3e,f). Our strain distribution patterning method even allows the transistor performance to be maintained under a global strain as high as 400% (Supplementary Fig. 10).

Tunable balance between device stability and density

Intrinsically stretchable electronics, in contrast to conventional electronics, should be designed to provide the desired electronic

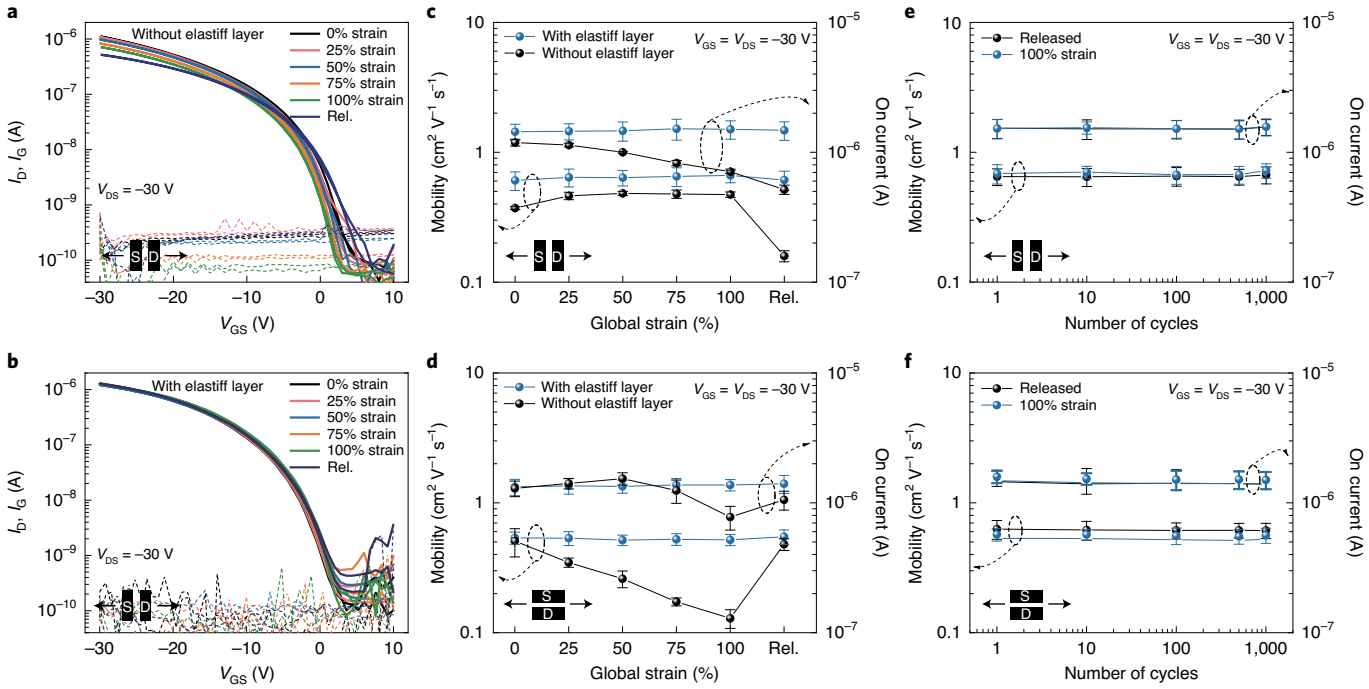

Fig. 3 | Electrical performance of the transistor array under global strain of up to 100%. a,**b**, Transfer characteristics during a stretching cycle in parallel to the channel direction of a representative transistor from transistor arrays without (**a**) and with (**b**) the elastiff layer. The same transistor is monitored during the stretching cycle. **c**,**d**, Mobility and on current averaged from ten representative transistors during a stretching cycle in parallel (**c**) and perpendicular (**d**) to the channel direction. **e**,**f**, Mobility and on current averaged from ten representative transistors during 1,000 repeated stretching cycles to 100% strain, where the strain is parallel (**e**) and perpendicular (**f**) to the channel direction. Device density, 340 transistors cm^{-2}; channel length and width, 70 μm and 280 μm, respectively; elastiff layer thickness, 50 μm. S, source; D, drain; Rel., released. Error bars represent standard deviations.

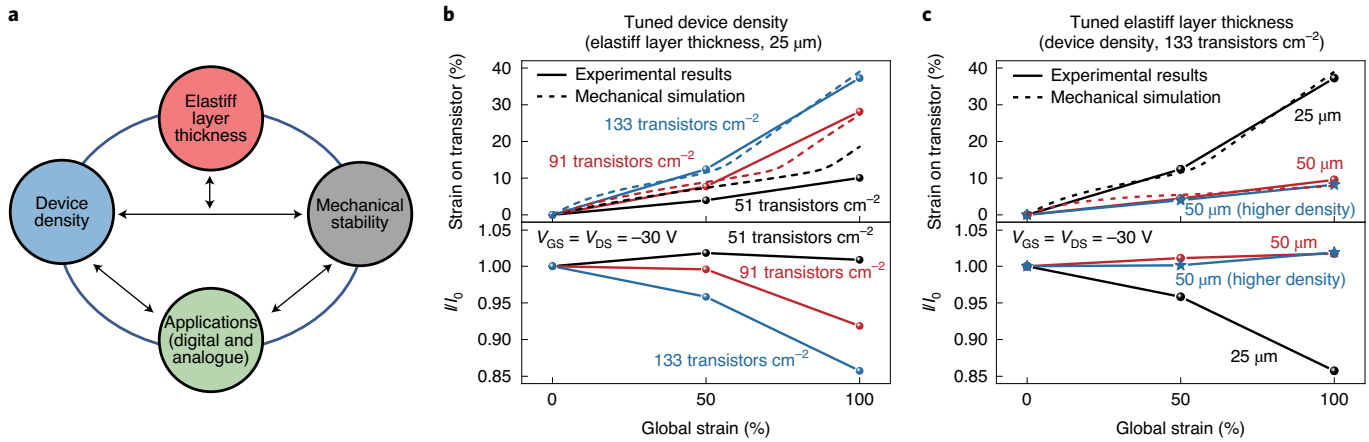

Fig. 4 | Tunable mechanical stability and device density. a, Schematic showing the design concept for strain-insensitive intrinsically stretchable electronics, where the strain-patterning concept can be used to design device structures to meet mechanical, geometric and electrical requirements. **b**, Top: experimental (solid lines) and simulation (dashed lines) results of the strain on device from the transistor arrays with different device densities of 51, 91 and 133 transistors cm^{-2}. Bottom: the corresponding changes in the on current from the transistors in the top panel. They share the same elastiff layer with a Young's modulus of 47.3 MPa and thickness of 25 μm. **c**, Top: experimental (solid lines) and simulation (dashed lines) results of the strain on device from transistor arrays with the device density of 133 transistors cm^{-2} but different elastiff layer thicknesses of 25 μm and 50 μm. Bottom: the corresponding changes in the on current from the transistors in the top panel. Blue lines refer to the array with a density of 340 transistors cm^{-2} and the same inter-device distance/device size (0.25) as the array with a density of 133 transistors cm^{-2}. I/I_0 represents the ratio change of drain current during stretching. All the experimental strains on device and on currents are acquired by averaging from ten representative transistors.

functionalities (as highly related to the device density) and to realize necessary mechanical stability based on needs. Our described design for strain distribution patterning enables finding the optimal balance between these two performance metrics as per the requirements of specific applications (Fig. 4a). As evidenced by both experimental and simulation results (Fig. 4b), reduced strains on device can be achieved by increasing the ratio of the inter-device spaces under the corresponding device densities of 133, 91 and 51

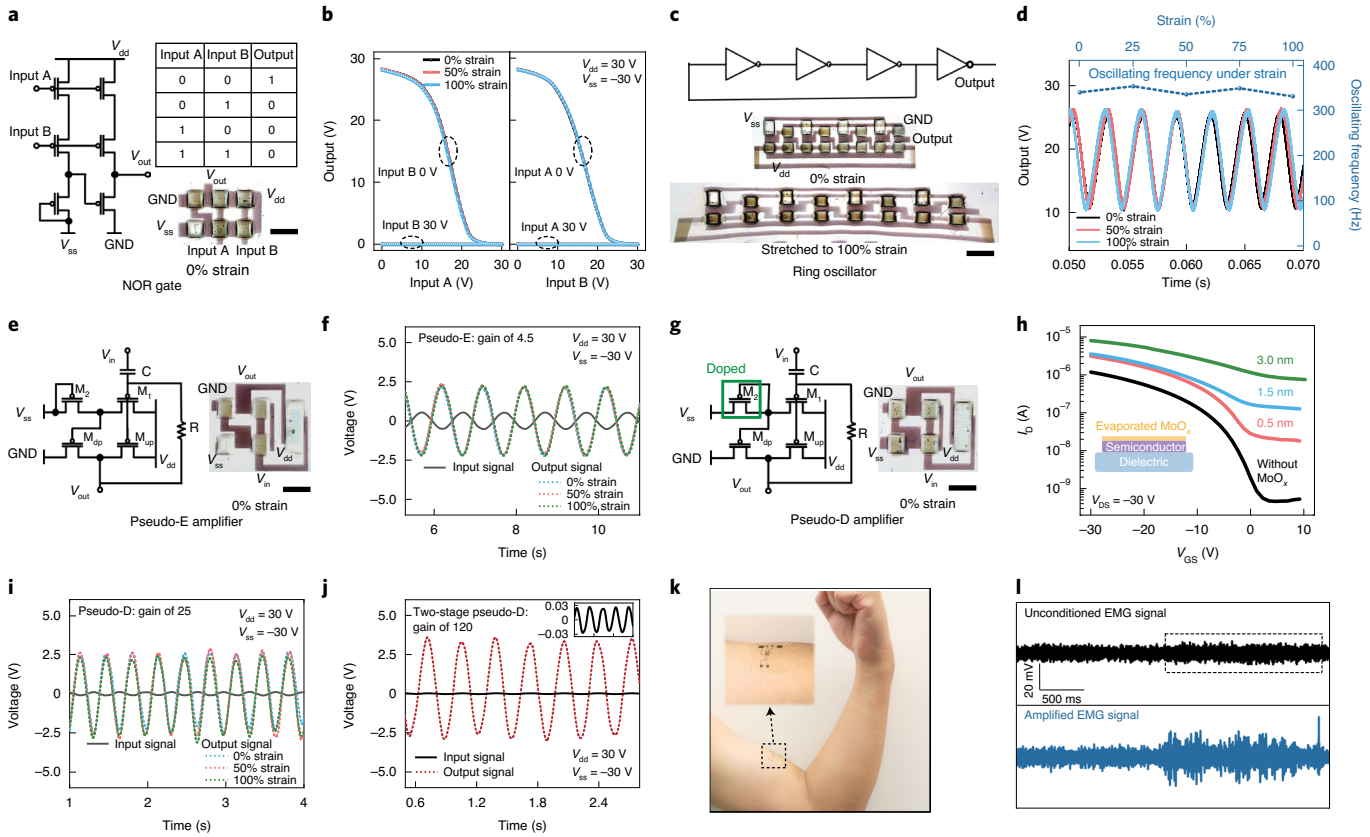

Fig. 5 | Strain-insensitive digital and analogue circuits for human electrophysiological signal conditioning. a, Circuit diagram and truth table of a NOR gate. **b**, Transfer characteristics of the stretchable NOR gate under strain. **c**, Circuit diagram and optical images of a three-stage stretchable ring oscillator. **d**, Output signals and oscillating frequency of the stretchable ring oscillator when stretched. **e**, Circuit diagram of a pseudo-E amplifier. M_2 transistor has a channel width of 80 μm; M_1, M_{up} and M_{dp} have a channel width of 1,440 μm. **f**, Input sinusoidal signal (1 Hz; amplitude, 0.5 V) along with the strain-insensitive output signal from the pseudo-E amplifier with the gain of ~4.5. **g**, Circuit diagram of a pseudo-D amplifier. M_1 transistor has a channel width of 400 μm; M_2, M_{up} and M_{dp} have a channel width of 1,440 μm. **h**, Representative transfer characteristics of an MoO_x-doped strain-patterned transistor array. **i**, Input sinusoidal signal (3 Hz; amplitude, 0.1 V) along with the strain-insensitive output signal from the pseudo-D amplifier, showing a stable gain of 25. **j**, Input sinusoidal signal (3 Hz; amplitude, 0.025 V) along with the output signal from a two-stage pseudo-D amplifier with a gain of ~120. **k**, Photograph showing a stretchable pseudo-D amplifier conformably attached on the human biceps for the amplification of EMG signals. **l**, EMG signals before (top) and after (bottom) amplification by the stretchable pseudo-D amplifier. Channel length for all the transistors is 80 μm. For the inverters in the NOR gate and ring oscillator, the loading transistor has a channel width of 120 μm, and the other transistors have a channel width of 1,680 μm. For the amplifiers, a non-gated transistor is used as the resistor R (~10^8 Ω) and C is the input capacitor (1 μF). V_{dd} (30 V) and V_{ss} (−30 V) are the direct-current voltages applied to the electrodes as the power source; V_{in}, input signal; V_{out}, output signal; GND, ground. Scale bars (**a**,**c**,**e**,**g**), 1.5 mm.

transistors cm^{-2} (with the corresponding inter-device distance/device size equal to 0.25, 0.50 and 1.00, respectively). Thus, improvement in the mechanical stability of the electronic performance can be obtained by reducing the device density (Fig. 4b). For practical electronic applications, a combination of high mechanical stability and low device density is generally more applicable for analogue circuits that directly interface with sensors. On the contrary, a higher density of devices is required to improve the performance of digital circuits, but they are more tolerant to the applied strain[1,4].

Since the stiffness of the elastiff layer can be controlled through the layer thickness and modulus, such a demonstrated trade off between the device density and mechanical stability can be further mitigated for satisfying specific applications that have demanding requirements with regard to both these criteria (Fig. 4a). For instance, at a device density of 133 transistors cm^{-2}, a further increase in the elastiff layer thickness from 25 to 50 μm (Supplementary Fig. 11) can reduce the strain on device by almost fourfold (39% versus 10% of the local strain) at a 100% global strain, leading to improved electrical performance stability (Fig. 4c). However, this will also require the interconnects between the devices to sustain higher strain under the same array layout, which could be as high as 400% at the edges of the elastiff layers. This subsequently reduces their overall operational strain range (Supplementary Fig. 12). On the other hand, a transistor array with scaled-down dimensions (340 transistors cm^{-2}) can behave similarly as the array with a density of 133 transistors cm^{-2} in terms of mechanical stability (Fig. 4c). This is because the ratio between the inter-device distance and device size of these two arrays with different densities is the same.

Strain-insensitive analogue and digital circuits

Since the transistor array with patterned strain distribution could function stably under large mechanical deformation, realizing integrated circuits that can provide unaltered quantitative signal processing under strain is now possible. To demonstrate digital circuit functions, we first fabricated a pseudo-complementary metal–oxide–semiconductor (CMOS)[39] NOR gate consisting of six transistors (Fig. 5a) as a 'universal gate' to form all the other logic gates. With our strain-patterning design, the transfer characteristics and logic computation of the NOR gate were kept unchanged till 100% strain (Fig. 5b). Moreover, a strain-insensitive ring oscillator that consists

of 16 transistors (Fig. 5c) was also realized. When stretched to 100% strain, the strain-patterned ring oscillator showed a stable (less than 3% variation) oscillating frequency of ~330 Hz (Fig. 5d). This demonstrates the applicability of our design towards realizing circuits with higher complexity. Next we show the strain-insensitivity benefit of our method in analogue circuits, whose electrical performance is more sensitive to the experienced strain[1]. We first built a pseudo-CMOS E-type (pseudo-E; Fig. 5e) stretchable amplifier and showed that its gain could be maintained at ~4.5 even up to 100% strain (Fig. 5f and Supplementary Fig. 13). To further improve the amplification factor, our patterned strain distribution design could incorporate materials/modifications with limited stretchability to the transistors to enhance the circuit performance. For example, the pseudo-CMOS D-type (pseudo-D; Fig. 5g) architecture of the amplifier design is known to have a higher gain than the pseudo-E design[39,40]. However, this has not yet been achieved by intrinsically stretchable transistors, because it was not possible to attain a high enough current under a zero V_{GS} load[1,23,41] (marked as M_2 in Fig. 5g) to satisfy the requirement of the pseudo-D design (Supplementary Fig. 14). However, with our strain-patterning design, we can now use a less-stretchable small-molecule doping method (for example, thermal evaporation of MoO_x onto the channel) to modify the semiconductor layer in the M_2 transistor for an increased zero V_{GS} current[42–44]. As shown in Fig. 5h, when ~3 nm MoO_x layer was deposited, the zero V_{GS} current increased by almost three orders of magnitude. Using this MoO_x-modified strain-patterned transistor, we were able to achieve the first strain-insensitive (up to 100%; Fig. 5i and Supplementary Fig. 13) intrinsically stretchable pseudo-D amplifier with a gain of ~25, which was also shown to be stable both over the constant biasing (Supplementary Fig. 15) and long-term storage in an inert atmosphere (Supplementary Fig. 16). In comparison, without the elastiff layer to protect the MoO_x-doped transistor, the gain value decreased significantly even under 20% strain (Supplementary Fig. 17).

With improved amplification and mechanical stability, we proceed to demonstrate the utility of our stretchable amplifier for the quantitative conditioning of electrophysiological signals. In particular, both the substantially boosted gain and strain insensitivity are important to the processing of weak electrophysiological signals (down to several millivolts) with minimal interference from skin or tissue deformation. Here this capability is demonstrated on electromyography (EMG), an important diagnostic procedure to assess the health of muscles and the associated motor neurons and neuromuscular junctions[45]. The photograph shown in Fig. 5k indicates the good skin conformability of the stretchable amplifier on human biceps. In the absence of an amplifier, the EMG signal generated during muscle contraction was dominated by background noises with sporadic spikes (Fig. 5l). However, when our stretchable amplifier was connected, significantly stronger EMG signals could be recorded with approximately seven times higher amplitudes. For cases when even higher amplification is needed, connecting two such amplifiers in series was observed to provide an overall gain greater than 120 (Fig. 5j). This high level of gain can also benefit analogue-to-digital conversion by reducing the minimum required digital resolution, allowing the combination of analogue signal processing and digital computation within an intrinsically stretchable system.

Conclusions

We have reported strain-insensitive, intrinsically stretchable transistor arrays and circuits that are created using an all-elastomer process for applying local stiffening. Using this approach, we resolved two previous limitations in the state-of-the-art stretchable transistors and circuits: electrical performance limited by strain and relatively low circuit performance. We demonstrated the stable operation of multiple types of circuit—from digital to analogue—under large strain. These circuits included NOR gates, ring oscillators and amplifiers, with intrinsically stretchable amplifiers exhibiting high gain and the capability of recording weak electrophysiological signals. By modulating the composition of our intrinsically stretchable electronics, the trade off between electronic functionality and mechanical stability can be adjusted according to specific application requirements. Furthermore, this strain-insensitive design broadens the materials choices and thus could offer further enhancements in the performance of intrinsically stretchable electronics. Our approach achieves all the desirable parameters for wearable electronics, including high device density, advanced electronic functionalities, high stretchability and strain insensitivity, and it could play a valuable role in the advancement of intrinsically stretchable electronics.

Methods

Materials. All the processing solvents, such as chlorobenzene, toluene, dodecane, octane, hexane, chloroform and ethoxynonafluorobutane, were purchased from commercial sources and used as received. The polymer semiconductor poly[2,5-bis(7-decylnonadecyl)pyrrolo[3,4-c]pyrrole-1,4-(2H,5H)-dione-(E)-(1,2-bis(5-(thiophen-2-yl)selenophen-2-yl)ethene)] (P-29-DPPDTSE) was synthesized via a reported method[46]. The molecular weight of the polymer semiconductor is (M_n) 34.0 kDa and (M_w) 72.3 kDa and the polydispersity index is 2.13. The azide cross-linker of bis(6-((4-azido-2,3,5,6-tetrafluorobenzoyl)oxy) hexyl) decanedioate was synthesized using a method we reported before[1]. Soft SEBS (H1221) with a volume fraction of poly(ethylene-co-butylene) of 88%, H1052 with a volume fraction of poly(ethylene-co-butylene) of 80% and rigid SEBS H1043 with a volume fraction of poly(ethylene-co-butylene) of 33% were provided by Asahi Kasei. SEBS H1052 was used as the stretchable dielectric layer, rigid SEBS was used as the elastiff layer and soft SEBS was used in the CONPHINE semiconductor[2] and as the stretchable substrate in the intrinsically stretchable transistor array. Dextran and octadecyltrimethoxysilane were purchased from Sigma-Aldrich and used as received. Carbon nanotubes (CNTs) for the electrodes were purchased from Carbon Solutions (P3-SWNTs and P2-SWNTs). Poly(3-hexylthiophene-2,5-diyl) (P3HT) was provided by BASF (Sepiolid P200).

Fabrication of intrinsically stretchable transistor array with strain distribution patterning method. As the substrate for the fabrication process, a SiO_2/Si wafer was first cleaned with oxygen plasma (150 W, 200 mtorr) for 2 min and then sonicated in acetone, 2-propanol and deionized water for 5 min each. Dextran (10 wt%) was dissolved in water and spin coated on top of the cleaned Si/SiO_2 wafer at 1,500 r.p.m. for 18 s, followed by baking on a hot plate at 80 °C for 1 min and 180 °C for 30 min, to form a 300-nm-thick water-soluble sacrificial layer. SEBS (H1052) (60 mg ml^{-1}) was dissolved in toluene and stirred on a 70 °C hot plate overnight. Then, an SEBS solution with azide cross-linker (2.0 mg ml^{-1}) was spin coated on top of dextran at 1,000 r.p.m. to form the stretchable dielectric with a thickness of ~1.2 µm. To photo-pattern the dielectric layer, the film was selectively exposed under deep ultraviolet light (wavelength, 254 nm; Spectrum 1000 Precision UV Spot Curing System from American Ultraviolet) by a mask for 5 min at a dose of ~540 mJ cm^{-2}. The cross-linking reaction was initiated in the exposed areas. Next soft baking was performed at 120 °C for 15 min in air to further increase the cross-linking density. After that, a development process was performed in dodecane for 45 s to remove the unexposed parts, followed by final baking at 200 °C for 1 h in a glovebox. To promote the desirable phase separation morphology of the CONPHINE semiconductor, the surface of the patterned dielectric was modified with octadecyltrimethoxysilane molecules. The modification processes are as follows: O_2 plasma treatment for 30 s (150 W, 200 mtorr); spin coating of the octadecyltrimethoxysilane (OTS) solution (3 mM in hexane) at 3,000 r.p.m. for 2 min; and finally, vapour annealing in a desiccator with a small vial containing a few millilitres of ammonium hydroxide solution (28–30% in water) for 10 h at room temperature. Next the CONPHINE semiconductor solution (P-29-DPPDTSE:SEBS-H1221 solution, 10 mg ml^{-1} in chlorobenzene, at a volume ratio of 3:7) was spin coated on the top at 1,000 r.p.m., followed by annealing at 150 °C on a hot plate in a glovebox, to form the stretchable semiconductor. To pattern the semiconductor, a fluorinated layer (3M Novec 1902 Electronic Grade Coating diluted by ethoxynonafluorobutane in a volume ratio of 1:2) was first deposited on top by spin coating at 1,000 r.p.m. Then a Cu etching mask (120 nm) was thermally evaporated on top through a shadow mask aligned with the previous layers. The CONPHINE semiconductor not covered by Cu was then etched away by O_2 plasma etching (150 W, 200 mtorr). Then the Cu film was lifted off by soaking the device in ethoxynonafluorobutane to dissolve the fluorinated layer, giving a patterned CONPHINE semiconductor layer. The top source/drain electrodes were patterned by spray coating the CNT solution through a shadow mask. The CNT solution was prepared by dispersing 100 mg P3-SWNT in 350 ml 2-propanol with 1 ml water through consecutive 6 h bath sonication, followed by 20 min tip sonication and then centrifugation at

6,000 r.p.m. for 30 min. After depositing the source/drain electrodes, the rigid SEBS (H1043) solution in an octane/hexane co-solvent (160 mg ml^{-1} at a volume ratio of 3:1) was stencil printed through a shadow mask that was aligned with the previous components, forming the patterned elastiff layer for each transistor, which was about 25 µm in thickness. To fabricate a thicker elastiff layer (50 µm), the solution was coated twice through the shadow mask. The second layer was coated after the drying of the first layer at 45 °C for 5 min in air. Subsequently, the SEBS (H1221) stretchable substrate (180 µm) was conformably laminated on top, and the device was then baked in a glovebox at 70 °C for 30 min to increase the adhesion between the substrate and elastiff layer. In the next step of fabrication, the whole device was soaked in water to dissolve the dextran sacrificial layer and transfer all the components onto the substrate. Finally, two different CNT dispersions (2-propanol/water-dispersed P3-SWNT and chloroform-dispersed P2-SWNT/P3HT composite) were spray coated through a mask for patterning the gate electrodes on the dielectric SEBS and interconnect electrode crossing from the elastiff layer to the substrate, respectively. As the strain concentrated near the edge of the high-modulus elastiff layer, chloroform was selected so that it slightly dissolved the SEBS to cause the inter-diffusion of CNTs to increase the stretchability of the electrodes. This CNT solution was prepared by dispersing 80 mg P3-SWNT and 20 mg P3HT in 350 ml chloroform via 30 min tip sonication and then centrifuging at 8,000 r.p.m. for 30 min. After going through the entire process flow, the fabricated strain-patterned transistor array was baked at 80 °C in a vacuum heater for 4 h to fully remove any moisture before electrical characterization. All the alignments of the shadow masks in the fabrication process were performed under an optical microscope.

Mechanical properties' characterizations. All the mechanical strain–stress tests were performed by using an Instron 5565 instrument. Different types of SEBS were dissolved in the same solvent as used in the fabrication process of the strain-patterned transistor array (H1043 SEBS, 100 mg ml^{-1} in an octane:hexane = 3:1 co-solvent; H1221 SEBS, 100 mg ml^{-1} in toluene). The solutions were drop casted in the ambient environment and dried overnight. The thickness of the drop-casted films is around 0.15 mm, which is characterized by a Vernier calliper. All the samples were baked in vacuum at 100 °C for 1 h before performing the test. The stretching rate was 10% s^{-1}.

Electrical characterizations. All the electrical characterizations of the transistors and circuits were performed in the ambient environment on a probe station connected to a Keithley 4200 parameter analyser. For the circuits' characterizations (NOR gates, ring oscillators and amplifiers), a commercial buffer (LF412C Operational Amplifiers, Texas Instruments) was used. The buffer was connected between the output terminal of the stretchable circuits and the oscilloscope. A function generator and an oscilloscope were used to provide the input and collect the output signals, respectively. For the electrical characterization of all the circuits during the stretching cycle, the same equipment is used.

Strain-on-device measurements. All the strain-on-device measurements were performed using an optical microscope.

Human EMG signals' conditioning. All the external cables used for the connections were low-noise triaxial cables purchased from Keithley. Commercial gel electrodes (Syrtenty TENS Unit Electrodes Pads) were used for collecting the EMG signals. Two gel electrodes were attached on the human biceps. To acquire the original EMG signal, the output side of the electrodes was directly connected to an oscilloscope. To obtain the amplified EMG signal, the output side of the electrodes was connected to the input and ground terminal of the pseudo-D amplifier, respectively. During the measurement, Keithley 4200 was the power supply for both the amplifier and the buffer, and all the components were grounded together to reduce noise. The biceps shown in Fig. 5 is that of W. Wang, who has given his consent to publish the image.

Mechanical simulation. For the mechanical simulation, a research finite element simulation software based on the open-source finite element library called 'deal. II' (ref. [47]) was used. For the finite element model, three-dimensional eight-noded hex elements were used. The experimentally measured profiles were post processed to obtain an averaged elastiff layer geometry (Supplementary Fig. 18). The substrate layer geometry was obtained by a custom Python (version 3.6.9) script in combination with the adaptive refinement capability of the finite element software. The usage of the finite deformation material models was necessitated owing to the high strains experienced by both layers. We used the Yeoh model[48] to describe the hyperelastic response of the substrate. A Yeoh hyperelastic material follows the stress–strain relationship given by

$$\sigma = -pI + 2\sum_{i=1}^{3} iC_i(I_1 - 3)^{i-1}b$$

where σ is the stress tensor, p is the hydrostatic pressure used to enforce incompressibility, I is the identity tensor, I_1 is the first invariant of the deformation tensor and b is the left Cauchy–Green tensor. The calibrated parameters for the substrate using uniaxial experimental data (Supplementary Fig. 21a) are as follows: $C_1 = 0.2285$ MPa, $C_2 = -0.008$ MPa, and $C_3 = 0.0002388$ MPa.

Due to the high stiffness of the elastiff layer, the contribution of the semiconductor, dielectric and electrode were assumed to be insignificant for modelling purposes, and the behaviour of a typical elastiff layer–substrate system is studied. The finite deformation elastoplastic model[49] was used for the elastiff layer material and it has the following free energy expression:

$$\psi(\varepsilon_A^e, \alpha) = \frac{\kappa}{2}\left[\sum_{A=1}^{3}\varepsilon_A^e\right]^2 + \mu\left[\sum_{A=1}^{3}\left(\tilde{\varepsilon}_A^e\right)^2\right] + \frac{1}{2}H\alpha^2$$

where ε_A^e are the principal Hencky strains, $\tilde{\varepsilon}_A^e$ are their isochoric parts, α is the amount of isotropic hardening in the material, κ is the bulk modulus, μ is the shear modulus and H is the linear isotropic hardening coefficient. The principal stresses are given by

$$\tau_A = \frac{\partial\psi}{\partial\varepsilon_A^e}$$

The driving force of the plastic hardening is given by

$$\beta = \frac{\partial\psi}{\partial\alpha}$$

The yield function is defined as

$$\phi(\tilde{\tau}_A, \beta) = \sqrt{\sum_{A=1}^{3}(\tilde{\tau}_A)^2} - \sqrt{\frac{2}{3}}(y + \beta) \leq 0$$

where $\tilde{\tau}_A$ represents the isochoric part of the principal stresses and y is the yield stress of the material. The flow rule is given by

$$\dot{\alpha} = -\lambda\frac{\partial\phi}{\partial\beta}$$

where λ is the Lagrange multiplier that describes the rate of plastic deformation; along with ϕ, it satisfies the loading/unloading conditions, also known as the Karush–Kuhn–Tucker conditions. The calibrated elastoplastic parameters are as follows: $E = 56$ MPa, $\nu = 0.4$, $y = 7$ MPa and $H = 2.0$.

Here E is the elasticity modulus and ν is the Poisson's ratio. The above parameters were obtained by fitting the models to the optimal experimental data for the simulations, as shown in Supplementary Fig. 21. Assuming a large transistor array, the symmetric boundary conditions were applied by considering a typical central element, as shown in Supplementary Fig. 22. A displacement loading was applied along the longitudinal direction while constraining both the lateral faces to remain flat. The engineering strains were measured between two points that were approximately 0.35 mm apart along the loading direction in the reference configuration, situated at the top of the elastiff layer, as shown in Supplementary Fig. 23. As both materials had a time-independent behaviour, an arbitrary time step of 0.02 was used and the 100% global strain is applied in 50 equal steps.

The simulations allowed us to carefully analyse the strain distribution within both the substrate and the elastiff layer. Along the loading direction, the majority of the strain was taken by the substrate, while the elastiff layer took a comparatively smaller strain. Due to the modulus difference, there was a strain concentration at the interface between the substrate and the elastiff layer. The simulation results (Supplementary Fig. 19) showed that the amount of strain concentration increased if the stiffness ratio between the elastiff layer and substrate increased. The modulus ratio of the strain-patterned transistor array was ~32. Furthermore, Supplementary Fig. 20 shows the local strain along a horizontal line.

For the cases of high transistor densities and low elastiff layer thicknesses, the steep increase in the local strains compared with the global strains could be attributed to the yielding of the elastiff layer, captured by the elastoplastic material model. Although the elastiff layer initially had a perfectly elastic response, it showed a curved response at the initial stages because of the slight softening of the substrate material as illustrated by its material curve (Supplementary Fig. 21).

Testing the devices on human biceps. The tests of the devices on human biceps described herein do not need Institutional Review Board approval, because our experiments do not affect living people physically or physiologically, and we have not sought or received identifiable private information.

Reporting Summary. Further information on research design is available in the Nature Research Reporting Summary linked to this article.

Data availability

The data that support the plots within this paper and the other findings of this study are available from the corresponding authors upon reasonable request.

Code availability

The code that supports the results within this paper and the other findings of this study are available from the corresponding authors upon reasonable request.

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Author contributions

S.W., W.W. and Z.B. designed the project and experiments. W.W. and S.W. fabricated the intrinsically stretchable transistor array and circuits and carried out the electrical characterizations. S.N. helped with the circuits design and measurements. R.R., P.K.A. and C.L. carried out the mechanical simulations. Y.O. and Y.Z. synthesized the azide compound. W.W. and X.Y carried out the materials characterizations. S.-K.K. provided the conjugated polymer. A.M.F. and R.N helped to take device photographs. N.M., J.X., Y.J. and Z.Z. helped with the experiments design and manuscript preparation. W.W., S.W., Z.B. and J.B.-H.T. wrote the manuscript. All the authors reviewed and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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Software and code

Policy information about availability of computer code

Data collection	No commercial or open source code were used for data collection. The only exception is the code to for the strain-distribution simulation.
Data analysis	No commercial or open source were used for data analysis. The only exception is the Matlab code for basic signal analysis such as signal filtering.

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Sample size	Sample is selected within the authors. No sample size was calculated due to the nature of electronics research.
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Population characteristics	Two of the authors, Dr. Xuzhou Yan and Weichen Wang are involved in the collection of EMG signals.
Recruitment	The two testers are within the authors of the current manuscript.
Ethics oversight	The Institutional Review Board (IRB) office in Stanford University has determined that this project (Protocol Number: IRB-55230) does not meet the definition of human subject research as defined in federal regulations 45 CFR 46.102 or 21 CFR 50.3.

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